

**SCOPE: CMOS, 12-BIT BUFFERED, MULTIPLYING D/A CONVERTER**

<u>Device Type</u>	<u>Generic Number</u>
01	MX7545S(x)/883B
02	MX7545T(x)/883B
03	MX7545U(x)/883B
04	MX7545GU(x)/883B

**Case Outline(s).** The case outlines shall be designated in Mil-Std-1835 and as follows:

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
Q	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20
E	CQCC1-N20	20 LCC	L20

**Absolute Maximum Ratings:**

V <sub>REF</sub> to GND .....	-0.3V, + 17V
Digital Input to DGND .....	-0.3V to V <sub>DD</sub>
V <sub>RFB</sub> to GND .....	±25V
V <sub>REF</sub> to GND .....	±25V
V <sub>OUT1</sub> to AGND .....	-0.3V to V <sub>DD</sub>
AGND to DGND .....	-0.3V to V <sub>DD</sub>

Lead Temperature (soldering, 10 seconds) .....	+300°C
Storage Temperature .....	-65°C to +150°C

Continuous Power Dissipation .....	T <sub>A</sub> =+70°C
20 pin CERDIP(derate 11.1mW/°C above +70°C) .....	889mW
20 pin LCC(derate 9.1mW/°C above +70°C) .....	727mW
Junction Temperature T <sub>J</sub> .....	+150°C
Thermal Resistance, Junction to Case, Θ <sub>JC</sub>	
20 pin CERDIP.....	40°C/W
20 pin LCC .....	20°C/W
Thermal Resistance, Junction to Ambient, Θ <sub>JA</sub> :	
20 pin CERDIP.....	90°C/W
20 pin LCC .....	110°C/W

**Recommended Operating Conditions**

Ambient Operating Range (T <sub>A</sub> ) .....	-55°C to +125°C
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Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TABLE 1. ELECTRICAL TESTS:**

TEST	Symbol	CONDITIONS		Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T <sub>A</sub> ≤ +125°C 1/ Unless otherwise specified						
<b>ACCURACY</b>								
Resolution NOTE 2	RES	V <sub>DD</sub> =+5V and +15V			All	12		Bits
Relative Accuracy	RA	V <sub>DD</sub> =+5V and +15V		1,2,3	01 02 03,04		±2.0 ±1.0 ±0.5	LSB
Differential Nonlinearity	DNL	10-bit monotonic, V <sub>DD</sub> =+5V and +15V		1,2,3	01		±4.0	LSB
		12-bit monotonic, V <sub>DD</sub> =+5V and +15V			02,03, 04		±1.0	
Gain Error NOTE 3	AE	V <sub>DD</sub> =5V		1,2,3	01 02		±20 ±10	LSB
				1 2,3	03		±5.0 ±6.0	
				1 2,3	04		1.0 2.0	
Gain Error NOTE 3	AE	V <sub>DD</sub> =15V		1,2,3	01 02 03		±25 ±15 ±10	LSB
				1 2,3	04		±6.0 ±7.0	
Gain Temperature Coefficient NOTE 2	TC <sub>AE</sub>	V <sub>DD</sub> =+5V			All		±5	ppm/°C
		V <sub>DD</sub> =+15V					±10	
Power Supply Rejection	PSRR	ΔV <sub>DD</sub> =±5%, V <sub>DD</sub> =5V		1 2,3	All		±0.015 ±0.03	%/%
		ΔV <sub>DD</sub> =±5%, V <sub>DD</sub> =15V		1 2,3			±0.01 ±0.02	
Out1 Leakage Current	I <sub>OUT1</sub>	V <sub>DD</sub> =+5V & +15V, _____ D0-D11=0V, WR=CS=0V		1 2,3	All		±10 ±200	nA
Output Current Settling Time NOTE 2	t <sub>SL</sub>	V <sub>DD</sub> =5V, To ±0.5LSB. OUT1 load is 100Ω    13pF, from _____ falling edge of WR with CS =0V		4	All		2	μs
Output Current Settling Time NOTE 2	t <sub>SL</sub>	V <sub>DD</sub> =15V. To ±0.5LSB. OUT1 load is 100Ω, output measured from trailing edge of _____ WR with CS=0V		4	All		2	μs
Feedthrough Error NOTE 2, NOTE 4	FTE	VREF=±10V, 10kHz sine wave V <sub>DD</sub> =5V		4	All		10	mVp-p
		VREF=±10V, 10kHz sine wave V <sub>DD</sub> =15V						

TEST	Symbol	CONDITIONS	Group A Subgroup	Device type	Limits Min	Limits Max	Units
		-55 °C ≤ T <sub>A</sub> ≤ +125 °C 1/ Unless otherwise specified					
Input Resistance	R <sub>IN</sub>	V <sub>DD</sub> =+5V and +15V	1,2,3	All	7	25	kΩ
Digital Input High Voltage	V <sub>IH</sub>	V <sub>DD</sub> =+5V	1,2,3	All	2.4		V
		V <sub>DD</sub> =+15V			13.5		
Digital Input Low Voltage	V <sub>IL</sub>	V <sub>DD</sub> =+5V	1,2,3	All		0.8	V
		V <sub>DD</sub> =+15V				1.5	
Digital Input Leakage Current	I <sub>IN</sub>	V <sub>IN</sub> =0V or V <sub>DD</sub> V <sub>DD</sub> =+5V or +15V	1 2,3	All		±1.0 ±10	μA
Digital Input Capacitance NOTE 2	C <sub>IN</sub>	D0-D11, V <sub>DD</sub> =5V	4	All		5	pF
		$\overline{\text{WR}}, \overline{\text{CS}}, V_{\text{DD}}=5\text{V}$				20	
		D0-D11, V <sub>IN</sub> =0V, V <sub>DD</sub> =15V				5	
		$\overline{\text{WR}}, \overline{\text{CS}}, V_{\text{IN}}=0\text{V}, V_{\text{DD}}=15\text{V}$				20	
Output Capacitance NOTE 2	C <sub>OUT1</sub>	V <sub>DD</sub> =5V D0-D11=0V, $\overline{\text{WR}}, \overline{\text{CS}}=0\text{V}$	4	All		70	pF
		V <sub>DD</sub> =5V D0-D11=V <sub>DD</sub> , $\overline{\text{WR}}, \overline{\text{CS}}=0\text{V}$				200	
		V <sub>DD</sub> =15V D0-D11=0V, $\overline{\text{WR}}, \overline{\text{CS}}=0\text{V}$				70	
		V <sub>DD</sub> =15V D0-D11=V <sub>DD</sub> , $\overline{\text{WR}}, \overline{\text{CS}}=0\text{V}$				200	
Chip Select to Write-Setup Time NOTE 5	t <sub>CS</sub>	V <sub>DD</sub> =5V	9	All	380		ns
		V <sub>DD</sub> =15V			200		
Chip Select to Write-Hold Time NOTE 5	t <sub>CH</sub>	V <sub>DD</sub> =+5V and +15V	9	All	0		ns
Write Pulse Width NOTE 5	t <sub>WR</sub>	V <sub>DD</sub> =+5V	9	All	400		ns
		t <sub>CS</sub> ≥ t <sub>WR</sub> , t <sub>CH</sub> ≥ 0, V <sub>DD</sub> =15V			240		
Data-Setup Time NOTE 5	t <sub>DS</sub>	V <sub>DD</sub> =5V	9	All	210		ns
		V <sub>DD</sub> =15V			120		
Data-Hold Time NOTE 5	t <sub>DH</sub>	V <sub>DD</sub> =+5V and +15V	9	All	30		ns
Supply Current	I <sub>DD</sub>	All digital inputs V <sub>IL</sub> or V <sub>IH</sub> V <sub>DD</sub> =+5V and +15V	1,2,3	All		2.0	μA
		All digital inputs 0V or V <sub>DD</sub> V <sub>DD</sub> =+5V and +15V	1 2,3			100 500	

- NOTE 1:  $V_{DD}=+15V$ ,  $V_{OUT1}=0V$ ;  $VREF=+10V$ ,  $AGND=DGND$ , unless otherwise specified.  
 NOTE 2: Characteristics supplied for use as a typical design limit, but not production tested.  
 NOTE 3: Measured using internal feedback resistor and includes effect of 5ppm max gain TC.  
 NOTE 4: Feedthrough error can be reduced by connecting the metal lid on the package to ground.  
 NOTE 5: Timing Diagram. See Commercial Datasheet

**ORDERING INFORMATION:**

	Package	Pkg. Code	MAXIM PART #
01	20 pin CERDIP	J20	MX7545SQ/883B
01	20 pin LCC	L20	MX7545SE/883B
02	20 pin CERDIP	J20	MX7545TQ/883B
02	20 pin LCC	L20	MX7545TE/883B
03	20 pin CERDIP	J20	MX7545UQ/883B
03	20 pin LCC	L20	MX7545UE/883B
04	20 pin CERDIP	J20	MX7545GUQ/883B
04	20 pin LCC	L20	MX7545GUE/883B

**TERMINAL CONNECTIONS:**

J20 & L20	
Pin	
1	OUT1
2	AGND
3	DGND
4	D11(MSB)
5	D10
6	D9
7	D8
8	D7
9	D6
10	D5
11	D4
12	D3
13	D2
14	D1
15	D0(LSB)
16	— CS
17	— WR
18	$V_{DD}$
19	VREF
20	$R_{FB}$

## QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883:
  1. Test condition A, B, C, D.
  2. TA = +125°C, minimum.
  3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

**TABLE 2. ELECTRICAL TEST REQUIREMENTS**

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9
Group C and D End-Point Electrical Parameters Method 5005	1

\* PDA applies to Subgroup 1 only.

\*\* Subgroup 4 shall be tested at initial qualification and upon redesign. Sample size will be 116 units.