

SCOPE: CMOS 8-Bit, μ P-Compatible, 12-Bit D/A Converter

<u>Device Type:</u>	<u>Generic Number:</u>
-01	MX7548S(x)/883B
-02	MX7548T(x)/883B

Case Outline(s).

<u>Outline Letter</u>	<u>Mil-Std-1835</u>	<u>Case Outline</u>	<u>Package Code</u>
Q	GDIP1-T20 or CDIP2-T20	20 Lead CERDIP	J20
E	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings:

V_{DD} to DGND	+17V
VREF to AGND	± 25 V
V_{RFB} to AGND	± 25 V
Digital Input Voltage to DGND	-0.3V, V_{DD}
V_{OUT1} to DGND	-0.3V, V_{DD}
AGND to DGND	-0.3V, V_{DD}

Lead Temperature (soldering, 10 seconds)	+300°C
Storage Temperature	-65°C to +150°C

Continuous Power Dissipation	$T_A = +70^\circ\text{C}$
20 pin CERDIP (derate 10mW/°C above +70°C)	889mW
20 pin LCC (derate 9.09mW/°C above +70°C)	727mW
Junction Temperature T_J	+150°C
Thermal Resistance, Junction to Case, θ_{JC}	
20 pin CERDIP	40°C/W
20 pin LCC	20°C/W
Thermal Resistance, Junction to Ambient, θ_{JA} :	
20 pin CERDIP	90°C/W
20 pin LCC	110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A)	-55°C to +125°C
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Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55°C ≤ T _A ≤ +125°C 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC PERFORMANCE							
Resolution	N		1,2,3	All	12		Bits
Integral Nonlinearity	INL		1,2,3	01 02		±1 ±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic to 12 bits	1,2,3	01 02		±1 ±0.5	LSB
Gain Error	FSE	Using internal feedback resistor	1 2,3	01		±2 ±3	LSB
Gain Error	FSE	Using internal feedback resistor	1 2,3	02		±1 ±2	LSB
Gain Tempco	TC _{FS}	NOTE 2 (ΔGain/ΔTemp)		All		±5	ppm/°C
DC Supply Rejection	PSR	ΔV _{DD} =±5% (ΔGain/ΔSupply)	1 2,3	All		±0.001 ±0.002	%/%
DYNAMIC PERFORMANCE							
Current Settling Time	t _s	To 0.5LSB, OUT1 load: R _L =100 Ω: CL=13pF: DAC register alternately loaded with all 1s and all 0s.	4	All		1	μs
Digital to Analog Glitch Impulse	Q	V _{REF} =0V, OUT1 load: R _L =100 Ω: CL=13pF: DAC register alternately loaded with all 1s and all 0s.	4,5,6	All		200	nV-s
AC Feedthrough at OUT1 NOTE 3	FTE	V _{REF} =±10Vp-p at 10kHz, DAC register loaded with all 0s.	4,5,6	All		5	mVp-p
Total Harmonic Distortion	THD	V _{REF} =6V _{RMS} at 1kHz, DAC register loaded with all 1s.	4,5,6	All		-90	dB
Output Noise Voltage Density	en	10Hz to 100kHz. Measured between R _{FB} and OUT1.	4,5,6	All		15	nV/Hz
REFERENCE INPUT							
Input Resistance	R _{REF}	V _{REF} pin to OUT1	1,2,3	All	7	15	kΩ
ANALOG OUTPUT							
OUT1 Leakage Current	ILKG	DAC register loaded with all 0s.	4 5,6	All		±5 ±100	nA
OUT1 Capacitance NOTE 2	C _{OUT1}	DAC register loaded with all 0s DAC register loaded with all 1s	4,5,6	All		70 140	pF

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55°C ≤ T _A ≤ +125°C 1/ Unless otherwise specified	GROUP A Subgroup	Device type	Limits Min	Limits Max	Units
DIGITAL INPUTS							
Digital Input High Voltage	V _{IH}		1,2,3	All	2.4		V
Digital Input Low Voltage	V _{IL}		1,2,3	All		0.8	V
Digital Input Leakage Current	I _{IN}	Digital Inputs at 0V or V _{DD}	1,2,3	All		±1	μA
Input Capacitance NOTE 2	C _{IN}	Digital Inputs at 0V or V _{DD}	4,5,6	All		7	pF
SWITCHING CHARACTERISTICS NOTES 2, 4							
Data Valid Setup	t _{DS}		9,10,11	All	160		ns
Data Valid Hold	t _{DH}		9,10,11	All	10		ns
_____ _____ CSMSB or CSLSB _____ to WR Setup	t _{CWS}		9,10,11	All	0		ns
_____ _____ CSMSB or CSLSB _____ to WR Hold	t _{CWH}		9,10,11	All	0		ns
_____ _____ LDAC to WR Setup	t _{LWS}		9,10,11	All	0		ns
_____ _____ LDAC to WR Hold	t _{LWH}		9,10,11	All	0		ns
_____ _____ WR Pulse Width	t _{WR}		9,10,11	All	120		ns
POWER SUPPLY							
V _{DD} Range NOTE 5	V _{DD}	V _{DD} =+12V or +15V V _{DD} =+5V	1,2,3	All	+11.4 +4.75	+15.75 +5.25	V
I _{DD} Range	I _{DD}	All digital inputs at V _{IL} or V _{IH} V _{DD} =+12V or +15V V _{DD} =+5V	1,2,3	All		3 2	mA
		All digital inputs at 0V or V _{DD} V _{DD} =+12V or +15V V _{DD} =+5V	1,2,3	All		1 300	mA μA

NOTE 1: V_{DD}=+5V, +12V or +15V; V_{OUT1}=AGND=DGND=0V; V_{REF}=+10V, unless otherwise noted.

NOTE 2: Characteristics supplied for use as a typical design limit but not production tested.

NOTE 3: Feedthrough can be further reduced by connecting the metal lid to DGND on the ceramic package.

NOTE 4: Timing shown in commercial datasheet, Figure 5.

NOTE 5: Specifications are guaranteed over these ranges.

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TERMINAL CONNECTIONS:

	MX7548		
	J20 & L20		J20 & L20
1	I _{OUT}	11	DB3
2	AGND	12	DB2
3	DGND	13	DB1
4	<u> </u> CSMSB	14	DB0(LSB)
5	<u> </u> DF/DOR	15	<u> </u> LDAC
6	CTRL	16	<u> </u> CSLSB
7	(MSB)DB7	17	<u> </u> WR
8	DB6	18	V _{DD}
9	DB5	19	VREF
10	DB4	20	R _{FB}

ORDERING INFORMATION:

01	J20	MX7548SQ/883B
01	L20	MX7548SE/883B
02	J20	MX7548TQ/883B
02	L20	MX7548TE/883B

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QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with Mil-Prf-38535, Appendix A as Specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. $T_A = +125^{\circ}\text{C}$, minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, Including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

- a. End-point electrical parameters shall be specified in Table 1.
- b. Steady-state life test, Method 1005 of Mil-Std-883.
 1. Test condition A, B, C, D.
 2. $T_A = +125^{\circ}\text{C}$, minimum.
 3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups Per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6**, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, 5, 6 shall be tested at initial qualification and upon redesign.
Sample size will be 116 units.

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