SCOPE: CMOS DUAL 12-BIT DOUBLE-BUFFERED µP-COMPATIBLE DAC

Device Type	Generic Number
01	MX7549S(x)/883B
02	MX7549T(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20
E	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

V_{DD} to DGND ..... -0.3V, +17V
VREFA, VREFB to AGND ..... ±25V
$V_{RFB}A$, $V_{RFB}B$ to AGND ..... ±25V
Digital Input Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)
IOUTA, IOUTB Voltage to DGND ..... -0.3V, (V_{DD}+0.3V)
AGND to DGND ..... -0.3V, (V_{DD}+0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
20 lead CERDIP(derate 11.11mW/°C above +70°C) 889mW
20-Pin LCC (derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 20 lead CERDIP..... 40°C/W
Case Outline 20-Pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 20 lead CERDIP..... 90°C/W
Case Outline 20-Pin LCC ..... 110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V_{DD}) ..... +10.8V dc to +15.75V dc

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SWITCH							
Resolution	N		1,2,3	All	12		Bits
Integral Nonlinearity	INL		1,2,3	01 02	-1.0 -0.5	+1.0 +0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All		±1.0	LSB
Gain Error	FSE		1,2,3	01 02		±6.0 ±3.0	LSB
Gain Tempco ΔGain/ΔTemp.	TCFS	2/	4	All		±5.0	ppm/°C
IOUTA, IOUTB Leakage Current	I_{LKG}	DAC Register loaded with all 0s	1 2,3	All		±20 ±250	nA
Reference Input Resistance	RREF		1,2,3	All	7	18	kΩ
VREFA, VREFB Input Resistance Match	ΔR_{REF}		1,2,3	01 02		±3.0 ±2.0	%
		DYNAMIC PERFORMANCE 3/					
Output-Current Settling Time 4/	t_S		9,10,11	All		1.5	µs
AC Feedthrough VREF to IOUT_ 5/			4 5,6	All		-70 -65	dB
Output Capacitance	C_{OUT}	DAC_ loaded with all 0's DAC_ leaded with all 1's	4,5,6	All		80 160	pF
DIGITAL INPUT							
Input Current	I_{IN}	V_{IN}= V_{DD}	1 2,3	All		±1 ±10	µA
Input Low Voltage	V_{IL}		1,2,3	All		0.8	V
Input High Voltage	V_{IH}		1,2,3	All	2.4		V
Output Capacitance	C_{IN}	3/	4,5,6	All		7.0	pF
SUPPLY							
Power Supply	I_{DD}	All digital inputs at V_{IH}	1,2,3	All		3.0	mA
Power-Supply Rejection	ΔGain/Δ V_{DD}	V_{DD}=10.8V to 15.75V	4,5,6	All		±.002	%/%
TIMING							
Address Valid to Write Setup Time	t_1		9 10,11	All	50 90		ns
Address Valid to Write Hold Time	t_2		9,10,11	All	0		ns
Data Setup Time	t_3		9 10,11	All	70 120		ns
Data Hold Time	t_4		9,10,11	All	0		ns
Chip Select or Update to Write Setup	t_5		9,10,11	All	0		ns
Chip Select or Update to Write Hold	t_6		9,10,11	All	0		ns
Write Pulse Width	t_7		9 10,11	All	50 90		ns
Clear Pulse Width	t_8		9 10,11	All	75 90		ns

NOTE 1: V_{DD}=+15V±5%, VREFA=VREFB=+10V, IOUTA=IOUTB=AGND=DGND=0V. At V_{DD}=+5V, the device is functional with degraded performance. Performance at power-supply tolerance limits is guaranteed by Power-Supply Rejection test.

NOTE 2: Guaranteed by design.

NOTE 3: If not tested, shall be guaranteed to the limits in Table 1.

NOTE 4: IOUT LOAD=100Ω, CEXT=13pF. DAC output measured from falling edge of $\overline{WR}$. Measured to 0.01% of full-scale range.

NOTE 5: VREF_=20Vp-p 10kHz sine wave. DAC register is loaded with all zeros.

NOTE 6: Measured with VREFA=VREFB=0V. IOUTA, IOUTB load=100Ω, CEXT=13pF. DAC registers alternately loaded with all 0's and 1's.

TRUTH TABLE

CLR	$\overline{UPD}$	$\overline{CS}$	$\overline{WR}$	A2	A1	A0	FUNCTION
0	X	X	1	X	X	X	No data transfer.
0	1	1	X	X	X	X	No data transfer.
1	X	X	X	X	X	X	All registers cleared.
0	1	0	⎍	0	0	0	DAC A low-nibble register loaded from data bus.
0	1	0	⎍	0	0	1	DAC A mid-nibble register loaded from data bus.
0	1	0	⎍	0	1	0	DAC A high-nibble register loaded from data bus.
0	1	0	⎍	0	1	1	DAC A register loaded from nibble registers.
0	1	0	⎍	1	0	0	DAC B low-register loaded from data bus.
0	1	0	⎍	1	0	1	DAC B mid-nibble loaded from data bus.
0	1	0	⎍	1	1	0	DAC B high-register loaded from data bus.
0	1	0	⎍	1	1	1	DAC B register loaded from nibble registers.
0	0	1	⎍	X	X	X	DAC A and DAC B registers updated simultaneously

TERMINAL CONNECTIONS:

Lead #	J20/ L20
1	D3
2	D2
3	D1
4	D0
5	$\overline{UPD}$
6	A2
7	A1
8	A0
9	$\overline{CS}$
10	$\overline{WR}$
11	CLR
12	DGND
13	V_{REFB}
14	R_{FBB}
15	I_{OUTB}
16	AGND
17	I_{OUTA}
18	R_{FBA}
19	V_{REFA}
20	V_{DD}

ORDERING INFORMATION:

Pkg.	
J20	MX7549SQ/883B
L20	MX7549SE/883B
J20	MX7549TQ/883B
L20	MX7549TE/883B

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9, 10, 11
Group A Test Requirements Method 5005	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.
** Subgroups 10 and 11, if not tested shall be guaranteed to the limits of Table 1.