SCOPE: CMOS DUAL 8-BIT BUFFERED MULTIPLYING D/A CONVERTER

Device Type	Generic Number
01	MX7628T(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter	Mil-Std-1835	Case Outline	Package Code
Q	GDIP1-T20 or CDIP2-T20	20 LEAD CERDIP	J20
E	CQCC1-N20	20-Pin Ceramic LCC	L20

Absolute Maximum Ratings

V_{DD} to AGND ..... 0V, +17V
V_{DD} to DGND ..... 0V, +17V
AGND to DGND ..... V_{DD}
DGND to AGND ..... V_{DD}
Digital Input Voltage to DGND ..... -0.3V, V_{DD}
IOUTA, IOUTB Voltage to DGND ..... -0.3V, V_{DD}
VREFA, VREFB to AGND ..... ±25V
$\overline{\text{VREFA}}$, $\overline{\text{VREFB}}$ to AGND ..... ±25V

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
20 lead CERDIP(derate 11.11mW/°C above +70°C) 889mW
20-Pin LCC (derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC:
Case Outline 20 lead CERDIP..... 40°C/W
Case Outline 20-Pin LCC ..... 20°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
Case Outline 20 lead CERDIP..... 90°C/W
Case Outline 20-Pin LCC ..... 110°C/W

Recommended Operating Conditions.

Ambient Operating Range (T_A) ..... -55°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
DC ACCURACY							
Resolution	N		1,2,3	All	8		Bits
Integral Nonlinearity	INL		1,2,3	01		±0.5	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All		±1.0	LSB
Gain Error	FSE	Measured using RFBA, RFBB, DAC registers loaded with all 1's.	1 2,3	All		±2.0 ±3.0	LSB
Gain Tempco ΔGain/ΔTemp.	TCFS	2/	4	All		±35	ppm/°C
Supply Rejection	PSR	ΔV_{DD}=±5%, NOTE 3	1 2,3	All		±0.01 ±0.02	%FSR/%
I_{OUTA}, I_{OUTB} Leakage Current	I_{LKG}	DAC Register loaded with all 0s	1 2,3	All		±50 ±200	nA
REFERENCE INPUT							
VREFA, VREFB Input Resistance	RREF		1,2,3	All	8	15	kΩ
VREFA, VREFB Input Resistance Match	ΔR_{REF}		1,2,3	All		±1.0	%
		DYNAMIC PERFORMANCE					
Output-Current Settling Time NOTE 3	t_S	To 0.5LSB, IOUT Load is 100Ω || 13pF, D0-D7=0V to 5V to 0V, OUTA=OUTB, $\overline{WR}$=$\overline{CS}$=0V	9 10,11	All		350 400	ns
AC Feedthrough VREFA to I_{OUTA} NOTE 3	FTE	DAC registers loaded with all 0s. VREFA=20Vp-p, 10kHz sine wave, VREFB=0V.	4	All		-70	dB
AC Feedthrough VREFB to I_{OUTB} NOTE 3	FTE	DAC registers loaded with all 0s. VREFB=20Vp-p, 10kHz sine wave, VREFA=0V.	4	All		-70	dB
Output Capacitance	C_{OUT}	DACA, DACB loaded with all 0's DACA, DACB leaded with all 1's	4	All		25 60	pF
DIGITAL INPUT							
Input Current (I_{OUTA}, I_{OUTB})	I_{IN}	V_{IN}=0V or V_{DD}	1 2,3	All		±1 ±10	µA
Input Low Voltage	V_{IL}		1,2,3	All		0.8	V
Input High Voltage	V_{IH}		1,2,3	All	2.4		V
Input Capacitance	C_{IN}	D0-D7 $\overline{WR}$, $\overline{CS}$, DAC A/DAC B	4	All		10 15	pF
SUPPLY							
Power Supply	I_{DD}	Digital inputs at V_{IH} or V_{IL} Digital inputs at 0V or V_{DD}	1 2,3 1 2,3	All		2.0 2.5 0.1 0.5	mA

TEST	Symbol	CONDITIONS -55 °C ≤T_A≤ +125°C 1/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
SWITCHING CHARACTER-ISTICS							
Chip Select to Write- Setup Time	t_{CS}		9 10,11	All	160 210		ns
Chip Select to Write- Hold Time	t_{CH}		9,10,11	All	10		ns
DAC Select to Write-Setup Time	t_{AS}		9 10,11	All	160 210		ns
DAC Select to Write-Hold Time	t_{AH}		9,10,11	All	10		ns
Write Pulse Width	t_{WR}		9 10,11	All	150 210		ns
Data-Setup Time	t_{DS}		9 10,11	All	160 210		ns
Data-Hold Time	t_{DH}		9,10,11	All	10		ns

NOTE 1: V_{DD}=10.8V or 15.75V, VREF =+10V, VOUTA=VOUTB. Specifications apply to both DACs unless otherwise specified.

NOTE 2: Guaranteed but not production tested.

NOTE 3: Included for design guidance, not subject to test.

TERMINAL CONNECTIONS:

PIN	J20/ L20
1	AGND
2	OUTA
3	RFBA
4	VREFA
5	DGND
6	$\overline{\text{DAC A/DAC B}}$
7	D7(MSB)
8	D6
9	D5
10	D4
11	D3
12	D2
13	D1
14	D0(LSB)
15	$\overline{\text{CS}}$
16	$\overline{\text{WR}}$
17	V_{DD}
18	VREFB
19	RFBB
20	OUTB

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 9, 10, 11***
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, capacitance tests shall be tested at initial qualification and upon redesign. Sample size will be 116 units.

** Subgroups 10 and 11, if not tested, shall be guaranteed to the limits of Table 1.