SCOPE: CMOS QUAD SERIAL INTERFACE, 8-BIT D/A CONVERTER

Device Type	Generic Number
01	MAX500B(x)/883B

Case Outline(s). The case outlines shall be designated in Mil-Std-1835 and as follows:

Outline Letter		Mil-Std-1835	Case Outline	Package Code
MAXIM	SMD			
JE	E	GDIP1-T16 or CDIP2-T16	16 LEAD CERDIP	J16
LP	2	CQCCI-N20	20 LEADLESS CHIP CARRIER	L20

Absolute Maximum Ratings

V_{DD} to AGND ..... -0.3V, +17V
V_{DD} to DGND ..... -0.3V, +17V
V_{SS} to DGND..... -7V, V_{DD} +0.3V
V_{DD} to V_{SS} ..... -0.3V, +24V
Digital Input Voltage to DGND ..... -0.3V,(V_{DD} +0.3V)
V_{REF} to AGND ..... -0.3V,(V_{DD} +0.3V)
V_{OUT} to AGND 1/..... -0.3V,(V_{DD} +0.3V)

Lead Temperature (soldering, 10 seconds) ..... +300°C
Storage Temperature ..... -65°C to +150°C

Continuous Power Dissipation ..... T_A=+70°C
16 pin CERDIP(derate 10mW/°C above +70°C) 800mW
20 pin LCC(derate 9.1mW/°C above +70°C) 727mW
Junction Temperature T_J ..... +150°C
Thermal Resistance, Junction to Case, ΘJC
16 pin CERDIP..... 40°C/W
20 pin LCC ..... 50°C/W
Thermal Resistance, Junction to Ambient, ΘJA:
16 pin CERDIP..... 20°C/W
20 pin LCC ..... 110°C/W

Recommended Operating Conditions

Ambient Operating Range (T_A) ..... -55°C to +125°C
Positive Supply Voltage (V_{DD}) Single Supply …..... +14.25V to +15.75V
Positive Supply Voltage, (V_{DD}) Dual Supply ……..... +11.4V to +16.5V

1/ The outputs may be shorted to AGND provided that the power dissipation of the package is not exceeded. Typical short circuit current to AGND is 25mA.

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TABLE 1. ELECTRICAL TESTS:

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 2/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
STATIC PERFORMANCE		**DUAL SUPPLY SPECIFICATION**					
Resolution	N		1,2,3	All	8		Bits
Total unadjusted error	BT	V_{DD}=15V±5%, V_{REF}=10V	1,2,3	All		±2.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All		±1.0	LSB
Zero Code Error	BPOE		1 2,3	All		±20 ±30	mV
REFERENCE INPUT							
Reference Input Range	V_{REF}		1,2,3	All	2	V_{DD}-4	V
Reference Input Resistance	R_{IN}	Pins V_{REF}C and V_{REF}D Pins V_{REF}A/B	1,2,3	All	11 5.5		kΩ
Reference Input Capacitance	C_{REF}IN	Code dependent NOTE 3	4	All		100	pF
Channel-to-Channel Isolation		NOTE 3, 4	4	All	-60		dB
AC Feedthrough		NOTE 3, 4	4	All	-70		dB
DIGITAL INPUTS							
Input High Level Voltage	V_{IH}		1,2,3	All	2.4		V
Input Low Level Voltage	V_{IL}		1,2,3	All		0.8	V
Output High Level Voltage	V_{OH}	I_{OUT}=-1mA, SRO only	1,2,3	All	V_{DD}-1		V
Output Low Level Voltage	V_{OL}	I_{OUT}=+1mA, SRO only	1,2,3	All	0.4		V
Input Leakage Current	I_{IL}	$\overline{\text{LOAD}}$, NOTE 5 $\overline{\text{LOAD}}$=0V, NOTE 5	1,2,3	All		±1.0 30	µA
Digital Input Capacitance	C_{DIG}IN	NOTE 5	1,2,3	All		8	pF
DYNAMIC PERFORMANCE							
Voltage Output Slew Rate		NOTE 3, NOTE 6	4	All	3		V/µs
V_{OUT} Settling Time	t_S	To 0.5 LSB, V_{REF}=10V, V_{DD}=+15V, 2kΩ in parallel with 100pF load. NOTE 3	9	All		4.0	µs
Output Load Resistance		V_{OUT}=10V	1,2,3	All	2		kΩ
POWER SUPPLIES		**Dual Supply Specifications**					
Positive Supply Voltage	V_{DD}	For specification performance	1,2,3	All	11.4	16.5	V
Positive Supply Current	I_{DD}	Outputs unloaded	1 2,3	All		10 12	mA
Negative Supply Current	I_{SS}	Outputs unloaded	1 2,3	All		-9 -10	mA
SWITCHING CHARACTERISTICS		**Three-Wire Mode** NOTE 6					
SDA valid to SCL setup	t_{S1}	See Figure 5	9	All	150		ns
SDA valid to SCL hold	t_H	See Figure 5	9	All	0		ns
SCL high time	t1		9	All	350		ns
SCL low time	t2		9	All	350		ns
$\overline{\text{LOAD}}$ pulse width	t_{LDW}		9	All	150		ns

TEST	Symbol	CONDITIONS -55 °C <=T_A<= +125°C 2/ Unless otherwise specified	Group A Subgroup	Device type	Limits Min	Limits Max	Units
$\overline{\text{LOAD}}$ delay from SCL	t_{LDS}		9	All	150		ns
$\overline{\text{LDAC}}$ pulse width	t_{LDAC}		9	All	150		ns
SRO output delay	t_{D1}	C_{LOAD}=50pF	9	All		150	ns
Switching Characteristics		**Two-Wire Mode** NOTE 6 Figure 6					
SDA valid to SCL setup	t_{S2}	Start condition	9	All	100		ns
SCL valid to SDA setup	t_{S1}	Start condition	9	All	150		ns
SDA valid to SCL hold	t_H		9	All	0		ns
SCL high time	t_1		9	All	350		ns
SCL low time	t_2		9	All	350		ns
SDA valid to rising SCL	t_{S3}		9	All	125		ns
$\overline{\text{LOAD}}$ pulse width	t_{LDW}		9	All	150		ns
$\overline{\text{LDAC}}$ pulse width	t_{LDAC}		9	All	150		ns
SRO output delay	t_{D1}	C_{LOAD}=50pF	9	All		150	ns
STATIC PERFORMANCE 7/		**SINGLE SUPPLY SPECIFICATION**					
Resolution	N		1,2,3	All	8		Bits
Total unadjusted error	BT	V_{DD}=15V±5%, V_{REF}=10V	1,2,3	All		±2.0	LSB
Differential Nonlinearity	DNL	Guaranteed monotonic	1,2,3	All		±1.0	LSB
Zero Code Error	BPOE		1 2,3	All		±20 ±30	mV
Power Supplies 7/		**Single Supply Specifications**					
Positive Supply Voltage	V_{DD}	For specification performance	1,2,3	All	14.25	15.75	V
Positive Supply Current	I_{DD}	Outputs unloaded	1 2,3	All		10 12	mA

NOTE 2: V_{DD}=+11.4V to 16.5V, V_{SS}=-5V±10%, AGND=DGND=0V, and V_{REF}=+2V to (V_{DD}-4V).
NOTE 3: Guaranteed by design. Not production tested.
NOTE 4: $\overline{\text{LDAC}}$=VREF=10kHz, 10V peak-to-peak sine wave.
NOTE 5: LOAD has a weak internal pull-up resistor to $V_{DD.}$
NOTE 6: Sample tested at +25°C to ensure compliance.
NOTE 7: V_{DD}=+15V±5%, V_{SS}=AGND=DGND=0V and V_{REF}=10V.
Figures 5 and 6: See Commercial Datasheet.

	Package	ORDERING INFORMATION:	SMD Number
01	16 pin CERDIP	MAX500BMJE/883B	5962-9452702MEA
01	20 pin LCC	MAX500BMLP/883B	5962-9452702M2C

TERMINAL CONNECTIONS

	J16	20 LCC		J16	20 LCC
1	$V_{OUT}B$	NC	11	SRO	SDA
2	$V_{OUT}A$	$V_{OUT}B$	12	$V_{REF}D$	$\overline{\text{LOAD}}$
3	V_{SS}	$V_{OUT}A$	13	$V_{REF}C$	SCL
4	V_{REF} A/B	V_{SS}	14	V_{DD}	NC
5	AGND	$V_{REF}A/B$	15	$V_{OUT}D$	SRO
6	DGND	AGND	16	$V_{OUT}C$	$V_{REF}D$
7	$\overline{\text{LDAC}}$	NC	17		$V_{REF}C$
8	SDA	NC	18		V_{DD}
9	$\overline{\text{LOAD}}$	DGND	19		$V_{OUT}D$
10	SCL	$\overline{\text{LDAC}}$	20		$V_{OUT}C$

QUALITY ASSURANCE

Sampling and inspection procedures shall be in accordance with MIL-Prf-38535, Appendix A as specified in Mil-Std-883.

Screening shall be in accordance with Method 5004 of Mil-Std-883. Burn-in test Method 1015:

1. Test Condition, A, B, C, or D.
2. TA = +125°C minimum.
3. Interim and final electrical test requirements shall be specified in Table 2.

Quality conformance inspection shall be in accordance with Method 5005 of Mil-Std-883, including Groups A, B, C, and D inspection.

Group A inspection:

1. Tests as specified in Table 2.
2. Selected subgroups in Table 1, Method 5005 of Mil-Std-883 shall be omitted.

Group C and D inspections:

a. End-point electrical parameters shall be specified in Table 1.
b. Steady-state life test, Method 1005 of Mil-Std-883:
   1. Test condition A, B, C, D.
   2. TA = +125°C, minimum.
   3. Test duration, 1000 hours, except as permitted by Method 1005 of Mil-Std-883.

TABLE 2. ELECTRICAL TEST REQUIREMENTS

Mil-Std-883 Test Requirements	Subgroups per Method 5005, Table 1
Interim Electric Parameters Method 5004	1
Final Electrical Parameters Method 5005	1*, 2, 3, 4**, 5, 6, 9
Group A Test Requirements Method 5005	1, 2, 3, 4**, 5, 6, 9
Group C and D End-Point Electrical Parameters Method 5005	1

* PDA applies to Subgroup 1 only.

** Subgroup 4, Capacitance tests are performed initially and after any design changes.