DATA SHEET
SE4110S: GPS Receiver IC

Applications

- High sensitivity / low power GPS and A-GPS applications
- Portable navigation devices, mobile phones and GPS peripheral devices
- Telematics equipment

Features

- Single-conversion L1-band GPS radio with integrated IF filter
- Integrated LNA; 1.6 dB typ. noise figure
- Low RF system noise figure; 2.25 dB typ.
- Low 10 mA operating current with 2.7-3.3 V supply; 8 mA with internal LNA disabled
- Standby current <10 µA
- Fully Integrated PLL, compatible with 13, 16.368, 19.5 and 26MHz reference frequencies
- 2-bit SIGN & MAG Digital IF output
- Integrated VCO and resonator
- I/O supply range extends down to 1.7 V
- 2.2 x 2.2 x 0.3 mm, 46 pad, 250um pitch, SnAg solder bump, RoHS-compliant package

Ordering Information

Part No.	Package	Remark
SE4110S-R	46-Pad Chip-Scale Package	Shipped in Tape & Reel

Functional Block Diagram

Product Description

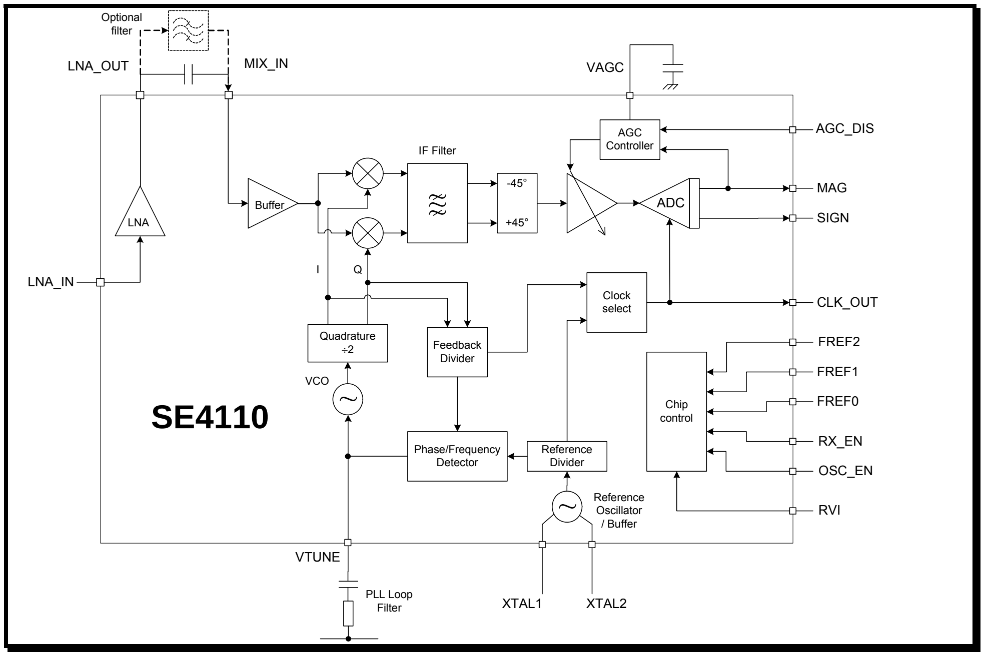
The SE4110S is a highly integrated GPS receiver offering high performance and low power operation in a wide range of low-cost applications. It is particularly well suited to cellphone and high sensitivity L1-band GPS / A-GPS systems.

The SE4110S includes an on-chip LNA, a low IF receiver with a linear AGC and 2-bit analogue-to-digital converter (ADC). The receiver incorporates a fully integrated image reject mixer so no SAW filter is required in many applications. There is also an on-chip IF filter.

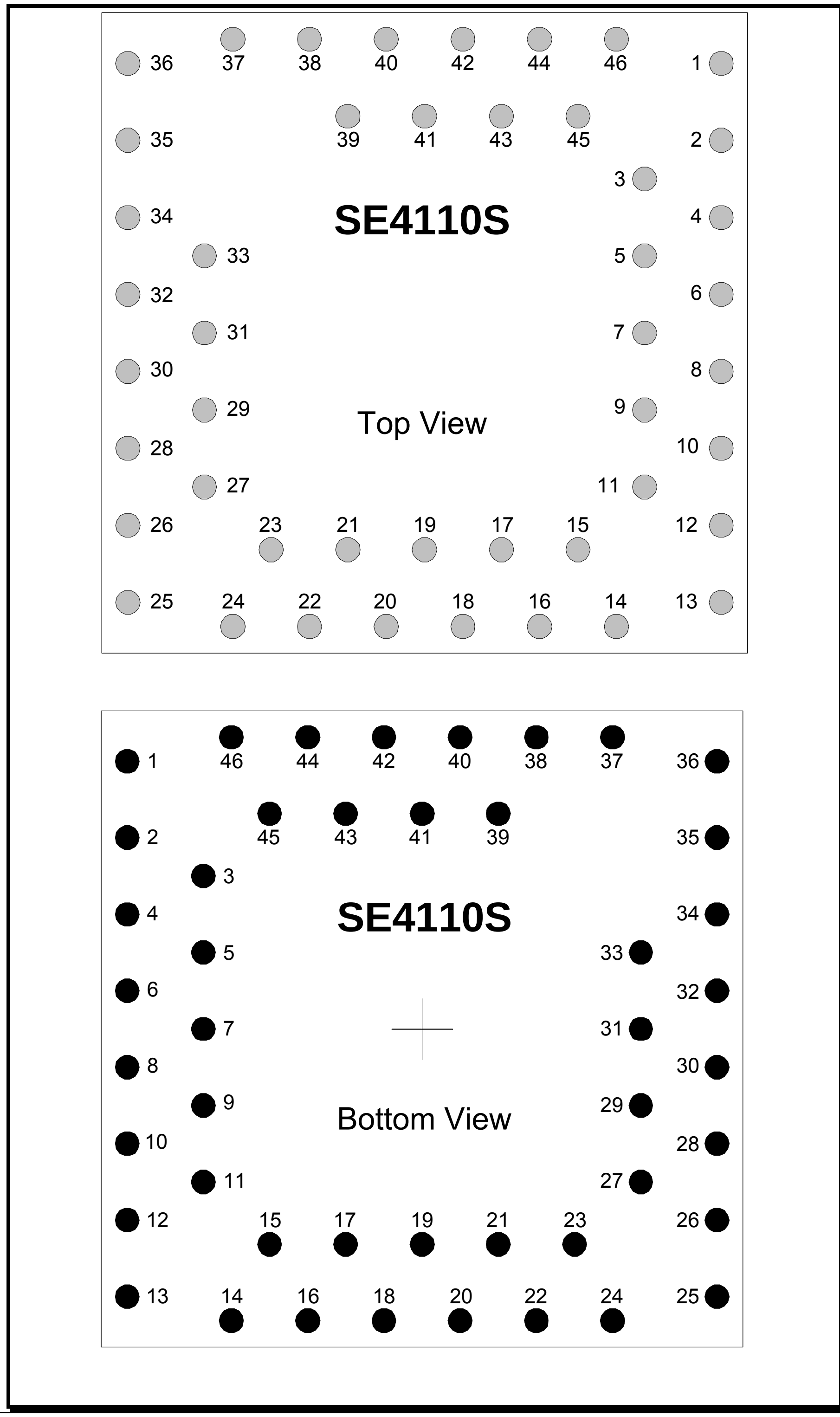
The SE4110S supports a wide range of reference frequencies addressing both traditional GPS systems and emerging mobile phone applications. The synthesizer is highly integrated requiring only two passive components to implement an off-chip loop filter.

The SE4110S is optimized for the lowest possible power consumption consistent with the very low external component count.

The SE4110S incorporates current controlled low-spurious output buffers which may optionally be run from a separate external supply to interface to low voltage systems. The buffers supply sufficient current to drive most baseband devices directly.


Optional filter
LNA_OUT
MIX_IN
VAGC
AGC Controller
AGC_DIS
IF Filter
Buffer
LNA
-45°
+45°
ADC
MAG
SIGN
LNA_IN
I
Q
Clock select
CLK_OUT
Quadrature ÷2
Feedback Divider
FREF2
FREF1
FREF0
VCO
SE4110
Chip control
RX_EN
OSC_EN
Phase/Frequency Detector
Reference Divider
Reference Oscillator / Buffer
RVI
VTUNE
PLL Loop Filter
XTAL1
XTAL2

Pad Diagram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5 33
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8 30
9 Bottom View 29
10 28
11 27
12 15 17 19 21 23 26
13 14 16 18 20 22 24 25

Pad Description

Pad	Label	Function	Connection
1	VCC_LNA	Analogue power supply for LNA	Connect to VCC via dedicated decoupling network, to enable LNA. Connect to GND to disable LNA
2	GND	GND connection	Connect to GND
3	VCC_AGC	Analogue power supply for AGC	Connect to VCC
4	LNA_IN	LNA RF input	DC blocking capacitor required. Connect to matching network in a compact RF layout.
5	GND	GND connection	Connect to GND
6	GND	GND connection	
7	*NC*	*(reserved)*	*Leave unconnected*
8	GND	GND connection	Connect to GND
9	GND	GND connection	
10	GND	GND connection	
11	VDD_FSE1	Power supply for configuration logic	Connect to VCC
12	VDD_FSE2	Power supply for configuration logic	
13	VAGC	AGC filter capacitor	Single capacitor to GND (Pad also allows external control of AGC when AGC_DIS='1')
14	RX_EN	Receiver enable	Connect to VDD to enable Radio Connect to VSSN / GND to disable Radio
15	AGC_DIS	AGC Inhibit Input	AGC Gain hold (Connect to VDD) or Enable AGC (Connect to VSSN / GND)
16	VSSN	Ground return for digital interface	Connect to GND, or digital ground for baseband IC
17	VDDN	Digital power supply for digital interface	Connect to VDD, or digital supply for baseband IC
18	*NC*	*(reserved)*	*Leave unconnected*
19	*NC*	*(reserved)*	
20	*NC*	*(reserved)*	
21	FREF0	Frequency reference select input (bit 0)	Select desired Reference / IF / CLK_OUT frequency plan as per "FREF Hardware Configuration" Table (Connect to RX_EN or VSSN / GND as required)
22	CLK_OUT	Sample clock output	ADC Sample Clock output to baseband IC, at VDDN logic levels
23	SIGN	SIGN output data	ADC SIGN output to baseband IC, at VDDN logic levels

Pad	Label	Function	Connection
24	MAG	MAG output data	ADC MAG output to baseband IC, at VDDN logic levels
25	FREF2	Frequency reference select input (bit 2)	Select desired reference / IF / CLK_OUT frequency plan as per “FREF Hardware Configuration” table (Connect to RX_EN or VSSN / GND as required)
26	FREF1	Frequency reference select input (bit 1)	
27	GND	GND connection	Connect to GND
28	XTAL1	Crystal/TCXO connection	If using TCXO reference source: Connect to AC coupled TCXO reference signal If using Crystal reference source: Connect to Crystal input 1 (XTAL1)
29	GND	GND connection	Connect to GND
30	XTAL2	Crystal connection	If using TCXO reference source: Leave unconnected If using Crystal reference source: Connect to Crystal input 2 (XTAL 2)
31	VSSQ	Ground return for quiet digital circuits	Connect to GND
32	VDDQ	Power supply for quiet digital circuits	Connect to VCC
33	VSSCP	Ground return for PLL Charge-Pump	Connect to GND
34	VDDCP	Power supply for PLL Charge-Pump	Connect to VCC
35	VTUNE	VCO tuning voltage input / PLL Charge pump output	Connect to PLL filter network
36	GND	GND connection	Connect to GND
37	GND	GND connection	Connect to GND
38	MIX_IN	Mixer input	DC coupled RF input to RF Mixer
39	OSC_EN	Crystal oscillator enable	If using TCXO reference source (NO crystal oscillator needed): Connect to VSSN / GND If using Crystal reference source, with crystal oscillator: Connect to VDDN
40	GND	GND connection	Connect to GND
41	RVI	Program baseband output drive current	Leave unconnected or Connect to via resistor to analogue VCC for up to 2x output drive current
42	VCC_RF	Analogue power supply for RF blocks	Connect both pads to VCC
43	VCC_RF	Analogue power supply for RF blocks	
44	GND	GND connection	Connect to GND
45	*NC*	*(reserved)*	*Leave unconnected*

Pad	Label	Function	Connection
46	LNA_OUT	LNA RF output	RF output from LNA. DC blocked, with 10 kΩ (nom) DC impedance to ground.

Functional Description

LNA

The internal LNA allows a high-performance, low-power GPS receiver to be completed without using any additional active components.

The GPS L1 input signal which is applied to LNA_IN (pad 4), is a spread-spectrum signal centered on 1575.42 MHz with a 1.023 Mbps BPSK modulation. The signal level at the antenna is typically -130 dBm in open-sky conditions, dropping to below -150 dBm in masked signal areas (e.g. indoors). The LNA noise figure is the largest contributor to the sensitivity so it is an important parameter; the lower, the better.

The LNA input requires a minimum of external matching components to achieve good RF gain with minimal noise figure; only a single series inductor and single shunt capacitor are required. The input requires a DC blocking cap if circuitry prior to the LNA has a DC bias. Although attention should be paid to track lengths and interference throughout the design, the LNA input matching circuit is the only RF circuit critically sensitive to layout.

The LNA output includes internal 50 Ω matching for connection to the mixer input either directly or via an optional external filter.

In applications where the internal LNA is not needed, the LNA can be disabled by connecting VCC_LNA (pad 1) to GND. This will save approximately 1.9 mA of active current.

Mixer RF Input

The mixer RF input, MIX_IN (pad 38), is a single ended 50 Ω input, designed to interface either to LNA_OUT (pad 46) or to the output of an external filter. An external active antenna can also be connected to the mixer input.

The image reject mixer ensures that the receiver's full sensitivity is achieved without an external filter. For applications where additional selectivity is required, an external filter can be added between the LNA_OUT and MIX_IN pads.

IF Filter

The SE4110S includes a fully integrated Intermediate Frequency (IF) filter which provides excellent interference rejection with no additional external components. The filter has a 3rd order Butterworth bandpass response.

The bandpass response has a nominal bandwidth of 2.2 MHz; the nominal center frequency is preset to 4.092 MHz. These parameters ensure very low implementation loss in all frequency plan configurations.

AGC and ADC

The SE4110S features a linear IF chain with 2-bit SIGN / MAG ADC. SIGN is on pad 23, and MAG on pad 24.

An Automatic Gain Control (AGC) system is included. This provides over 40 dB of gain control range so that the output signal level is held at an optimum level at the input of the ADC.

The MAG data controls the AGC loop, such that the MAG bit is active (HIGH) for approximately 33% of the time.

The SIGN and MAG signals are latched by the falling edge of the sample clock, CLK_OUT (pad 22). The SIGN and MAG signals are best sampled by the GPS baseband IC on the rising edge of CLK_OUT, for optimum sample and hold in the ADC.

The AGC time constant is determined by a single external capacitor, connected between VAGC (pad 13), and VSSN / GND. The settling-time of the AGC is within 10 ms with a 10 nF capacitor.

The AGC system also features a control-inhibit facility, via AGC_DIS (pad 15). By connecting AGC_DIS to VDDN, the internal AGC controller is inhibited, and the gain held at the level set prior to the inhibition. While the AGC controller is inhibited, it is possible to control the AGC gain from an external source, by applying a low-impedance voltage to VAGC (pad 13).

PLL and Loop Filter

The entire phase-locked loop (PLL) generating the local oscillator for the mixer is contained on-chip, with the exception of the PLL loop filter.

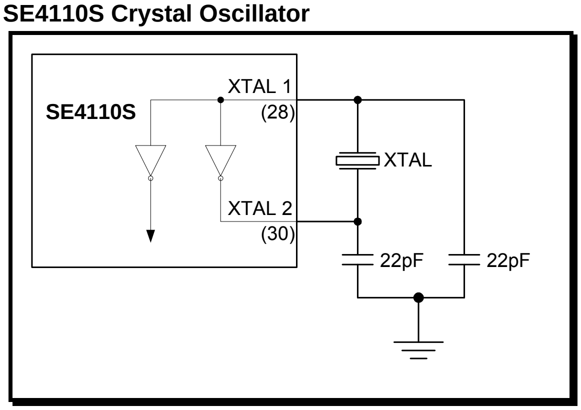
A PLL loop filter can be implemented by attaching a series capacitor (220 pF) and a resistor (33 kΩ) between VTUNE (pad 35) and GND / VSSN. The PLL follows a classic 3^{rd}-order response; this is achieved in conjunction with an on-chip 10 pF capacitor connected between VTUNE and GND / VSSN. Typical PLL Loop Bandwidth is set to be 200 kHz.
The reference frequency for the PLL may be supplied either externally or using the on-chip crystal oscillator.

Crystal Oscillator

The SE4110S features a very low power crystal oscillator which may be used to provide the frequency reference. The oscillator is primarily designed to work with parallel resonant crystals, but can equally be driven from an external TCXO.

The crystal drive level is carefully controlled so that the device is well suited for use with miniature surface mount crystals. The crystal oscillator is a Pierce configuration, as shown in the following diagram. The application circuit is designed to work with parallel resonant crystals with a parallel load capacitance of approx. 10 pF.

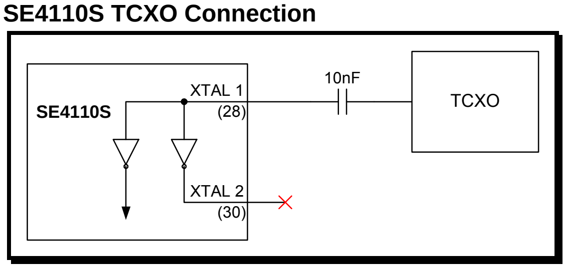
SE4110S Crystal Oscillator



The PCB layout should avoid excessive track length between XTAL1 (pad 28) and XTAL2 (pad 30) and the crystal. The capacitors at each terminal of the crystal should be mounted adjacent to the crystal and have a low impedance connection to the ground plane, in order to maintain the Oscillator Loop Gain and Phase-Noise performance under all conditions.

The SE4110S can also be used with an external TCXO as shown in the following diagram. The TCXO should provide a clipped sinewave signal. The XTAL2 pad should be left unconnected in this configuration.

SE4110S TCXO Connection



Clock and Data Output Coupling

The high input sensitivity achieved by the SE4110S's internal LNA requires careful control of harmonically related sources of interference.

For this reason the CLK_OUT (pad 22), SIGN (pad 23) and MAG (pad 24) outputs provide carefully controlled current and slew-rate. The data and clock outputs of the SE4110S are specified to drive up to 10 pF load (max standard CMOS input capacitance). The output drive of the SE4110S can be adjusted with a resistor, connected between VDDQ (pad 32) and RVI (pad 41), as shown in the Logic Level Characteristics section below.

The output current drive is determined by a bias current ratio internal to the SE4110S and the external resistor.

Frequency Plan Selection

The SE4110S supports operation with a range of reference frequencies, aimed at both 'traditional' GPS and the emerging cellular GPS applications.

The supported frequency plans are tabulated below.

A (+) sign on the IF (output) frequency denotes that the digital signal is not spectrally inverted with respect to the RF input at 1575.42 MHz, as a result of the RF mixer using a low-side Local Oscillator.

A (-) sign indicates that there is a spectral inversion to be taken into account, as a result of the RF mixer using a high-side Local Oscillator.

Supported Frequency Plans

Reference Frequency	Intermediate Frequency (SIGN/MAG pads)	Sample Clock (CLK_OUT pad)
13 MHz	-4.080 MHz	19.5 MHz
16.368 MHz	+4.092 MHz	16.368 MHz
19.5 MHz	-4.080 MHz	19.5 MHz
26 MHz	-4.080 MHz	19.5 MHz

The frequency plan may be configured by connecting the FREF<2:0> inputs (pads 21, 26 and 25) to RX_EN (pad 14) for Logic '1', or VSSN for Logic '0'.

The following truth table gives the settings for hardware configuration.

FREF Hardware Configuration

Reference frequency	Selection value (FREF<2:0>)
16.368 MHz	000
13 MHz	100
19.5 MHz	101
26 MHz	110

Power-up Sequencing

To use the SE4110S device with either FREF0 (pad 21), FREF1 (pad 26) or FREF2 (pad 25) connections set to a logic '1' to enable one of the Hardware Configurations described above, the pins concerned should be connected directly to the signal driving RX_EN (pad 14). The RX_EN signal should be set to VDD levels (logic '1') a short time (>100us) *after* main VCC/VDD power is applied to the SE4110S device.

Power Management

The SE4110S has 3 levels of power control: standby, oscillator only and active. These are controlled by two enable inputs, RX_EN (pad 14) and OSC_EN (pad 39). A table showing the Power Control states follows:

SE4110S Power Control States

RX_EN	OSC_EN	Power state
0	0	Standby
0	1	Oscillator only
1	0	Fully active (external reference)
1	1	Fully active (internal oscillator)

In standby mode all circuits are off and the device consumes only leakage current.

The oscillator-only mode is provided for applications where it is required to keep the sample clock (CLK_OUT (pad 22)) available when active GPS reception is not needed. This feature allows a clock to be maintained with reduced current consumption, but is not available in 13 MHz mode.

There are two settings in the SE4110S Power Control States table for fully active operation depending on whether an external signal or the internal crystal oscillator is used to provide the reference frequency. When using an external reference, approximately 0.4 mA of supply current is saved.

The RX_EN input, (pad 14), has a 1.5 MΩ pull-down resistor to GND, on-chip. This ensures that the RFIC will put itself in standby (or oscillator only mode if OSC_EN is controlled separately) when the RX_EN controller on the baseband is tri-stated to an impedance much greater than 1.5 MΩ.

The internal LNA can be disabled by connecting the Vcc supply connection to the LNA, VCC_LNA (pad 1) to GND. This may be desirable in some applications, and prevents the LNA from consuming any current, saving approximately 1.9 mA.

Logic Interfacing

The SE4110S Logic inputs can either be driven from an external Baseband IC, or permanently set, by connecting to either VDDN (pad 17) for Logic '1', or VSSN (pad 16) for Logic '0'. The digital interface on the SE4110S, supplied from VDDN has been designed to operate at the same voltage as the GPS baseband IC across a wider voltage range than the RF sections of the device. It will accommodate the lower voltage baseband ICs down to 1.7 V. The SE4110S Logic Input signals are shown in the following table:

SE4110S Logic Inputs

Pad	Name	Description	Logic
14	RX_EN	Radio enable	'1' Enable radio '0' Standby mode
15	AGC_DIS	AGC inhibit input	'1' Hold AGC Gain '0' Enable AGC
21	FREF0	Frequency reference select (bit 0)	See table: *"FREF Hardware Configuration"*
26	FREF1	Frequency reference select (bit 1)	
25	FREF2	Frequency reference select (bit 2)	
39	OSC_EN	Crystal oscillator enable	'1' Crystal source with osc enabled '0' TCXO source with osc disabled

Absolute Maximum Ratings

These are stress ratings only. Exposure to stresses beyond these maximum ratings may cause permanent damage to, or affect the reliability of the device. Avoid operating the device outside the recommended operating conditions defined below. This IC can be damaged by electro-static discharges. Handling and assembly of this device should be at ESD protected workstations.

Symbol	Parameter	Note	Min.	Max.	Unit
V_{CC}/V_{DD}	Supply Voltage	1	-0.3	+3.6	V
V_{XSS}	Voltage On Any Pad With Respect To GND	1	-0.3	V_{DD}+0.3	V
LNA_IN_{MAX}	LNA input power	1	-	+3	dBm
ESD	Electrostatic Discharge Immunity (HBM)	1, 2	-	2	kV
T_{STG}	Storage Temperature Range	1	-40	+150	°C
T_{SLDR}	Solder Reflow Temperature	1	-	+250	°C

Note: (1) No damage assuming only one parameter is set at limit at a time with all other parameters set at or below the recommended operating conditions.
(2) ESD checked to the Human Body Model (HBM). A charged 100 pF capacitor discharged through a switch and 1.5k ohm series resistor into the component.

Recommended Operating Conditions

Symbol	Parameter	Note	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-	-40	+85	°C
V_{CC}	Main Supply Voltage	1	2.7	3.6	V
V_{DDN}	Digital I/O Supply Voltage	-	1.7	3.6	V

Note: (1) All supply pads except V_{DDN}.

DC Electrical Characteristics

Conditions: $V_{CC} = V_{DDN} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
I_{CC}	Total Supply Current, All Circuits Active (16.368 MHz reference)	1	-	10	-	mA
	Total Supply Current, All Circuits Active (13, 19.5 & 26 MHz reference)	1	-	10.5	-	mA
$I_{CC(OSC)}$	Total supply Current, Receiver Shut Down, Clock Circuits Only Active (16.368 & 19.5 MHz reference)	2	-	1	-	mA
$I_{CC(OFF)}$	Supply Current, All Circuits Shut Down	-	-	3	10	µA
$I_{CC(LNA)}$	LNA supply Current	-	-	1.9	-	mA

Note: (1) Using on-chip crystal oscillator with SIGN (pad 23), MAG (pad 24) and CLK_OUT (pad 22) outputs unloaded.
(2) Oscillator-only mode unavailable in 13 and 26 MHz reference modes

AC Electrical Characteristics, LNA

Conditions: $V_{CC} = V_{DDN}$ = 3.3 V, T_A = 25 °C, f_{RF} = 1575.42 MHz unless otherwise stated

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
S_{21}	Forward Gain, f_{RF}=1570 MHz to 1580 MHz	-	-	16	-	dB
NF	Noise Figure, f_{RF}=1570 MHz to 1580 MHz	1	-	1.6	-	dB
S_{11}	Input 50 Ω return loss	1	-	5	-	dB
S_{22}	Output 50 Ω return loss, f_{RF}=1570 MHz to 1580 MHz	-	-	14	-	dB
P_{1dB}	1dB Gain Compression	-	-	-30	-	dBm
-	1dB GPS Signal Gain Compression (1575.42MHz) in presence of CW Blocking Signal	-	-	-	-	-
$P_{1dBLNBLK}$	1227.6 MHz (GPS L2) 824 - 849 MHz (GSM850) 880 - 915 MHz (GSM900) 1710 - 1785 MHz (DCS) 1850 - 1910 MHz (PCS) 1920 - 1980 MHz (W-CDMA) 2.4 -2.5 GHz (WLAN/Bluetooth)	2, 3	-	-26.0 -24.0 -23.5 -27.5 -24.0 -23.0 -8.5	-	dBm
t_R	Recovery Time From 0 dBm Input Overload Signal	4	-	1.5	-	µs

Note: (1) With specified input matching network
(2) 1575.42 MHz signal for blocking measurement is CW at a fixed level of -50 dBm
(3) Levels do not include effects of any external RF filtering
(4) LNA has recovered when forward gain (S_{21}) has resettled to achieve its minimum specification limit.

AC Electrical Characteristics, Receiver

Conditions: $V_{CC} = V_{DDN}$ = 3.3 V, T_A = 25 °C, f_{RF} = 1575.42 MHz unless otherwise stated

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
NF	Noise Figure, f_{RF}=1570 MHz To 1580 MHz, Input to 'MIX_IN'	-	-	10	-	dB
S_{11}	Input 50 Ω return loss, f_{RF}=1570 MHz to 1580 MHz	-	-	16	-	dB
f_{IF}	IF Center Frequency, FREF<2:0> = 100 (13 MHz reference)	1	-	-4.080	-	MHz
	IF Center Frequency, FREF<2:0> = 000 (16.368 MHz reference)	1	-	+4.092	-	MHz
	IF Center Frequency, FREF<2:0> = 101 (19.5 MHz reference)	1	-	-4.080	-	MHz
	IF Center Frequency, FREF<2:0> = 110 (26 MHz reference)	1	-	-4.080	-	MHz
M_{IX_IR}	Mixer Image Rejection	2	20	30	-	dB
BW	-3dB Bandwidth	3	-	2.2	-	MHz
A_{RIP}	Amplitude ripple , $f_C \pm$ 512 kHz	-	-	0.5	-	dBpp
ΔT_g	Group Delay Variation, $f_C \pm$ 512 kHz	-	-	60	-	ns
Av_2	Selectivity At $f_C \pm$ 2 MHz	-	-	8	-	dB
Av_4	Selectivity At $f_C \pm$ 4 MHz	-	-	23	-	dB
P_{MAX}	Maximum signal load at MIX_IN (pad 38) (for normal AGC operation)	4	-	-	-137	dBm/Hz
-	1dB GPS Signal Gain Compression (1575.42 MHz) in presence of CW Blocking Signal	-	-	-	-	-
$P_{1dBRXBLK}$	1227.6 MHz (GPS L2) 824 - 849 MHz (GSM850) 880 - 915 MHz (GSM900) 1710 - 1785 MHz (DCS) 1850 - 1910 MHz (PCS) 1920 - 1980MHz (W-CDMA) 2.4 -2.5 GHz (WLAN/Bluetooth)	5, 6	-	-32.0 -35.0 -35.5 -30.5 -29.5 -28.5 -26.0	-	dBm
t_R	Recovery Time From -20 dBm Input Overload Signal	7	-	3	-	µs

Note: (1) Positive IF frequency denotes no spectral inversion, negative frequency has inverted spectrum
(2) Ratio of level through mixer between wanted input signal at 1575.42MHz and image signal at 1567.236MHz.
(3) Centered at IF CF = 4.092 MHz.
(4) The application should be designed to meet this maximum level across 1575.42 ±5 MHz. An absence of strong interferers is assumed.

(5) 1575.42 MHz signal for blocking measurement is CW at a fixed level of -101 dBm.
(6) Levels do not include effects of any external RF filtering.
(7) AGC loop disabled. Receiver is deemed to have recovered when the rms signal level in the ADC has resettled to its initial value ±1.5 dB.

AC Electrical Characteristics, VCO and Local Oscillator

Conditions: $V_{CC} = V_{DDN} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{LO}	LO Centre Frequency (16.368 MHz reference)	1	-	1571.328	-	MHz
	LO Centre Frequency (13, 19.5 & 26 MHz reference)	1	-	1579.5	-	MHz
L_{1k}	LO SSB Phase Noise At 1 kHz Offset	2	-	-86	-	dBc/Hz
L_{10k}	LO SSB Phase Noise At 10 kHz Offset	2	-	-88	-	dBc/Hz
L_{100k}	LO SSB Phase Noise At 100 kHz Offset	2	-	-83	-	dBc/Hz
f_{CLK}	Sample clock output frequency (16.368 MHz reference)	-	-	16.368	-	MHz
	Sample clock output frequency (13, 19.5 & 26 MHz reference)	-	-	19.5	-	MHz

Note: (1) VCO frequency operates at 2x LO frequency.
(2) Typical PLL Loop Bandwidth = 200 kHz

AC Electrical Characteristics, Crystal Oscillator

Conditions: $V_{CC} = V_{DDN} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
f_{XTAL}	Oscillator Frequency	-	13	-	26	MHz
R_X C_{LOAD} P_X	Recommended crystal parameters ESR Load capacitance Drive power specification	1, 2	- - 50	- 22 -	80 - -	Ω pF µW
t_{START}	Oscillator Startup Time To 95 % Of Final Amplitude And Within 10 ppm Of Final Frequency	-	-	2	-	ms
V_{IN}	External oscillator drive level	-	0.2	1	-	V p-p
C_{IN}	External oscillator Input Load Capacitance	3	-	0.5	-	pF

Note: (1) Recommended crystal parameters assume a parallel, fundamental mode crystal is used.
(2) Valid for a 13 MHz crystal.
(3) Connected TCXO to XTAL1 (pad 28) input

Logic Level Characteristics

Conditions: $V_{CC} = V_{DDN} = 3.3$ V, $T_A = 25$ °C

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
V_{IN_H}	Logic High Input Voltage	1	$0.7V_{DDN}$	-	V_{DDN}	V
V_{IN_L}	Logic Low Input Voltage	1	0	-	$0.3V_{DDN}$	V
I_{IN_H}	Input Current Logic High Voltage	1	-	200	-	nA
$I_{IH\_RX\_EN}$	Input Current Logic High Voltage for RX_EN Input (pad 14)	2	-	2.2	-	µA
I_{IN_L}	Input Current Logic Low Voltage	1	-	-200	-	nA
C_{INLOAD}	Input Load Capacitance	1	-	-	2	pF
V_{OUT_H}	Logic High Output Voltage	3	V_{DDN} - 0.1V	-	V_{DDN}	V
V_{OUT_L}	Logic Low Output Voltage	3	0	-	0.1	V
I_{OUT_H}	Output Current Logic High Voltage	3, 4	-	1.45	-	mA
I_{OUT_L}	Output Current Logic Low Voltage	3, 4	-	-1.45	-	mA
$C_{OUTLOAD}$	Output Load Capacitance	3	-	-	10	pF

Note: (1) Applies to all Logic pads used as inputs: AGC_DIS (pad 15), FREF0 (pad 21), FREF1 (pad 26), FREF2 (pad 25), OSC_EN (pad 39), and RX_EN (pad 14).
(2) Applies to RX_EN (pad 14) only. Figure dominated by 1.5 MΩ (nom) on-chip pull-down resistor.
(3) Applies to all Logic pads used as outputs: CLK_OUT (pad 22), SIGN (pad 23), and MAG (pad 24).
(4) Output Current set at Nominal level; no Current Setting Resistor on RVI (pad 41). Positive value indicates current source; negative value indicates current sink.

Logic Output Current Drive Adjustment Settings

The Logic Outputs on the SE4110S can be adjusted to compensate for parasitics in application board layout. This can be achieved by adding a resistor between RVI (pad 41) and VDDQ (pad 32) as shown below.
The additional interface capacitance of PCB tracking and connectors between the SE4110S output and baseband IC input is included in these figures.
These figures are Typical only, and are not guaranteed across temperature and silicon process.

Conditions: $V_{CC} = V_{DD} = 3.3$ V, $T_A = 25$ °C

Current Setting Resistor Value (RVI (pad 41) to VDDQ (pad 32)) (Ω)	**Maximum Allowable Capacitive Loading** (pF)	**Current Drive Level**
Not Fitted	5	Nominal
100K	6	X 1.2
39K	7	X 1.4
0R	10	X 2.0

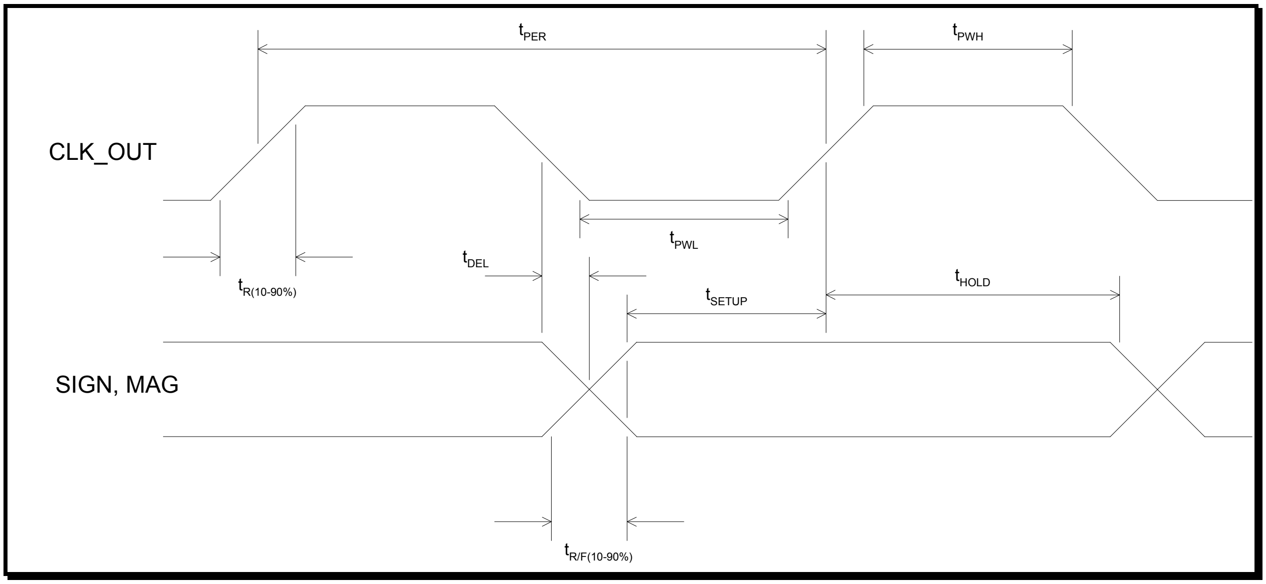
Logic Timing Characteristics

Conditions: $C_L \leq 10$ pF, $V_{CC} = V_{DDN} = 3.3$ V, $T_A = 25$ °C at Maximum Buffer Current

Symbol	Parameter	Note	Min.	Typ.	Max.	Unit
t_{PER}	Clock Period	-	51.2	-	61.1	ns
t_{PWL}	Clock Low Width	1	10	-	-	ns
t_{PWH}	Clock High Width	1	10	-	-	ns
t_{DEL}	Clock To Data Delay Time	2	-	-	12	ns
t_{SETUP}	Setup Time	1	10	-	-	ns
t_{HOLD}	Hold Time	-	10	-	-	ns
t_R	Rise Time, 10-90%	1	-	-	17	ns
$t_{R/F}$	Rise and Fall Time, 10-90%	1	-	-	17	ns

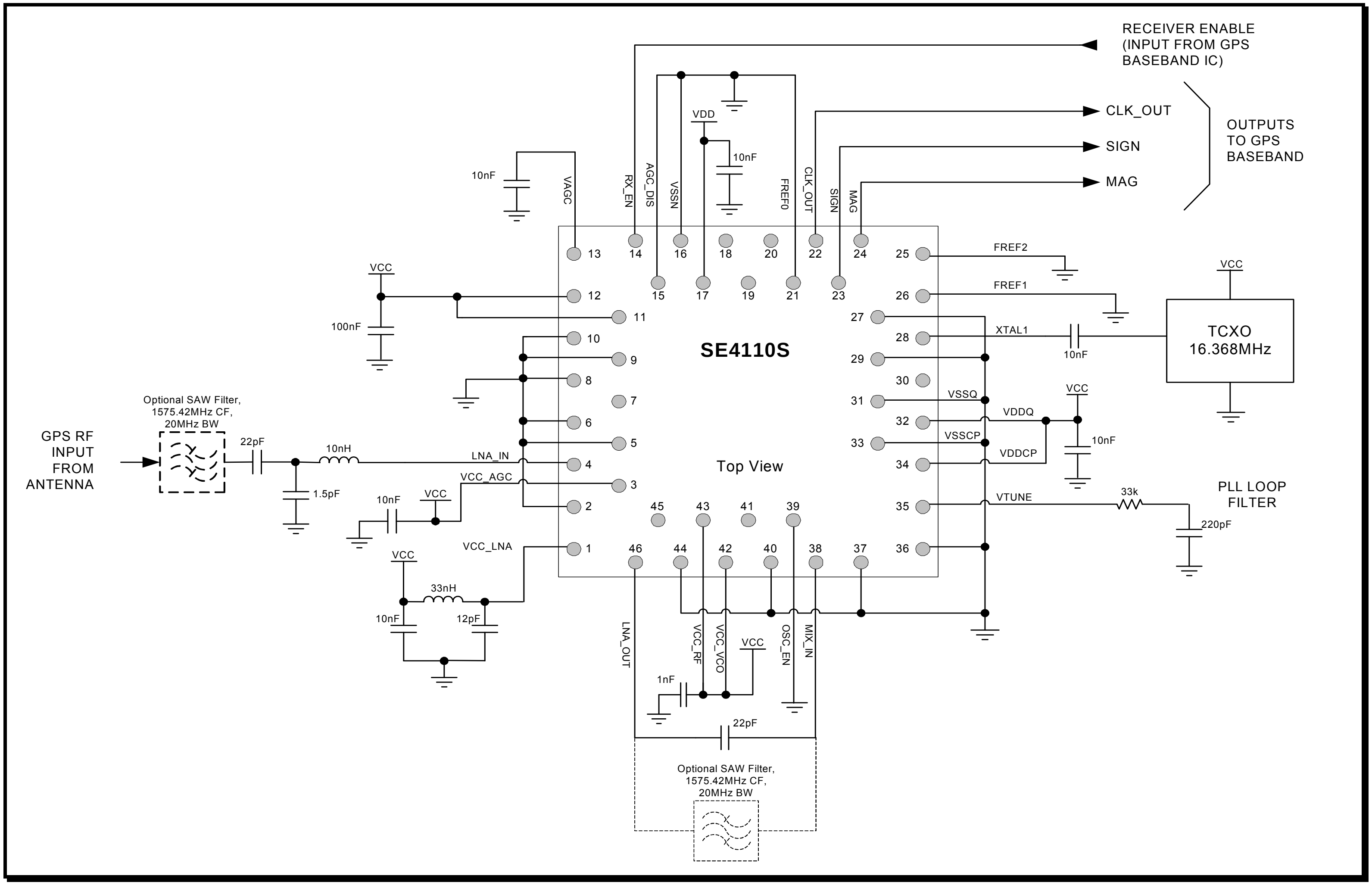
Note: (1) Values dependent on output drive set.
(2) Maximum Values dependent on load capacitance and output drive current level; determined by resistor on RVI (pin 20).

Logic Output Data Timing Diagram

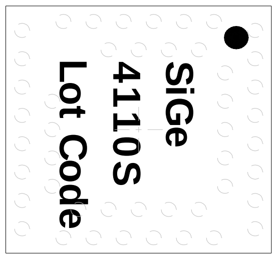


Conditions: $C_L \leq 10$ pF at Maximum Buffer Current

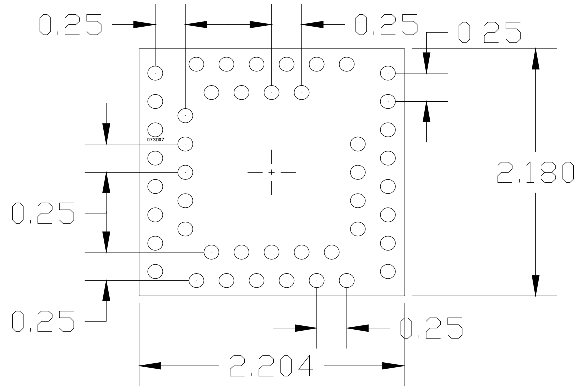
Typical Applications Circuit Diagram



Package Information

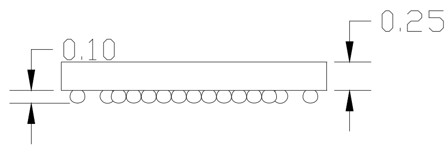


WLCSP MARKING [BOTTOM VIEW]



WLCSP SOLDER BUMPED DIE [TOP VIEW]

WLCSP DIE INFORMATION	
DIE SIZE:	2.204 mm x 2.180 mm
PERIPHERAL PAD:	46 pads
BUMP MATRIX:	2 Rows [46 solder balls]
BUMP MATERIAL:	Lead-Free Solder
BUMP PITCH:	0.25 mm
SOLDER BUMP DIAMETER:	0.10 mm
WAFER BACKGRIND THICKNESS:	0.25 mm
UNDERFILL MATERIAL:	HYSOL 4549



WLCSP SOLDER BUMPED DIE [SIDE VIEW]

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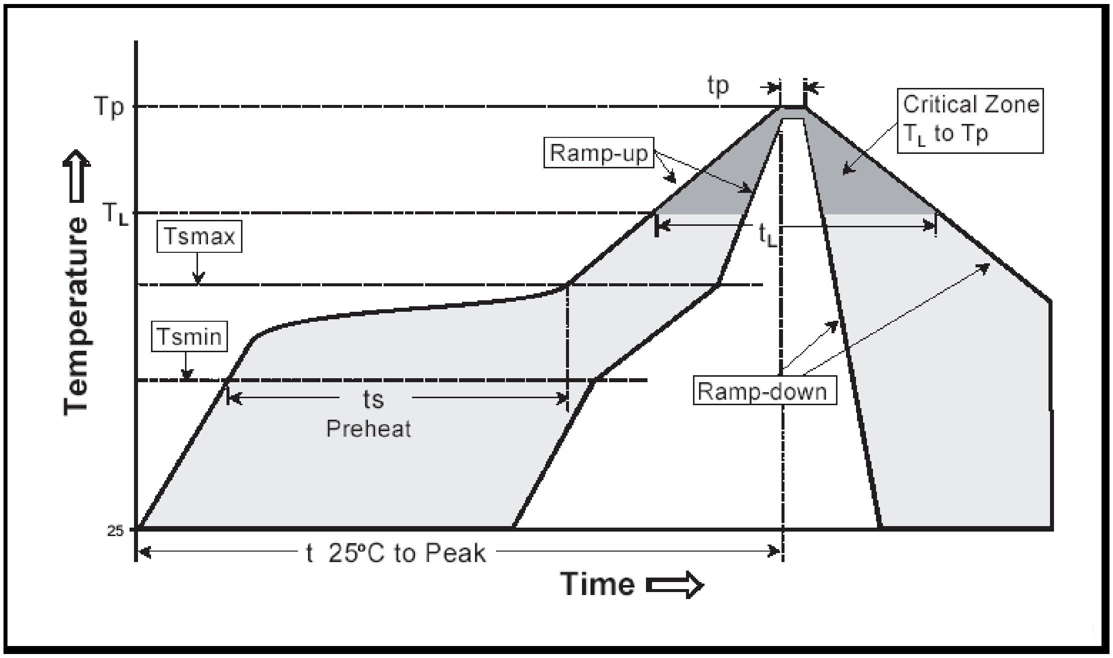
TITLE

SE4110S WLCSP OUTLINE DRAWING & MARKING

Recommended Reflow Temperature Profile

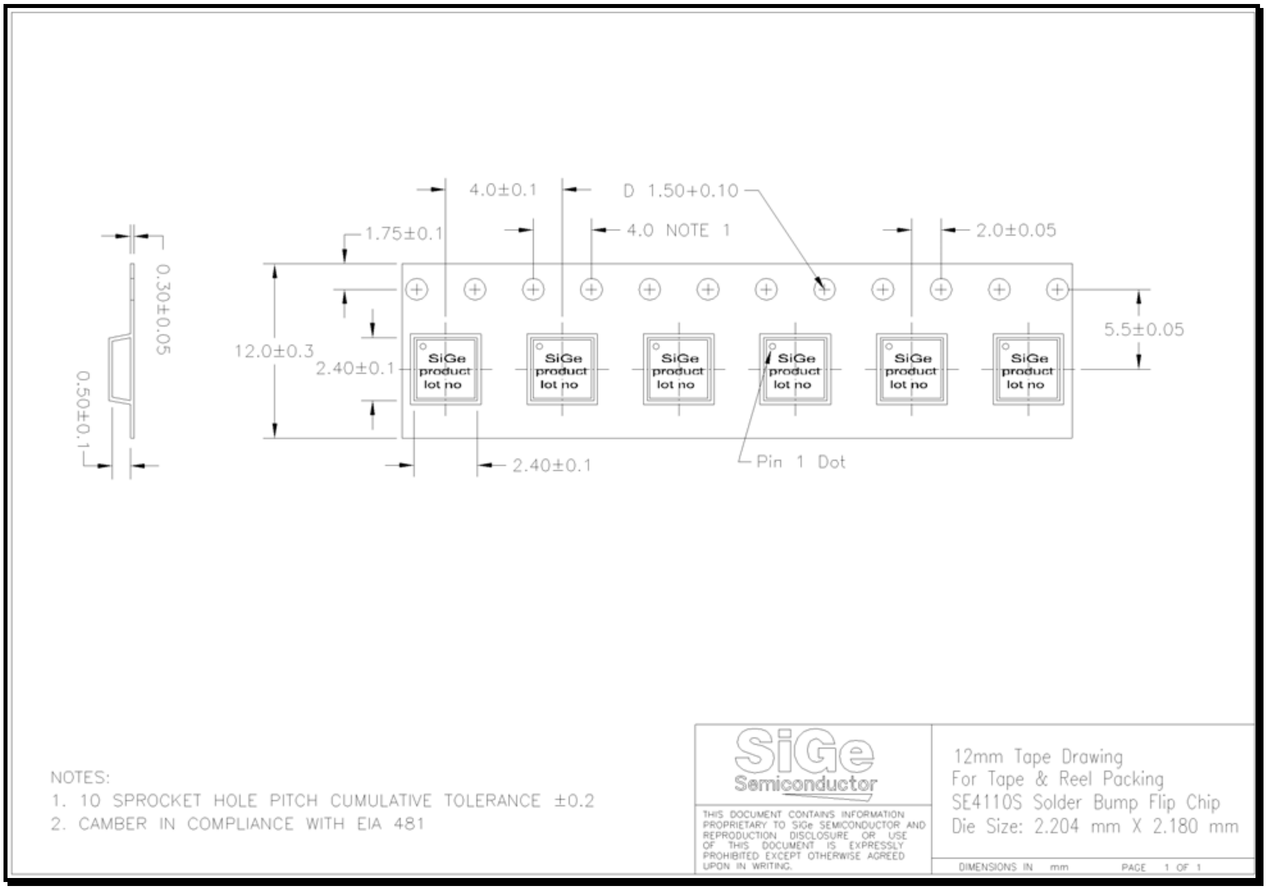
Profile Feature	SnPb Eutectic Assembly	Lead (Pb) Free Assembly
Average ramp-up rate (T_L to T_P)	3 °C/Second Max.	3 °C/Second Max.
Preheat		
Temperature min. (T_{smin})	100 °C	150 °C
Temperature max. (T_{smax})	150 °C	200 °C
Time (min. to max) (t_s)	60-120 s	60-180 s
Ramp Up		
Tsmax to t_L	-	3 °C/s Max.
Time 25 °C to peak temperature	6 Minutes Max.	8 Minutes Max.
Reflow		
Temperature (t_L)	183 °C	217 °C
Time maintained above t_L	60-150 s	60-150 s
Peak temperature (t_p)	240 +/-5 °C	260 +0/-5 °C
Time within 5 °C of actual peak temperature (t_p)	10-30 s	20-40 s
Ramp-Down		
Ramp-down rate	6 °C/s Max.	6 °C/s Max.

Reflow Profile (Reference JEDEC J-STD-020)



Tape and Reel Information

Parameter	Value
Devices per reel	3000
Reel diameter	7 inches
Tape width	12 mm



Underfill Requirements

The assembly of a CSP onto an electrical substrate requires special handling, and will normally need an underfill liquid epoxy mold compound. When fully cured, the underfill material forms a rigid, low stress seal that dissipates stress on solder joints and extends thermal cycling performance. Skyworks Solutions recommends the use of Loctite Hysol 4549 as an underfill material, and this should be cured for 30 minutes at +165° Celcius.

Attaching the CSP without an underfill will make the circuit more susceptible to mechanical damage. This damage can even occur if components in close proximity to the CSP are soldered or unsoldered on the substrate, without evenly preheating the entire board and die, prior to soldering or unsoldering. This can ultimately result in mechanical damage to the solder joint between the board and the die, which may impact electrical connectivity.

Contact Skyworks Solutions for more information.

Pad Coordinates

The SE4110S pad coordinates are shown below.

The origin of the coordinates (i.e. X = 0, Y = 0) is located at the center of the SE4110S package.

Please refer to the Pad Diagram at the front of this datasheet when interpreting the coordinates in the table below.

SE4110S Bump Pad Coordinates

Bump number	Bump Label	Bump coordinates	
		X [µm]	Y [µm]
1	VCC_LNA	-967	875
2	GND	-967	625
3	VCC_AGC	-717	500
4	LNA_IN	-967	375
5	GND	-717	250
6	GND	-967	125
7	*NC*	-717	0
8	GND	-967	-125
9	GND	-717	-250
10	GND	-967	-375
11	VDD_FSE1	-717	-500
12	VDD_FSE2	-967	-625
13	VAGC	-967	-875
14	RX_EN	-625	-954
15	AGC_DIS	-500	-704
16	VSSN	-375	-954
17	VDDN	-250	-704
18	*NC*	-125	-954
19	*NC*	0	-704
20	*NC*	125	-954
21	FREF0	250	-704
22	CLK_OUT	375	-954
23	SIGN	500	-704
24	MAG	625	-954

Bump number	Bump Label	Bump coordinates	
		X [µm]	Y [µm]
25	FREF2	967	-875
26	FREF1	967	-625
27	GND	717	-500
28	XTAL1	967	-375
29	GND	717	-250
30	XTAL2	967	-125
31	VSSQ	717	0
32	VDDQ	967	125
33	VSSCP	717	250
34	VDDCP	967	375
35	VTUNE	967	625
36	GND	967	875
37	GND	625	954
38	MIX_IN	375	954
39	OSC_EN	250	704
40	GND	125	954
41	RVI	0	704
42	VCC_RF	-125	954
43	VCC_RF	-250	704
44	GND	-375	954
45	*NC*	-500	704
46	LNA_OUT	-625	954

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