1.8 V to 5.5 V, 4 Ω Dual SPST Switches

DESCRIPTION

The DG721, DG722 and DG723 are precision dual SPST switches designed to operate from single 1.8 V to 5.5 V power supply with low power dissipation. The DG721, DG722 and DG723 can switch both analog and digital signals within the power supply rail, and conduct well in both directions.

Fabricated with advance submicron CMOS process, these switches provide high precision low and flat ON resistance, low leakage current, low parasitic capacitance, and low charge injection.

The DG721, DG722 and DG723 contain two independent Single Pole Single Throw (SPST) switches. Switch-1 and switch-2 are normally open for the DG721 and normally closed for the DG722. For the DG723, switch-1 is normally open and switch-2 is normally closed with a Break-Before-Make switching timing.

The DG721, DG722 and DG723 are the ideal switches for use in low voltage instruments and healthcare devices, fitting the circuits of low voltage ADC and DAC, analog front end gain control, and signal path control.

As a committed partner to the community and the environment, Vishay Siliconix manufactures this product with lead (Pb)-free device termination. The TDFN8 package has a nickel-palladium-gold device termination and is represented by the lead (Pb)-free “-E4” suffix to the ordering part number. The MSOP-8 package has tin device termination and is represented by “-E3”. Both device terminations meet all JEDEC standards for reflow and MSL rating.

As a further sign of Vishay Siliconix's commitment, the DG721, DG722 and D723 are fully RoHS compliant and Halogen-free.

FEATURES

- **Halogen-free according to IEC 61249-2-21 definition**
- 1.8 V to 5.5 V single power supply
- Low and flat switch on resistance, 2.5 Ω/typ.
- Low leakage and parasitic capacitance
- 366 MHz, - 3 dB bandwidth
- Latch-up current > 300 mA (JESD78)
- Space saving packages
  2 mm x 2 mm TDFN8
  MSOP8
- Over voltage tolerant TTL/CMOS compatible
- **Compliant to RoHS Directive 2002/95/EC**

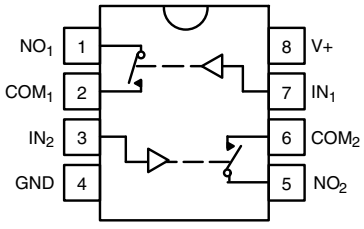
Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Healthcare and medical devices
- Test instruments
- Portable meters
- Data acquisitions
- Control and automation
- PDAs and modems
- Communication systems
- Audio, video systems
- Mechanical reed relay replacement

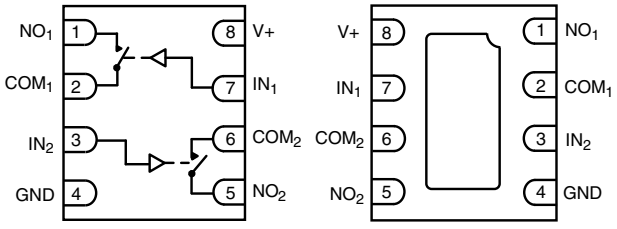
FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION

DG721, MSOP-8

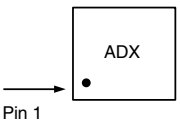


Top View

DG721, TDFN-8



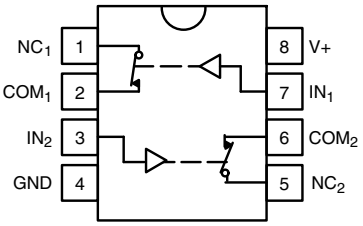
Top View | Bottom View



Device Marking for TDFN-8: for DG721
x = Date/Lot Traceability Code

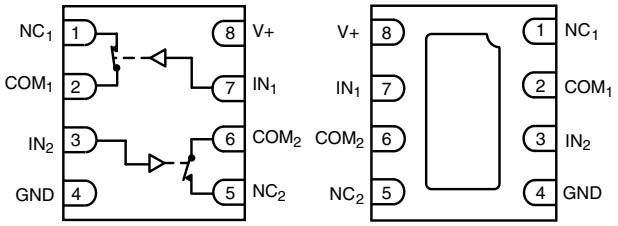
Device Marking for MSOP-8: 721

DG722, MSOP-8

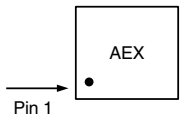


Top View

DG722, TDFN-8



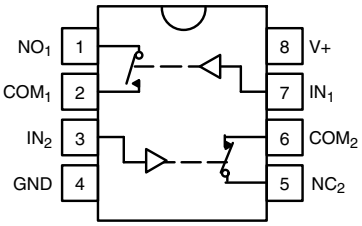
Top View | Bottom View



Device Marking for TDFN-8: for DG722
x = Date/Lot Traceability Code

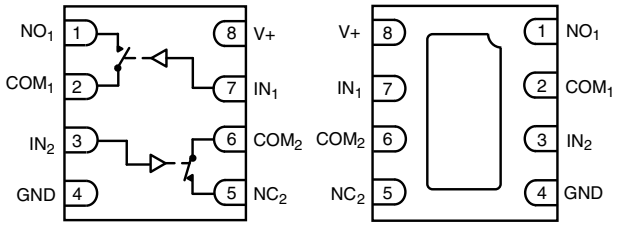
Device Marking for MSOP-8: 722

DG723, MSOP-8

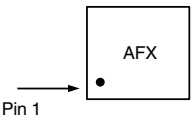


Top View

DG723, TDFN-8



Top View | Bottom View



Device Marking for TDFN-8: for DG723
x = Date/Lot Traceability Code

Device Marking for MSOP-8: 723

TRUTH TABLE (DG721, DG722)			
	DG721	**DG722**	**Switches**
Logic	0	1	Off
	1	0	On

TRUTH TABLE (DG723)		
Logic	**Switch-1**	**Switch-2**
0	Off	On
1	On	Off

ORDERING INFORMATION		
Temperature Range	**Package**	**Part Number**
- 40 °C to 85 °C	MSOP-8	DG721DQ-T1-GE3
		DG722DQ-T1-GE3
		DG723DQ-T1-GE3
	TDFN-8	DG721DN-T1-GE4
		DG722DN-T1-GE4
		DG723DN-T1-GE4

ABSOLUTE MAXIMUM RATINGS			
Parameter		**Limit**	**Unit**
Referenced V+ to GND		- 0.3 to 6	V
IN, COM, NC, NO[a]		- 0.3 to (V+ + 0.3)	
Continuous Current (Any Terminal)		± 50	mA
Peak Current (Pulsed at 1 ms, 10 % duty cycle)		± 200	
Storage Temperature (D Suffix)		- 65 to 150	°C
Power Dissipation (Packages)[b]	MSOP-8[c]	320	mW
	TDFN-8[d]	842	

Notes:
a. Signals on NC, NO, or COM or IN exceeding V+ will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads welded or soldered to PC board.
c. Derate 4 mW/°C above 70 °C.
d. Derate 10.53 mW/°C above 70 °C.

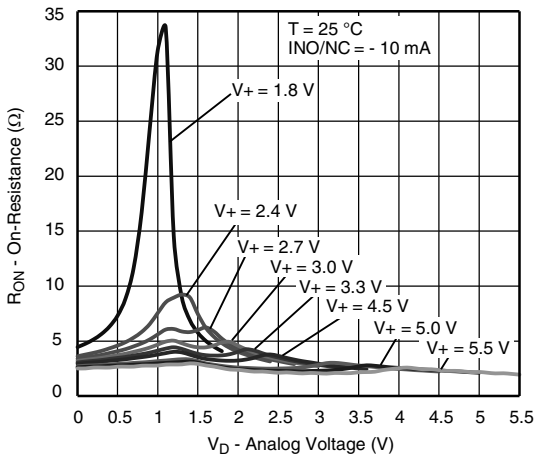
SPECIFICATIONS (V+ = 3 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 3 V, ± 10 %, V_{IN} = 0.4 or 1.5 V[e]	**Temp.[a]**	**Limits** - 40 °C to 85 °C **Min.[b]**	**Typ.[c]**	**Max.[b]**	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 2.7 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = - 10 mA	Room Full		6.5	 10	Ω
R_{ON} Flatness[d]	R_{ON} Flatness	V+ = 2.7 V, V_{COM} = 1.1 V to 1.6 V, I_{NO}, I_{NC} = - 10 mA	Room		0.4		
R_{ON} Match[d]	R_{ON} Match	V+ = 2.7 V, V_D = 1.1 V to 1.6 V, I_D = - 10 mA	Room Full		0.3	 0.9	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 3.3 V V_{NO}, V_{NC} = 1 V/3 V, V_{COM} = 3 V/1 V	Room Full	- 0.25 - 0.35		0.25 0.35	nA
	$I_{COM(off)}$		Room Full	- 0.25 - 0.35		0.25 0.35	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 3.3 V, V_{NO}, V_{NC} = V_{COM} = 1 V/3 V	Room Full	- 0.25 - 0.35		0.25 0.35	
Digital Control							
Input High Voltage	V_{INH}		Full	2			V
Input Low Voltage	V_{INL}		Full			0.4	
Input Capacitance[d]	C_{in}	f = 1 MHz	Full		2.4		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 1		1	µA
Dynamic Characteristics							
Turn-On Time	t_{ON}	V_{NO} or V_{NC} = 2 V, R_L = 300 Ω, C_L = 35 pF figures 1 and 2	Room Full		16	 55	ns
Turn-Off Time	t_{OFF}		Room Full		7	 40	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, figure 3	Room		1.8		pC
Bandwidth[d]	BW	V+ = 3 V, R_L = 50 Ω, C_L = 5 pF, - 3dB	Room		319		MHz
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 67		dB
Crosstalk[d]	X_{TALK}		Room		- 92		
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room		- 47		
Crosstalk[d]	X_{TALK}		Room		- 90		
Source-Off Capacitance[d]	$C_{NC/NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		8		pF
Drain-Off Capacitance[d]	$C_{COM(off)}$		Room		9		
Channel-On Capacitance[d]	C_{ON}		Room		22		
Power Supply							
Power Supply Current	I+	V_{IN} = 0 or V+, V+ = 3.3 V				1	µA

SPECIFICATIONS (V+ = 5 V)							
Parameter	**Symbol**	**Test Conditions Otherwise Unless Specified** V+ = 5 V, ± 10 %, V_{IN} = 0.8 or 2.4 V[e]	**Temp.[a]**	**Limits - 40 °C to 85 °C** Min.[b]	Typ.[c]	Max.[b]	**Unit**
Analog Switch							
Analog Signal Range[d]	V_{NO}, V_{NC} V_{COM}		Full	0		V+	V
On-Resistance	R_{ON}	V+ = 4.5 V, V_{COM} = 0 V to V+, I_{NO}, I_{NC} = 10 mA	Room Full		2.5	4.5 5	Ω
R_{ON} Flatness[d]	R_{ON} Flatness	V+ = 4.5 V, V_{COM} = 1.3 V to 3 V, I_{NO}, I_{NC} = 10 mA	Room		0.75	1.5	
R_{ON} Match[d]	R_{ON} Match	V+ = 4.5 V, I_D = 10 mA, V_{COM} = 1.3 V to 3 V	Room		0.2	0.9	
Switch Off Leakage Current	$I_{NO(off)}$ $I_{NC(off)}$	V+ = 5.5 V V_{NO}, V_{NC} = 1 V/4.5 V, V_{COM} = 4.5 V/1 V	Room Full	- 0.25 - 0.35		0.25 0.35	nA
	$I_{COM(off)}$		Room Full	- 0.25 - 0.35		0.25 0.35	
Channel-On Leakage Current	$I_{COM(on)}$	V+ = 5.5 V V_{NO}, V_{NC} = V_{COM} = 1 V/4.5 V	Room Full	- 0.25 - 0.35		0.25 0.35	
Digital Control							
Input High Voltage	V_{INH}		Full	2.4			V
Input Low Voltage	V_{INL}		Full			0.8	
Input Capacitance	C_{in}	f = 1 MHz	Full		2.2		pF
Input Current	I_{INL} or I_{INH}	V_{IN} = 0 or V+	Full	- 0.1	0.005	0.1	µA
Dynamic Characteristics							
Turn-On Time[d]	t_{ON}	V_{NO} or V_{NC} = 3 V, R_L = 300 Ω, C_L = 35 pF figures 1 and 2	Room Full		17	30 40	ns
Turn-Off Time[d]	t_{OFF}		Room Full		9	35	
Charge Injection[d]	Q_{INJ}	C_L = 1 nF, V_{GEN} = 0 V, R_{GEN} = 0 Ω, figure 3	Room		2.2		pC
Bandwidth[d]	BW	V+ = 5 V, R_L = 50 Ω, C_L = 5 pF, - 3 dB	Room		366		MHz
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz	Room		- 67		dB
Crosstalk[d]	X_{TALK}		Room		- 90		
Off-Isolation[d]	OIRR	R_L = 50 Ω, C_L = 5 pF, f = 10 MHz	Room		- 47		
Crosstalk[d]	X_{TALK}		Room		- 90		
Source-Off Capacitance[d]	$C_{NC/NO(off)}$	V_{IN} = 0 or V+, f = 1 MHz	Room		8		pF
Drain-Off Capacitance[d]	$C_{COM(off)}$		Room		9		
Channel-On Capacitance[d]	C_{ON}		Room		22		
Power Supply							
Power Supply Range	V+			1.8		5.5	V
Power Supply Current	I+	V_{IN} = 0 or V+, V+ = 5.5 V	Full			2	µA

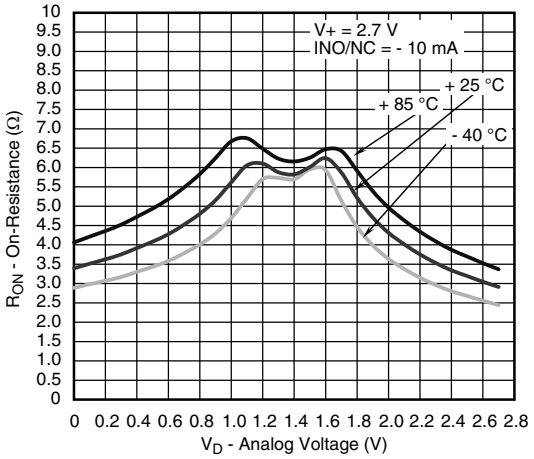
Notes:
a. Room = 25 °C, Full = as determined by the operating suffix.
b. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
c. Typical values are for design aid only, not guaranteed nor subject to production testing.
d. Guarantee by design, nor subjected to production test.
e. V_{IN} = input voltage to perform proper function.
f. Not production tested.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

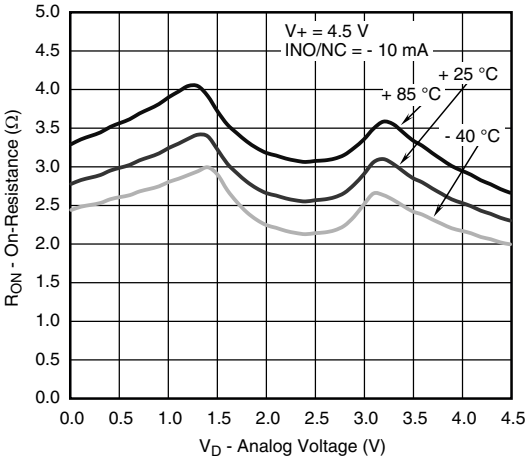
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



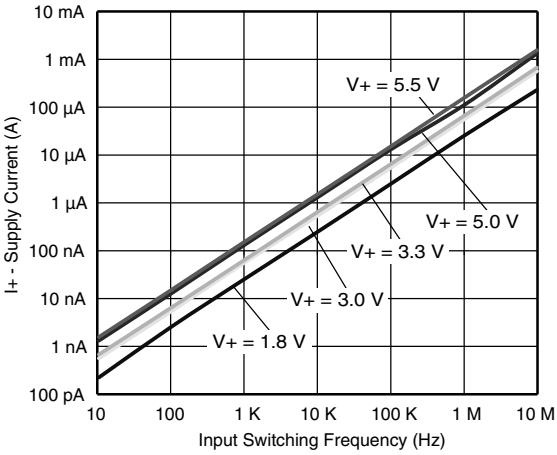
R_{ON} vs. V_D and Single Supply Voltage



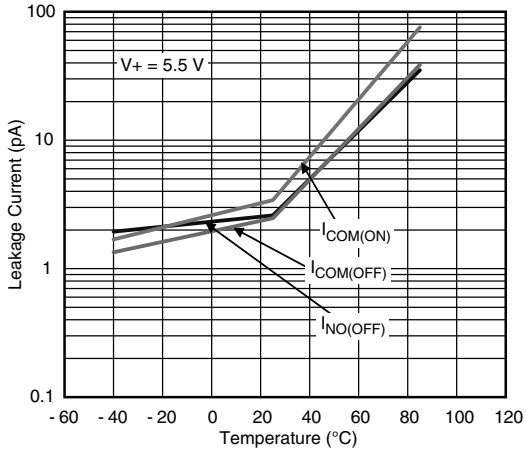
R_{ON} vs. Analog Voltage and Temperature



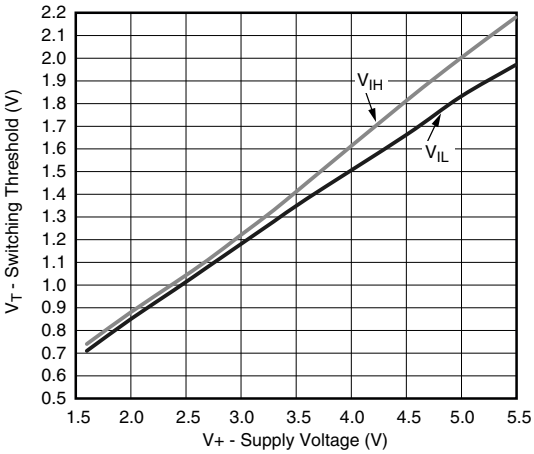
R_{ON} vs. Analog Voltage and Temperature



Supply Current vs. Input Switching Frequency

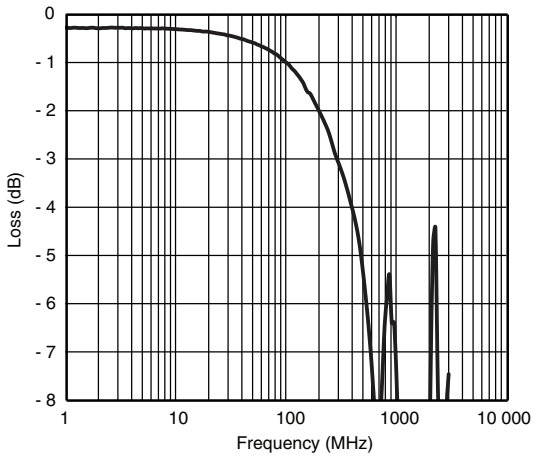


Leakage Current vs. Temperature

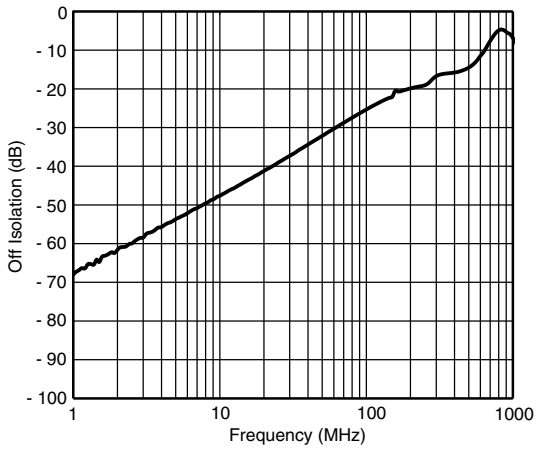


Switching Threshold vs. Supply Voltage

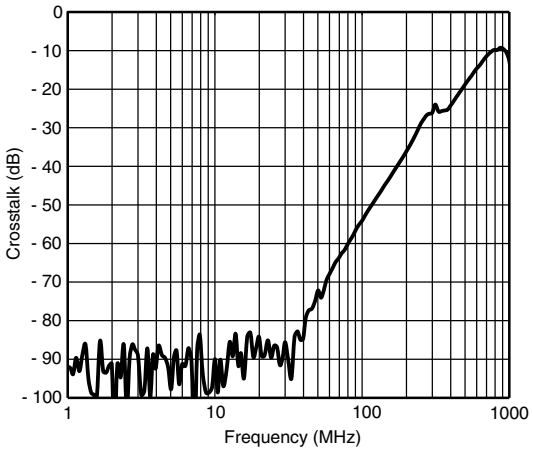
TYPICAL CHARACTERISTICS (T_A = 25 °C, unless otherwise noted)



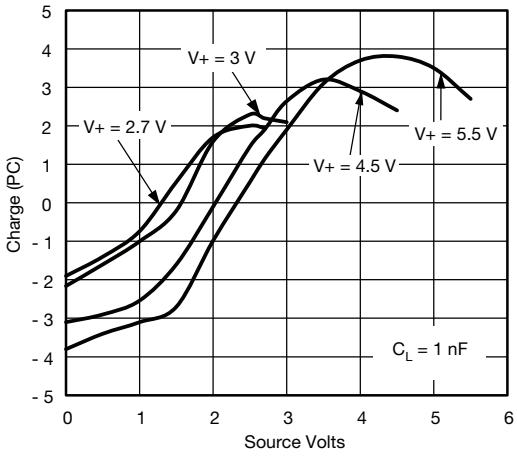
Insertion Loss vs. Frequency



Off Isolation vs. Frequency

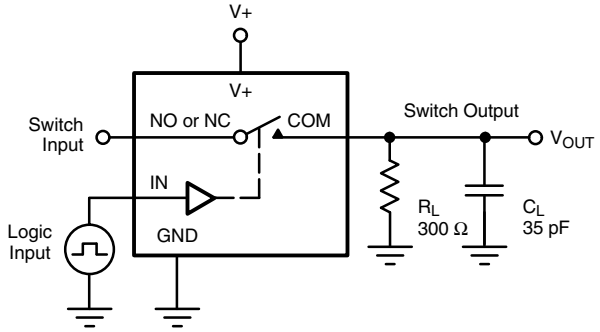


Crosstalk vs. Frequency



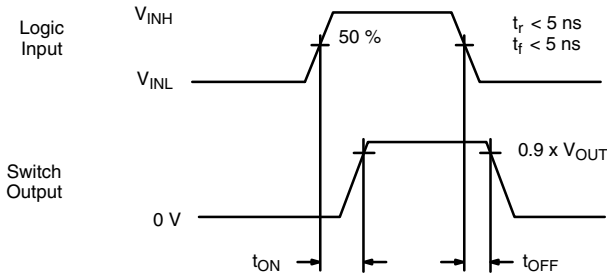
Charge Injection vs. Analog Voltage

TEST CIRCUITS



C_L (includes fixture and stray capacitance)

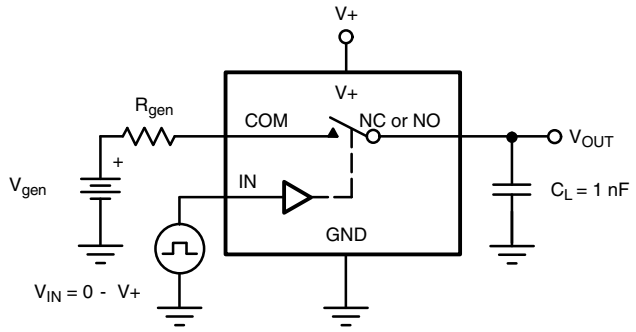
$$V_{OUT} = V_{COM}\left(\frac{R_L}{R_L + R_{ON}}\right)$$

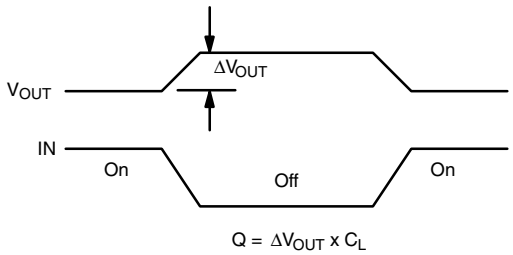


Logic "1" = Switch On
Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 1. Switching Time

TEST CIRCUITS





IN depends on switch configuration: input polarity determined by sense of switch.

Figure 2. Charge Injection

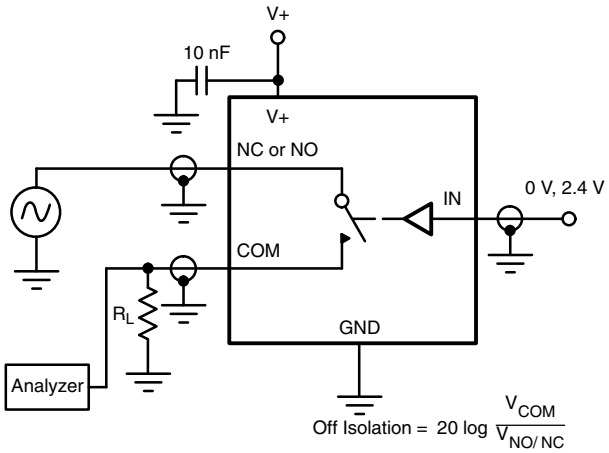


Figure 3. Off-Isolation

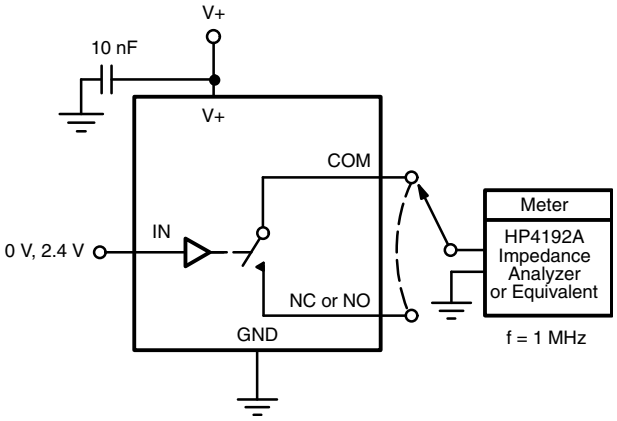


Figure 4. Channel Off/On Capacitance

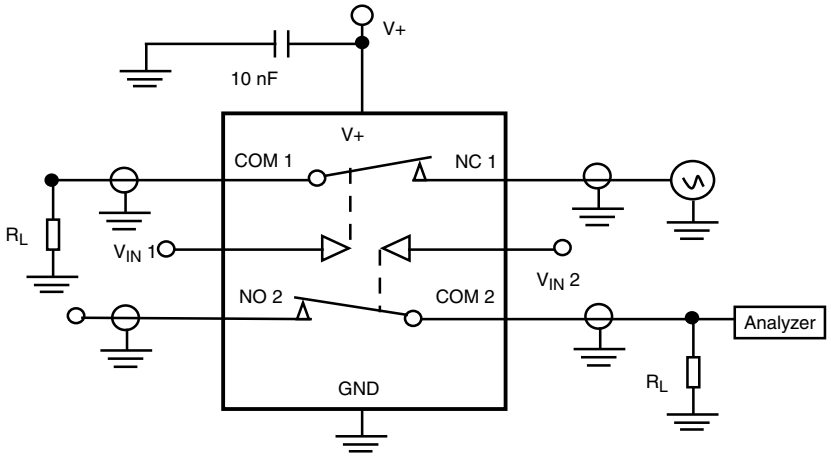
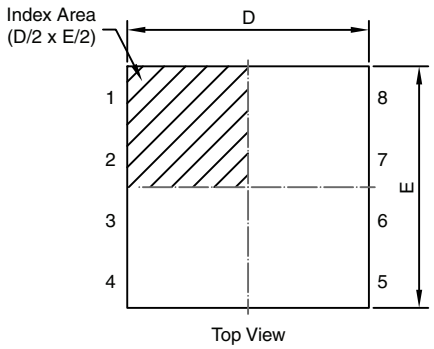
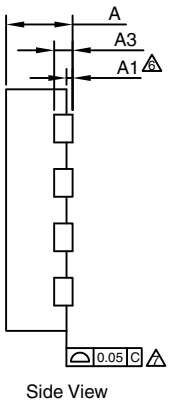


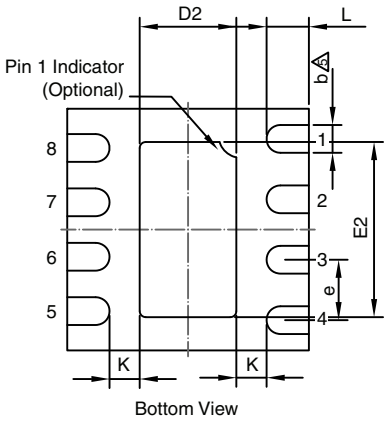
Figure 5. Channel to Channel Crosstalk

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?66586.

CASE OUTLINE FOR TDFN8 2 x 2







DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.152 REF			0.006 REF		
b	0.18	0.23	0.28	0.007	0.009	0.011
D	1.95	2.00	2.05	0.077	0.079	0.081
D2	0.75	0.80	0.85	0.030	0.031	0.033
e	0.50 BSC			0.020 BSC		
E	1.95	2.00	2.05	0.077	0.079	0.081
E2	1.40	1.45	1.50	0.055	0.057	0.059
K	-	0.20	-	-	0.008	-
L	0.30	0.35	0.40	0.012	0.014	0.016
ECN: C11-0033 Rev. A, 07-Feb-11 DWG: 5997						

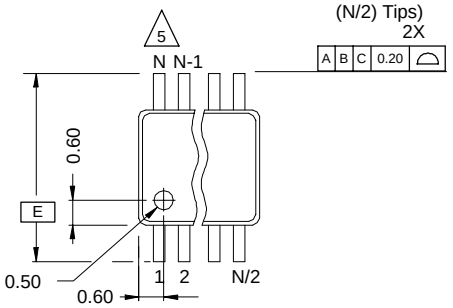
Note

1. All dimensions are in millimeters which will govern.
2. Max. package warpage is 0.05 mm.
3. Max. allowable burrs is 0.076 mm in all directions.
4. Pin #1 ID on top will be laser/ink marked.

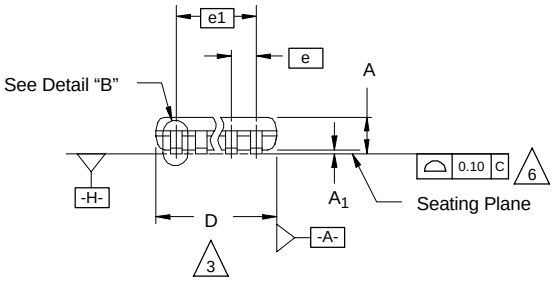
5. Dimension applies to meatlized terminal and is measured between 0.20 mm and 0.25 mm from terminal tip.
6. Applied only for terminals.
7. Applied for exposed pad and terminals.

MSOP: 8-LEADS

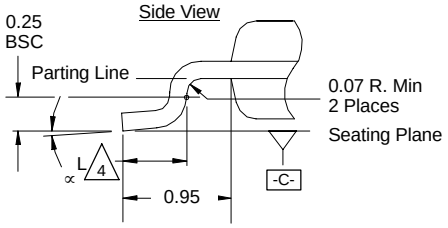
JEDEC Part Number: MO-187, (Variation AA and BA)



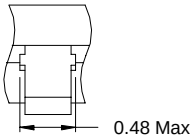
Top View



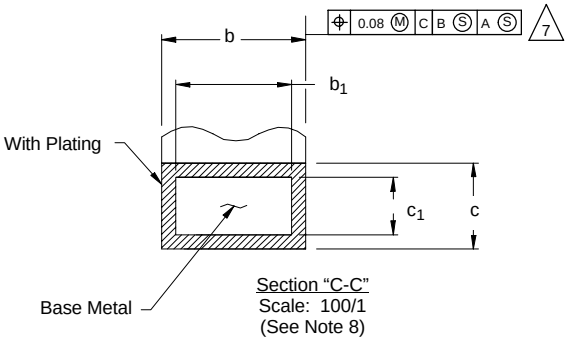
Side View



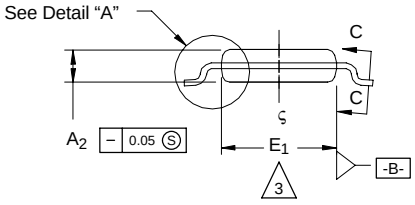
Detail "A"
(Scale: 30/1)



Detail "B"
(Scale: 30/1)
Dambar Protrusion



Section "C-C"
Scale: 100/1
(See Note 8)



End View

NOTES:

1. Die thickness allowable is 0.203 ± 0.0127.
2. Dimensioning and tolerances per ANSI.Y14.5M-1994.
3. Dimensions "D" and "E_1" do not include mold flash or protrusions, and are measured at Datum plane -H- , mold flash or protrusions shall not exceed 0.15 mm per side.
4. Dimension is the length of terminal for soldering to a substrate.
5. Terminal positions are shown for reference only.
6. Formed leads shall be planar with respect to one another within 0.10 mm at seating plane.
7. The lead width dimension does not include Dambar protrusion. Allowable Dambar protrusion shall be 0.08 mm total in excess of the lead width dimension at maximum material condition. Dambar cannot be located on the lower radius or the lead foot. Minimum space between protrusions and an adjacent lead to be 0.14 mm. See detail "B" and Section "C-C".
8. Section "C-C" to be determined at 0.10 mm to 0.25 mm from the lead tip.
9. Controlling dimension: millimeters.
10. This part is compliant with JEDEC registration MO-187, variation AA and BA.
11. Datums -A- and -B- to be determined Datum plane -H- .
12. Exposed pad area in bottom side is the same as teh leadframe pad size.

N = 8L

Dim	MILLIMETERS			Note
	Min	Nom	Max	
A	-	-	1.10	
A_1	0.05	0.10	0.15	
A_2	0.75	0.85	0.95	
b	0.25	-	0.38	8
b_1	0.25	0.30	0.33	8
c	0.13	-	0.23	
c_1	0.13	0.15	0.18	
D	3.00 BSC			3
E	4.90 BSC			
E_1	2.90	3.00	3.10	3
e	0.65 BSC			
e_1	1.95 BSC			
L	0.40	0.55	0.70	4
N	8			5
∝	0°	4°	6°	

ECN: T-02080—Rev. C, 15-Jul-02
DWG: 5867

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