N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A)
28	0.033 at V_{GS} = 4.5 V	4.6
	0.038 at V_{GS} = 3.0 V	4.3
	0.042 at V_{GS} = 2.5 V	4.1

FEATURES

- **Halogen-free**
- Low $R_{DS(on)}$
- V_{GS} Max Rating: 14 V
- Exceeds 2 kV ESD Protection
- 28 V V_{DS} Rated
- Symmetrical Voltage Blocking (Off Voltage)

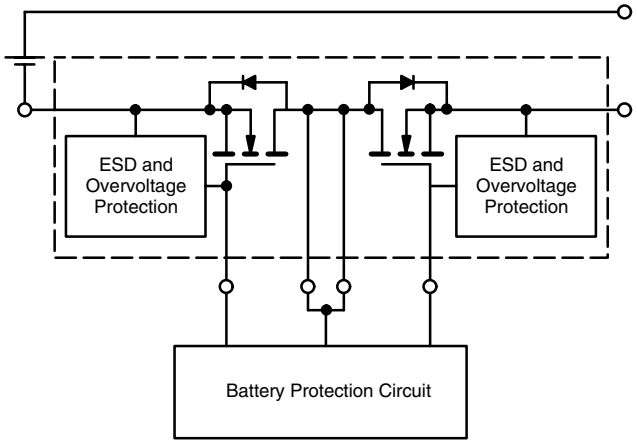
Pb-free

RoHS
COMPLIANT

DESCRIPTION

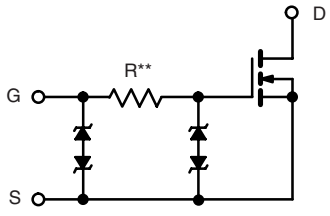
The Si6924AEDQ is a dual N-Channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The common-drain construction takes advantage of the typical battery pack topology, allowing a further reduction of the device's on-resistance. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second stage diode is designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to ≤ 10 mA at 14 V and the maximum t_{off} to 12 µs. The Si6924AEDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5 V $R_{DS(on)}$ rating and a safe 14 V gate-to-source maximum rating.

APPLICATION CIRCUITS



*Thermal connection to drain pins is required to achieve specific performance

Figure 1. Typical Use In a Lithium Ion Battery Pack

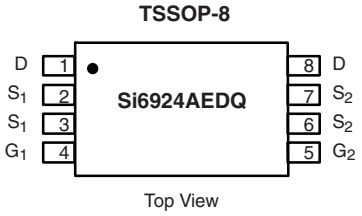


**R typical value is 3.3 kΩ by design.

See Typical Characteristics,
Gate-Current vs. Gate-Source Voltage, Page 3.

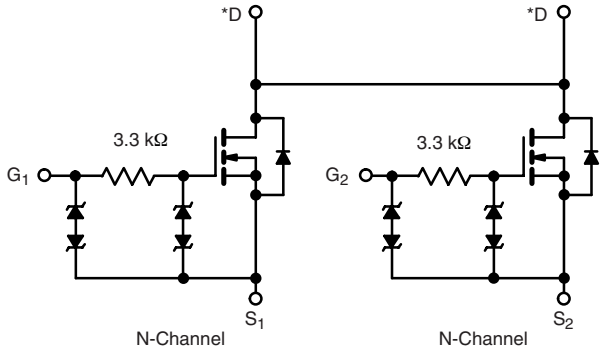
Figure 2. Input ESD and Overvoltage Protection Circuit

FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION



Ordering Information: Si6924AEDQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

Figure 3.



*Thermal connection to drain pins is required to achieve specific performance.

Figure 4.

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted					
Parameter		**Symbol**	**10 s**	**Steady State**	**Unit**
Drain-Source Voltage, Source-Drain Voltage		V_{DS}	28		V
Gate-Source Voltage		V_{GS}	± 14		
Continuous Drain-to-Source Current (T_J = 150 °C)[a]	T_A = 25 °C	I_D	4.6	4.1	A
	T_A = 70 °C		3.7	3.2	
Pulsed Drain-to-Source Current		I_{DM}	20		
Pulsed Source Current (Diode Conduction)[a]		I_S	1.2	0.9	
Maximum Power Dissipation[a]	T_A = 25 °C	P_D	1.3	1.0	W
	T_A = 70 °C		0.84	0.64	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		**Symbol**	**Typical**	**Maximum**	**Unit**
Maximum Junction-to-Ambient[a]	t ≤ 10 s	R_{thJA}	71	95	°C/W
	Steady State		96	125	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	56	70	

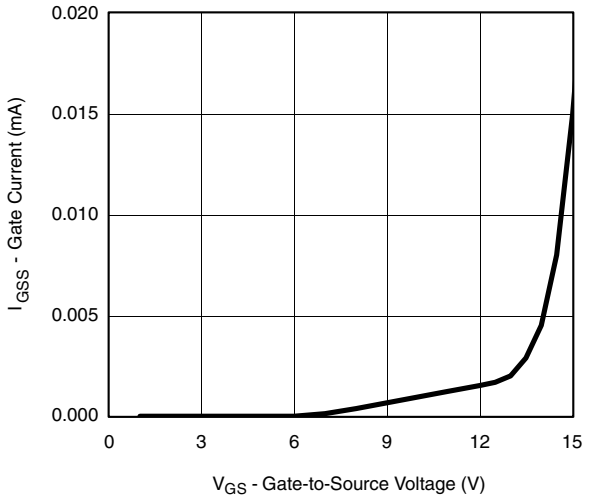
Notes:
a. Surface Mounted on FR4 board.

SPECIFICATIONS T_J = 25 °C, unless otherwise noted						
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250$ µA	0.6		1.5	V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = \pm 4.5$ V			± 1	µA
		$V_{DS} = 0$ V, $V_{GS} = \pm 14$ V			± 20	mA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 22.4$ V, $V_{GS} = 0$ V			1	µA
		$V_{DS} = 22.4$ V, $V_{GS} = 0$ V, $T_J = 55$ °C			5	
On-State Drain Current[b]	$I_{D(on)}$	$V_{DS} \geq 5$ V, $V_{GS} = 5$ V	10			A
Drain-Source On-State Resistance[b]	$R_{DS(on)}$	$V_{GS} = 4.5$ V, $I_D = 4.6$ A		0.022	0.033	Ω
		$V_{GS} = 3.0$ V, $I_D = 4.3$ A		0.025	0.038	
		$V_{GS} = 2.5$ V, $I_D = 4.1$ A		0.029	0.042	
Forward Transconductance[b]	g_{fs}	$V_{DS} = 10$ V, $I_D = 4.6$ A		25		S
Diode Forward Voltage[b]	V_{SD}	$I_S = 1.2$ A, $V_{GS} = 0$ V		0.7	1.1	V
Dynamic[a]						
Total Gate Charge	Q_g	$V_{DS} = 10$ V, $V_{GS} = 4.5$ V, $I_D = 4.6$ A		6.5	10	nC
Gate-Source Charge	Q_{gs}			1.2		
Gate-Drain Charge	Q_{gd}			1.5		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 10$ V, $R_L = 10$ Ω $I_D \cong 1$ A, $V_{GEN} = 4.5$ V, $R_G = 6$ Ω		0.95	1.5	µs
Rise Time	t_r			1.4	2.1	
Turn-Off Delay Time	$t_{d(off)}$			7	11	
Fall Time	t_f			3.1	5	

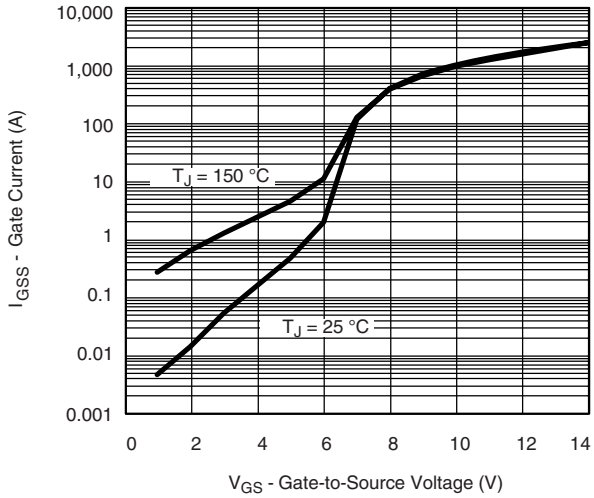
Notes:
a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

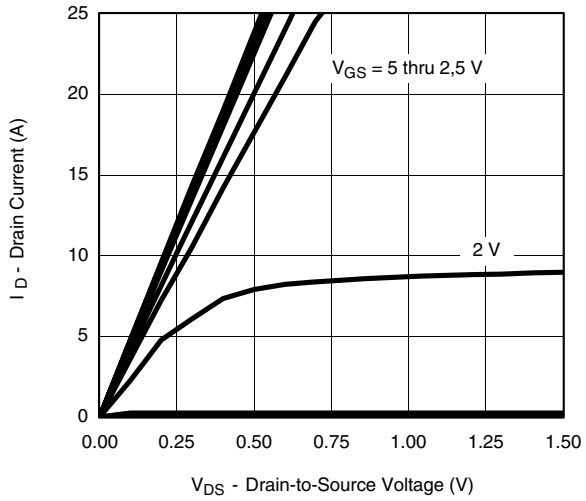


Gate-Current vs. Gate-Source Voltage

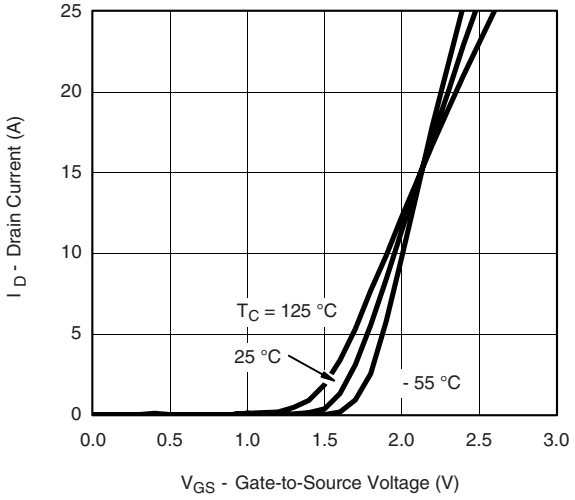


Gate Current vs. Gate-Source Voltage

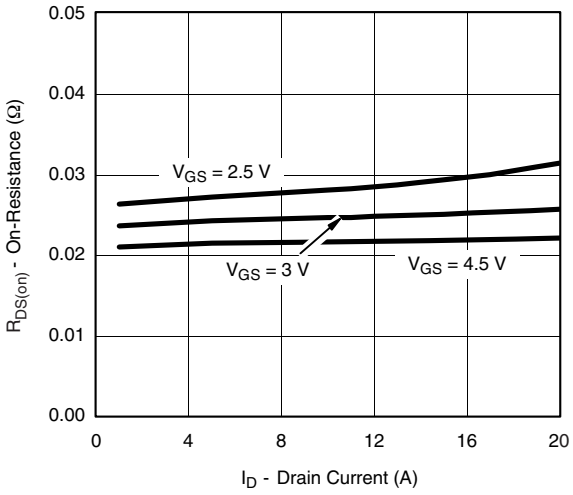
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



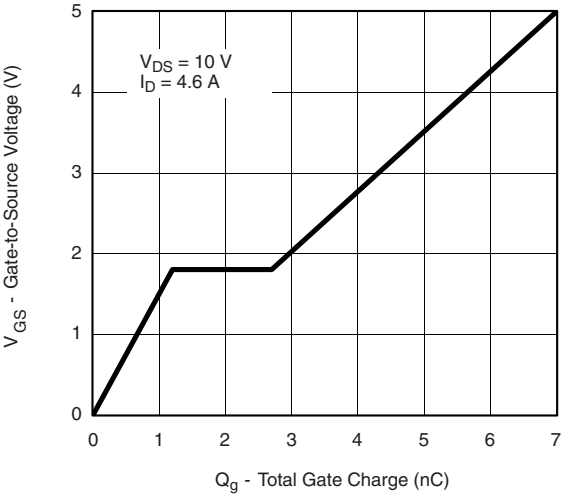
Output Characteristics



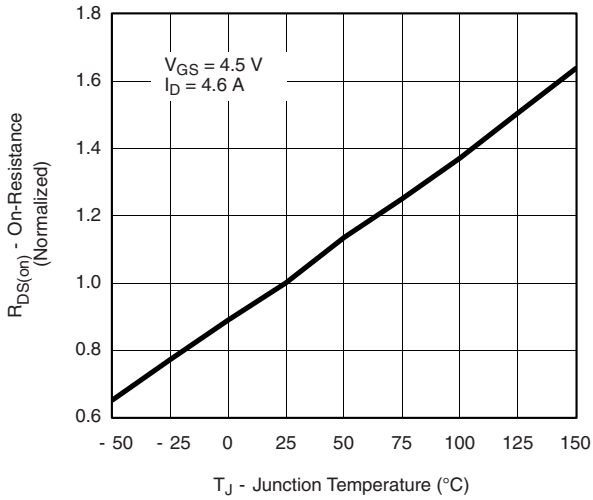
Transfer Characteristics



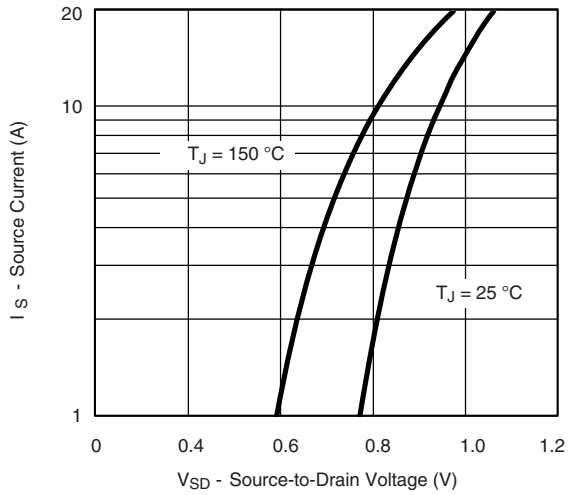
On-Resistance vs. Drain Current



Gate Charge

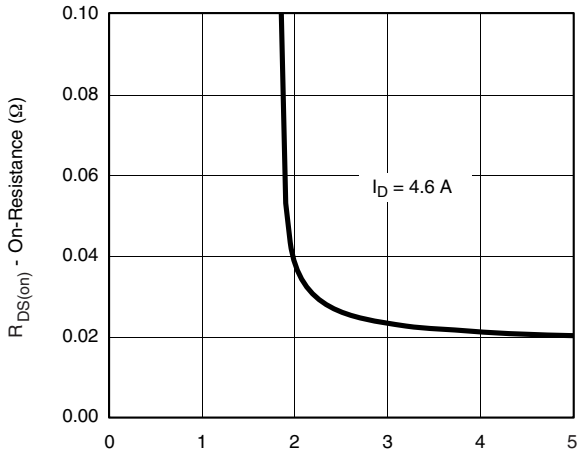


On-Resistance vs. Junction Temperature

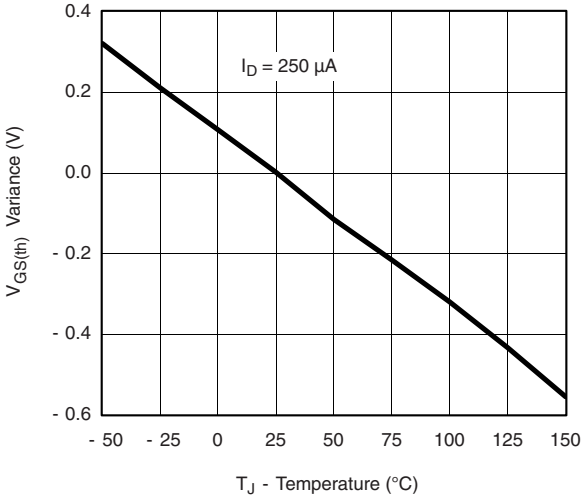


Source-Drain Diode Forward Voltage

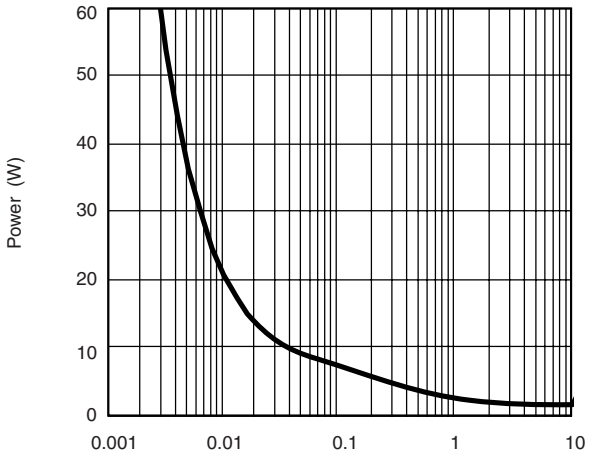
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



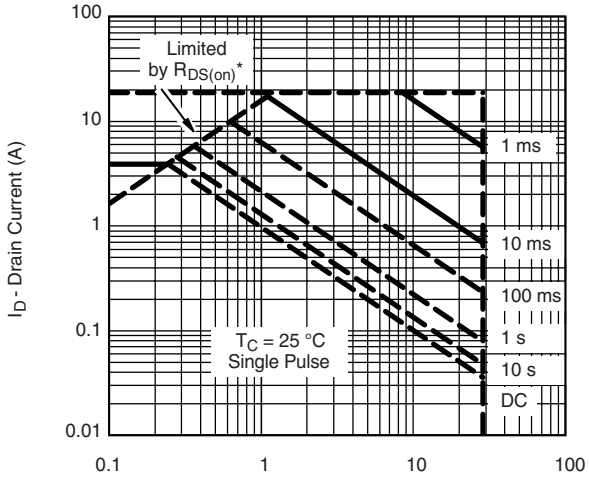
On-Resistance vs. Gate-to-Source Voltage



Threshold Voltage

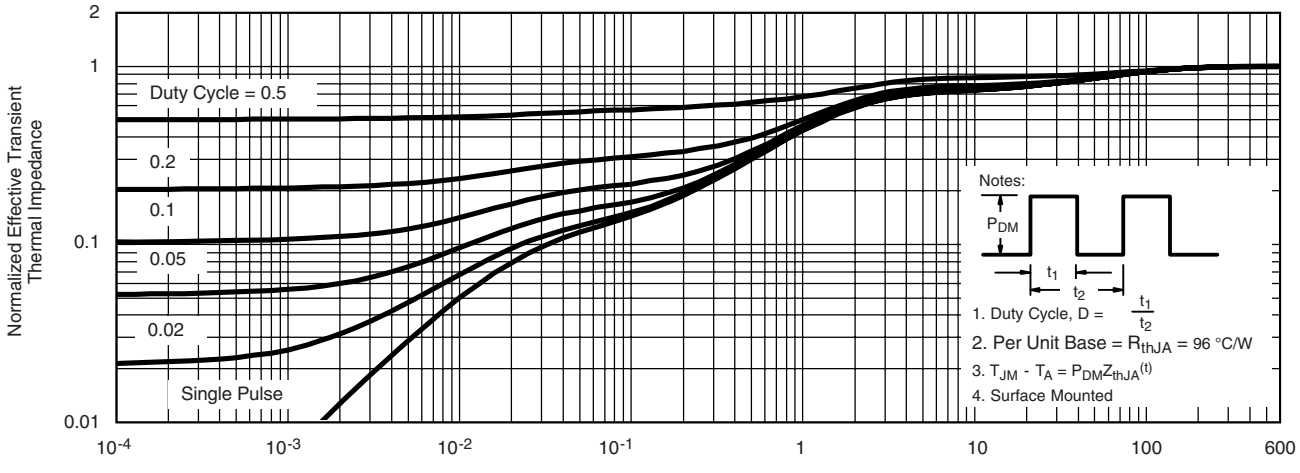


Single Pulse Power



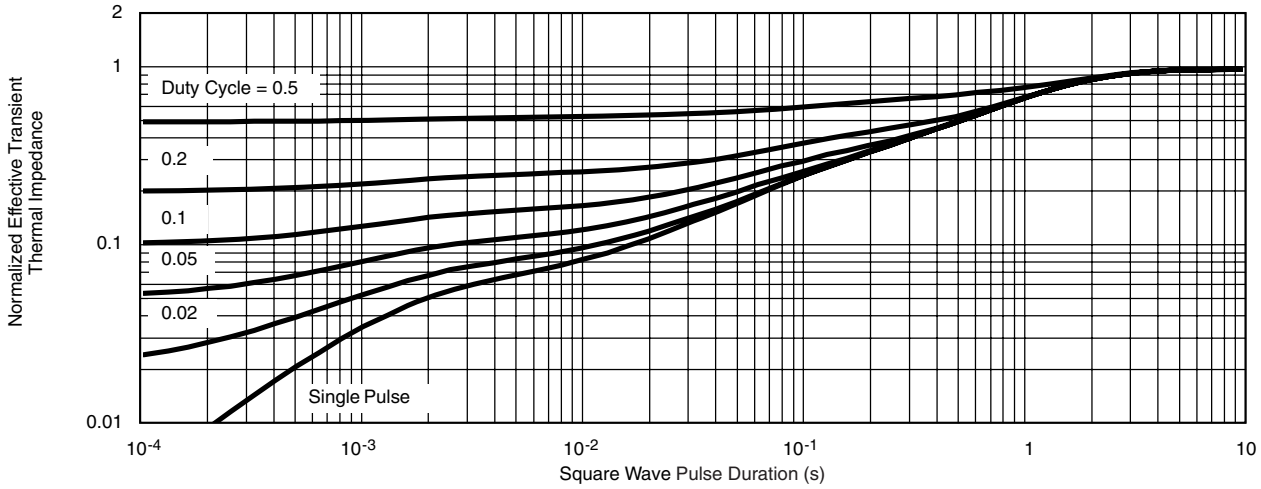
* V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

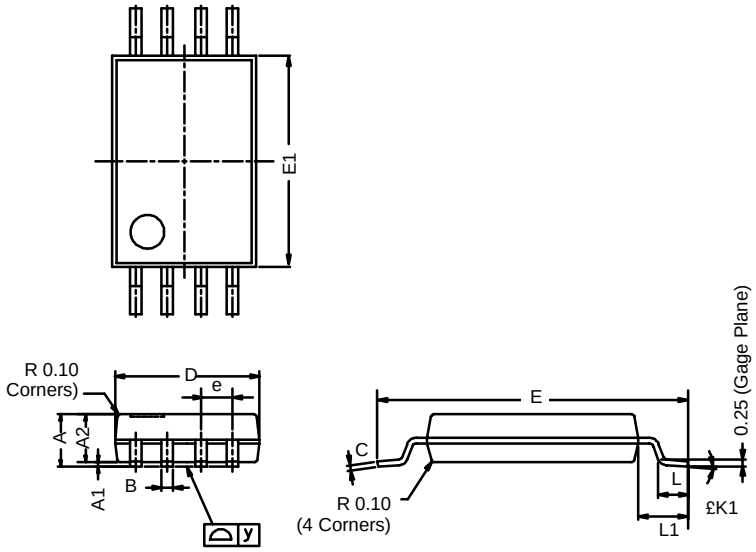


Normalized Thermal Transient Impedance, Junction-to-Foot

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72215.

TSSOP: 8-LEAD

JEDEC Part Number: MO-153



Dim	MILLIMETERS		
	Min	Nom	Max
A	–	–	1.20
A_1	0.05	0.10	0.15
A_2	0.80	1.00	1.05
B	0.19	0.28	0.30
C	–	0.127	–
D	2.90	3.00	3.10
E	6.20	6.40	6.60
E_1	4.30	4.40	4.50
e	–	0.65	–
L	0.45	0.60	0.75
L_1	0.90	1.00	1.10
Y	–	–	0.10
£K1	0°	3°	6°

ECN: S-03946—Rev. G, 09-Jul-01
DWG: 5844

LITTLE FOOT® TSSOP-8
The Next Step in Surface-Mount Power MOSFETs

Wharton McDaniel and David Oldham

When Vishay Siliconix introduced its LITTLE FOOT MOSFETs, it was the first time that power MOSFETs had been offered in a true surface-mount package, the SOIC. LITTLE FOOT immediately found a home in new small form factor disk drives, computers, and cellular phones.

The new LITTLE FOOT TSSOP-8 power MOSFETs are the natural evolutionary response to the continuing demands of many markets for smaller and smaller packages. LITTLE FOOT TSSOP-8 MOSFETs have a smaller footprint and a lower profile than LITTLE FOOT SOICs, while maintaining low $r_{DS(on)}$ and high thermal performance. Vishay Siliconix has accomplished this by putting one or two high-density MOSFET die in a standard 8-pin TSSOP package mounted on a custom leadframe.

THE TSSOP-8 PACKAGE

LITTLE FOOT TSSOP-8 power MOSFETs require approximately half the PC board area of an equivalent LITTLE FOOT device (Figure 1). In addition to the reduction in board area, the package height has been reduced to 1.1 mm.

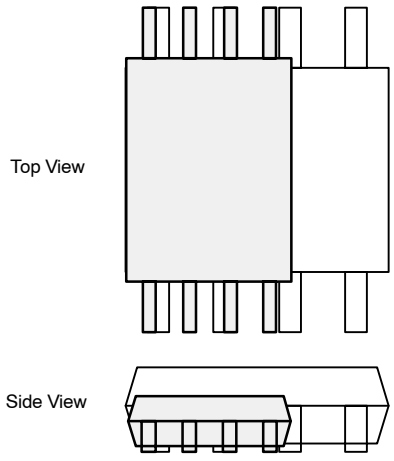


Figure 1. An TSSOP-8 Package Next to a SOIC-8 Package with Views from Both Top and Side

This is the low profile demanded by applications such as PCMCIA cards.

It reduces the power package to the same height as many resistors and capacitors in 0805 and 0605 sizes. It also allows placement on the “passive” side of the PC board.

The standard pinouts of the LITTLE FOOT TSSOP-8 packages have been changed from the standard established by LITTLE FOOT. This change minimizes the contribution of interconnection resistance to $r_{DS(on)}$ and maximizes the transfer of heat out of the package.

Figure 2 shows the pinouts for a single-die TSSOP. Notice that both sides of the package have Source and Drain connections, whereas LITTLE FOOT has the Source and Gate connections on one side of the package, and the Drain connections are on the opposite side.

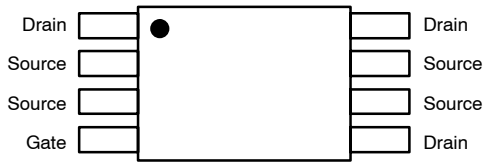


Figure 2. Pinouts for Single Die TSSOP

Figure 3 shows the standard pinouts for a dual-die TSSOP-8. In this case, the connections for each individual MOSFET occupy one side.

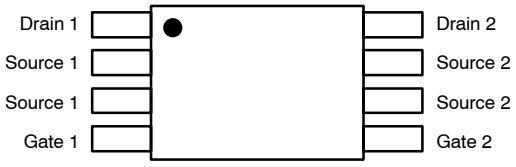
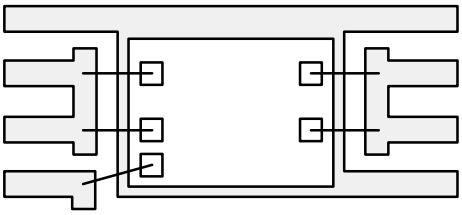


Figure 3. Pinouts for Dual-Die TSSOP

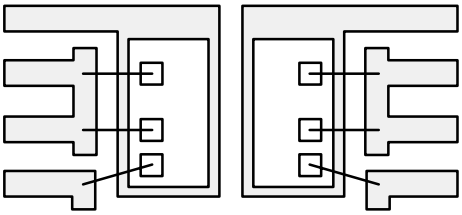
Because the TSSOP has a fine pitch foot print, the pad layout is somewhat more demanding than the layout of the SOIC. Careful attention must be paid to silkscreen-to-pad and soldermask-to-pad clearances. Also, fiduciary marks may be required. The design and spacing of the pads must be dealt with carefully. The pads must be sized to hold enough solder paste to form a good joint, but should not be so large or so placed as to extend under the body, increasing the potential for solder bridging. The pad pattern should allow for typical pick and place errors of 0.25 mm. See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286), for the recommended pad pattern for PC board layout.

THERMAL ISSUES

LITTLE FOOT TSSOP MOSFETs have been given thermal ratings using the same methods used for LITTLE FOOT. The maximum thermal resistance junction-to-ambient is 83°C/W for the single die and 125°C/W for dual-die parts. TSSOP relies on a leadframe similar to LITTLE FOOT to remove heat from the package. The single- and dual-die leadframes are shown in Figure 4.



a) 8-Pin Single-Pad TSSOP



b) 8-Pin Dual-Pad TSSOP

Figure 4. Leadframe

The MOSFETs are characterized using a single pulse power test. For this test the device mounted on a one-square-inch piece of copper clad FR-4 PC board, such as those shown in Figure 5. The single pulse power test determines the maximum amount of power the part can handle for a given pulse width and defines the thermal resistance junction-to-ambient. The test is run for pulse widths ranging from approximately 10 ms to 100 seconds. The thermal resistance at 30 seconds is the rated thermal resistance for the part. This rating was chosen to allow comparison of packages and leadframes. At longer pulse widths, the PC board thermal charateristics become dominant, making all parts look the same.

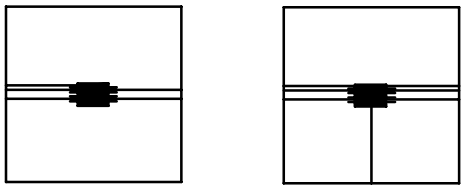


Figure 5.

The actual test is based on dissipating a known amount of power in the device for a known period of time so the junction temperature is raised to 150°C. The starting and ending junction temperatures are determined by measuring the forward drop of the body diode. The thermal resistance for that pulse width is defined by the temperature rise of the junction above ambient and the power of the pulse, ΔTja/P.

Figure 6 shows the single pulse power curve of the Si6436DQ laid over the curve of the Si9936DY to give a comparison of the thermal performance. The die in the two devices have equivalent die areas, making this a comparison of the packaging. This comparison shows that the TSSOP package performs as well as the SOIC out to 150 ms, with long-term performance being 0.5 W less. Although the thermal performance is less, LITTLE FOOT TSSOP will operate in a large percentage of applications that are currently being served by LITTLE FOOT.

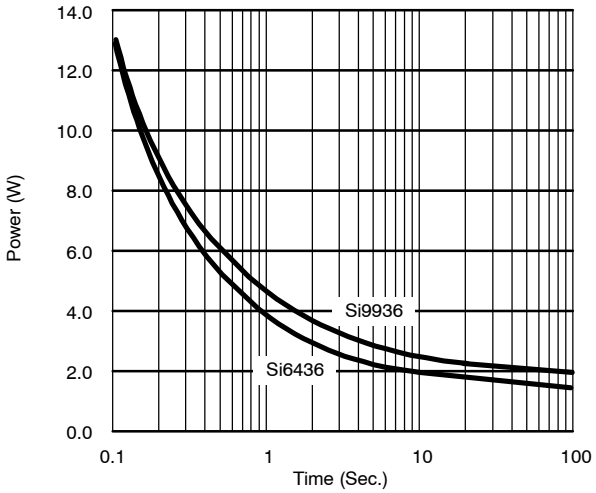


Figure 6. Comparison of Thermal Performance

CONCLUSION

TSSOP power MOSFETs provide a significant reduction in PC board footprint and package height, allowing reduction in board size and application where SOICs will not fit. This is accomplished using a standard IC package and a custom leadframe, combining small size with good power handling capability.

For the TSSOP-8 package outline visit:
http://www.vishay.com/doc?71201

For the SOIC-8 package outline visit:
http://www.vishay.com/doc?71192

Mounting LITTLE FOOT® TSSOP-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFET,* (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT TSSOP-8 power MOSFET package footprint. In converting the footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the TSSOP-8 package, the thermal connections are very simple. Pins 1, 5, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In the dual package, pins 1 and 8 are the two drains. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins also provide the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

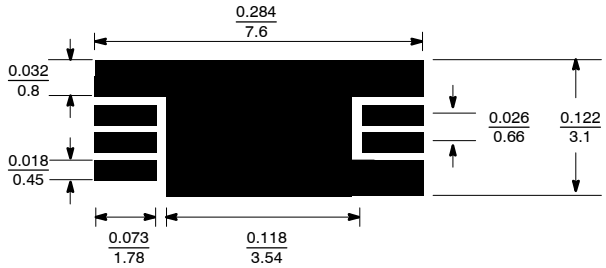


FIGURE 1. Single MOSFET TSSOP-8 Pad Pattern with Copper Spreading

The pad patterns with copper spreading for the single-MOSFET TSSOP-8 (Figure 1) and dual-MOSFET TSSOP-8 (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

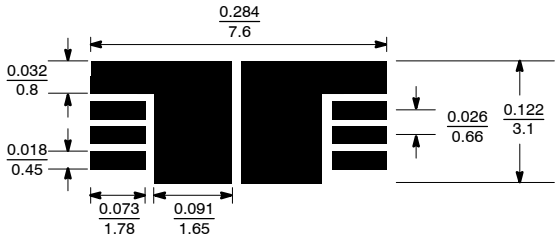
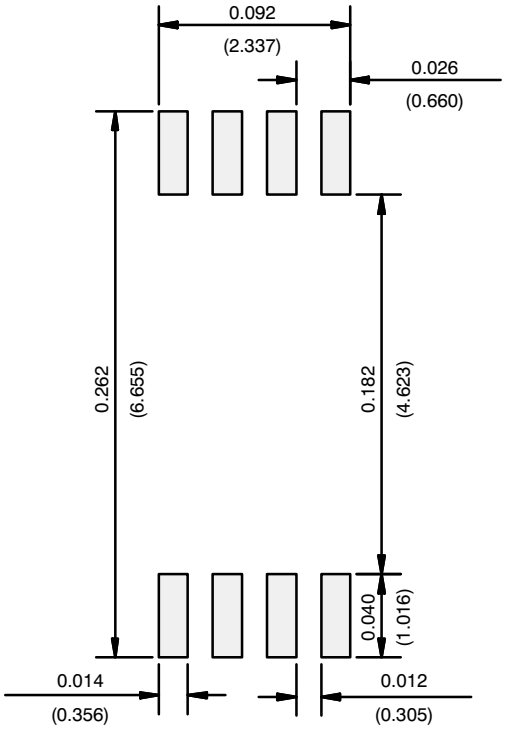


FIGURE 2. Dual MOSFET TSSOP-8 Pad Pattern with Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR TSSOP-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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