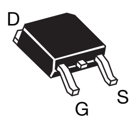
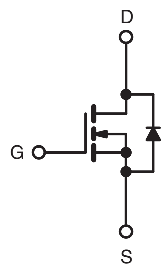
Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	50	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.20
Q_g (Max.) (nC)	10	
Q_{gs} (nC)	2.6	
Q_{gd} (nC)	4.8	
Configuration	Single	

DPAK (TO-252)





N-Channel MOSFET

FEATURES

- Low Drive Current
- Surface Mount
- Fast Switching
- Ease of Paralleling
- Excellent Temperature Stability
- Compliant to RoHS Directive 2002/95/EC

Pb Available
RoHS*
COMPLIANT

DESCRIPTION

The Power MOSFET technology is the key to Vishay's advanced line of Power MOSFET transistors. The efficient geometry and unique processing of this latest "State of the Art" design achieves: very low on-state resistance combined with high transconductance; superior reverse energy and diode recovery dV/dt capability.

The Power MOSFET transistors also feature all of the well established advantages of MOSFET'S such as voltage control, very fast switching, ease of paralleling and temperature stability of the electrical parameters.

Surface mount packages enhance circuit performance by reducing stray inductances and capacitance. The DPAK (TO-252) surface mount package brings the advantages of Power MOSFET's to high volume applications where PC Board surface mounting is desirable. The surface mount option IRFR9012, SiHFR9012 is provided on 16 mm tape. The straight lead option IRFU9012, SiHFU9012 of the device is called the IPAK (TO-251).

They are well suited for applications where limited heat dissipation is required such as, computers and peripherals, telecommunication equipment, dc-to-dc converters, and a wide range of consumer products.

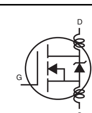
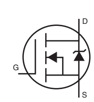
ORDERING INFORMATION	
Package	DPAK (TO-252)
Lead (Pb)-free	IRFR010PbF
	SiHFR010-E3
SnPb	IRFR010
	SiHFR010

ABSOLUTE MAXIMUM RATINGS (T_C = 25 °C, unless otherwise noted)					
PARAMETER			SYMBOL	LIMIT	UNIT
Drain-Source Voltage			V_{DS}	50	V
Gate-Source Voltage			V_{GS}	± 20	
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	8.2	A
		T_C = 100 °C		5.2	
Pulsed Drain Current[a]			I_{DM}	33	
Avalanche Current[b]			I_{AS}	1.5	
Linear Derating Factor				0.20	W/°C
Maximum Power Dissipation	T_C = 25 °C		P_D	25	W
Peak Diode Recovery dV/dt[c]			dV/dt	2.0	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. V_{DD} = 25 V, starting T_J = 25 °C, L = 100 µH, R_g = 25 Ω.
c. $I_{SD} \leq 8.2$ A, dI/dt ≤ 130 A/µs, $V_{DD} \leq 40$ V, $T_J \leq 150$ °C.
d. 1.6 mm from case.
e. When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS					
PARAMETER	**SYMBOL**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	
Case-to-Sink	R_{thCS}	-	1.7	-	°C/W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	5.0	

SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	50	-	-	V
Gate-Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 20 V	-	-	± 500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 50 V, V_{GS} = 0 V	-	-	250	μA
		V_{DS} = 40 V, V_{GS} = 0 V, T_J = 125 °C	-	-	1000	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 4.6 A[b]	-	0.16	0.20	Ω
Forward Transconductance	g_{fs}	V_{DS} ≥ 50 V, I_D = 3.6 A	2.1	3.1	-	S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1.0 MHz, see fig. 10	-	250	-	pF
Output Capacitance	C_{oss}		-	150	-	
Reverse Transfer Capacitance	C_{rss}		-	29	-	
Total Gate Charge	Q_g	V_{GS} = 10 V, I_D = 7.3 A, V_{DS} = 40 V, see fig. 6 and 13[b]	-	6.7	10	nC
Gate-Source Charge	Q_{gs}		-	1.8	2.6	
Gate-Drain Charge	Q_{gd}		-	3.2	4.8	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 25 V, I_D = 7.3 A, R_g = 24 Ω, R_D = 3.3 Ω, see fig. 10[b]	-	11	17	ns
Rise Time	t_r		-	33	50	
Turn-Off Delay Time	$t_{d(off)}$		-	12	18	
Fall Time	t_f		-	23	35	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact[c] 	-	4.5	-	nH
Internal Source Inductance	L_S		-	7.5	-	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 	-	-	8.2	A
Pulsed Diode Forward Current[a]	I_{SM}		-	-	33	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 8.2 A, V_{GS} = 0 V[b]	-	-	1.6	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 7.3 A, dI/dt = 100 A/μs[b]	41	86	190	ns
Body Diode Reverse Recovery Charge	Q_{rr}		0.15	0.33	0.78	μC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)				

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Pulse width ≤ 300 μs; duty cycle ≤ 2 %.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)

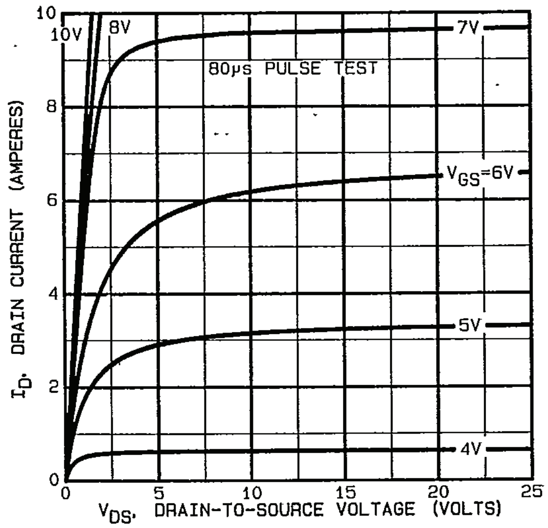


Fig. 1 - Typical Output Characteristics

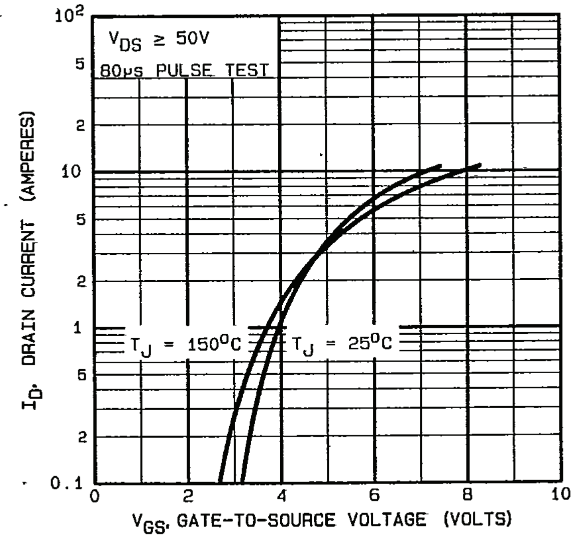


Fig. 3 - Typical Transfer Characteristics

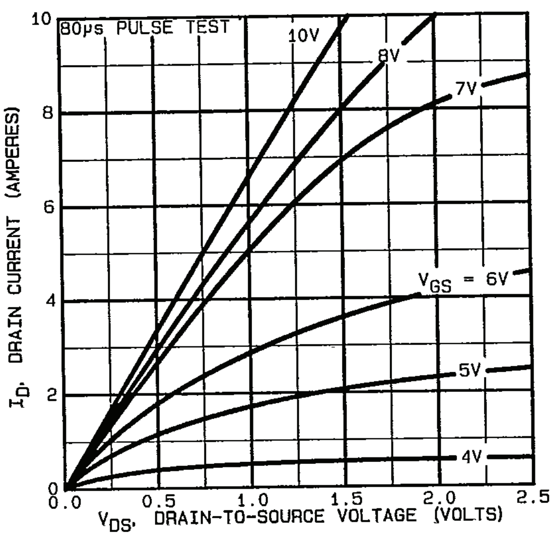


Fig. 2 - Typical Output Characteristics

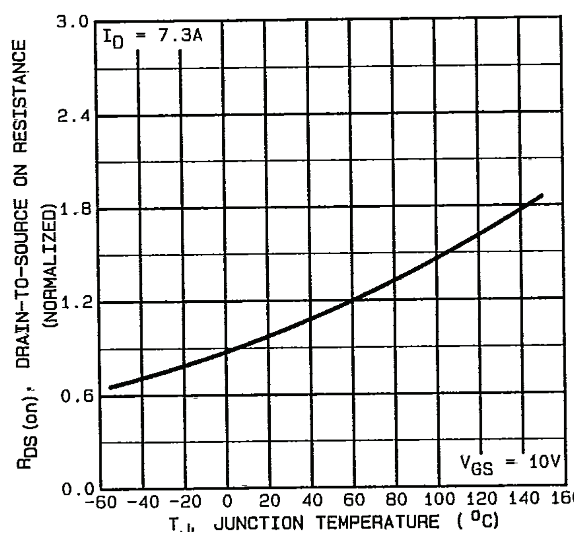


Fig. 4 - Normalized On-Resistance vs. Temperature

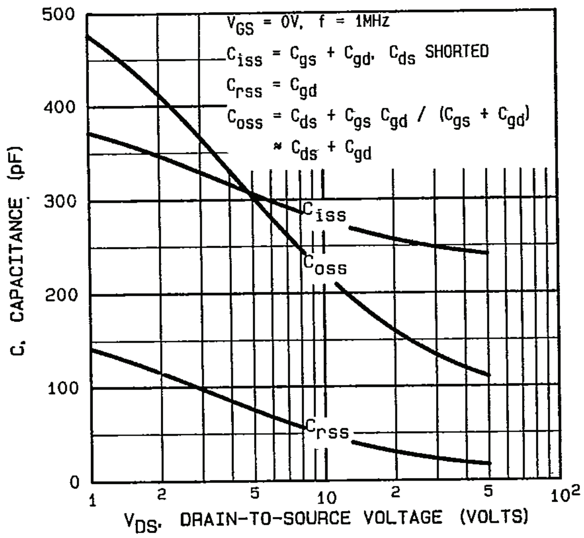


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

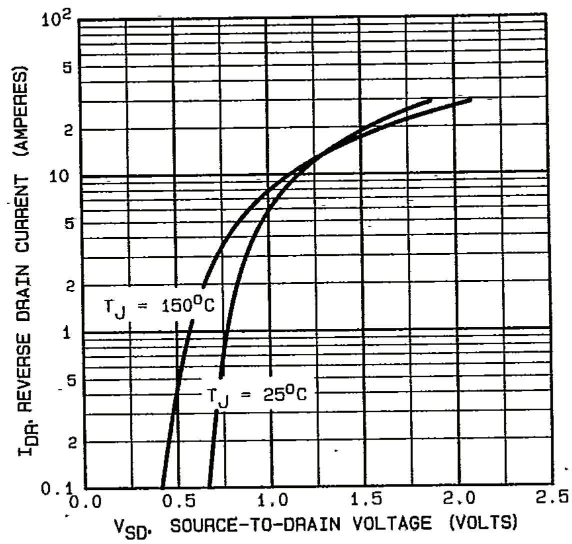


Fig. 7 - Typical Source-Drain Diode Forward Voltage

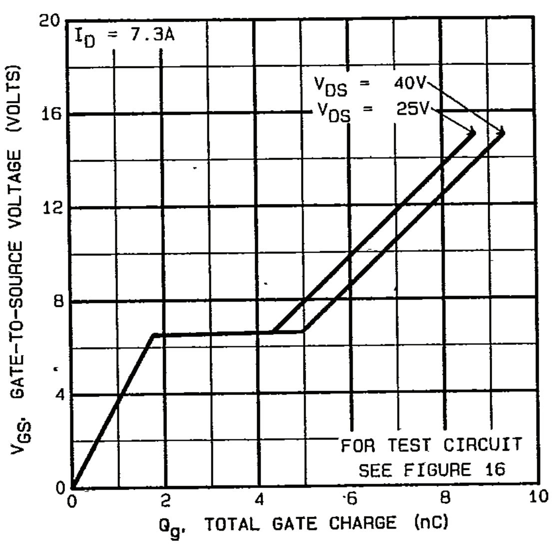


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

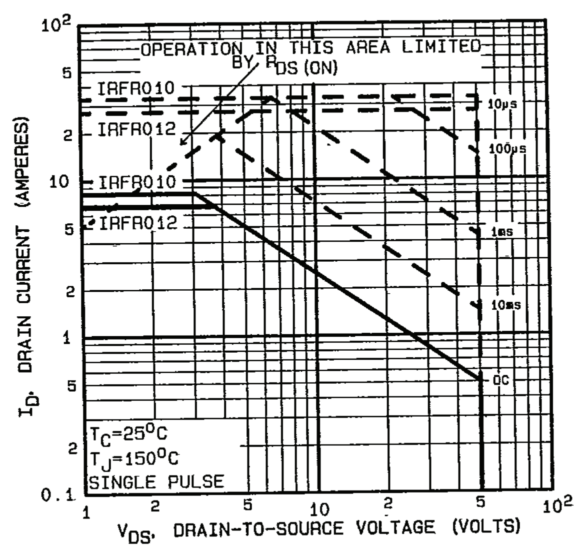


Fig. 8 - Maximum Safe Operating Area

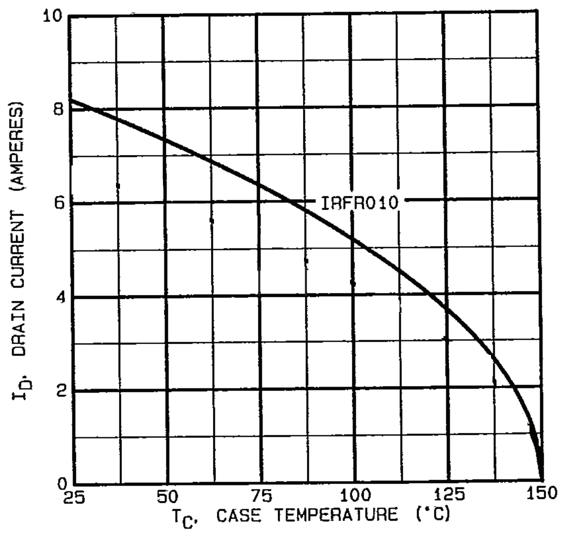


Fig. 9 - Maximum Drain Current vs. Case Temperature

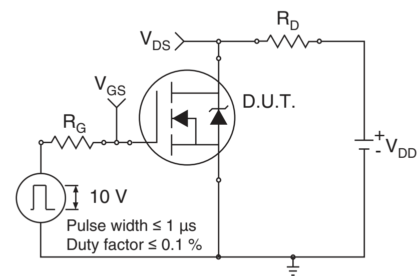


Fig. 10a - Switching Time Test Circuit

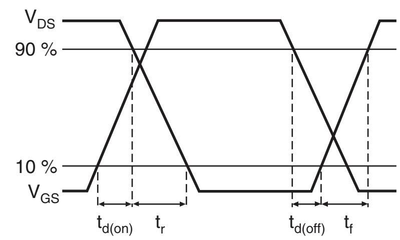


Fig. 10b - Switching Time Waveforms

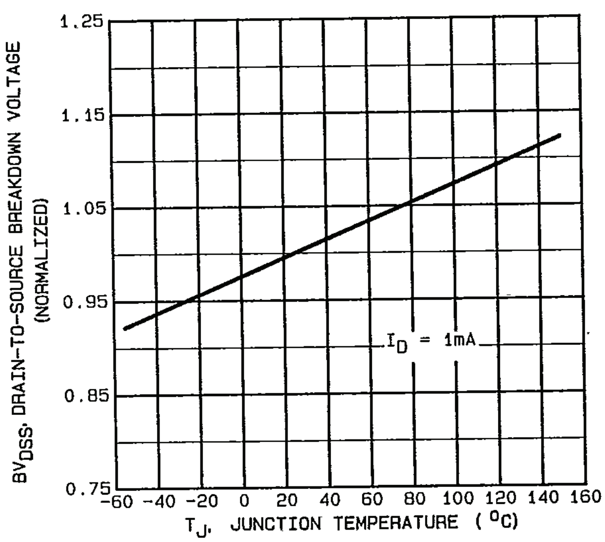


Fig. 10 - Breakdown Voltage vs. Temperature

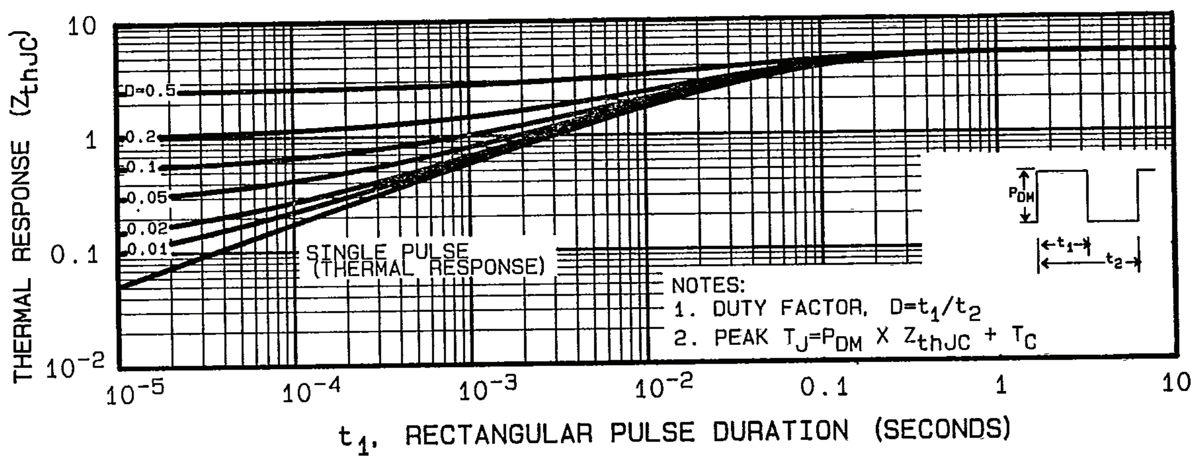


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

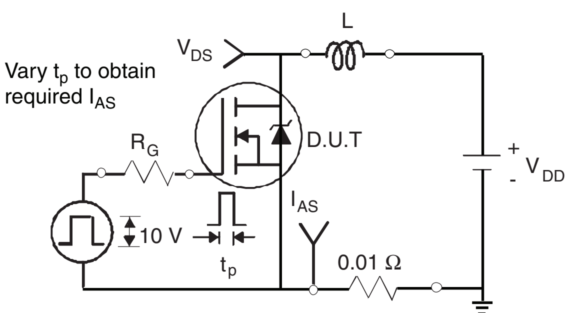


Fig. 12a - Unclamped Inductive Test Circuit

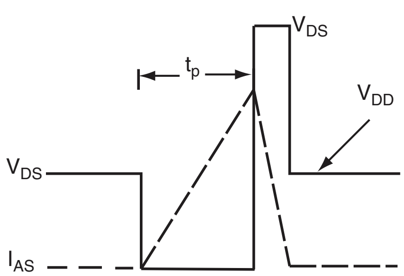


Fig. 12b - Unclamped Inductive Waveforms

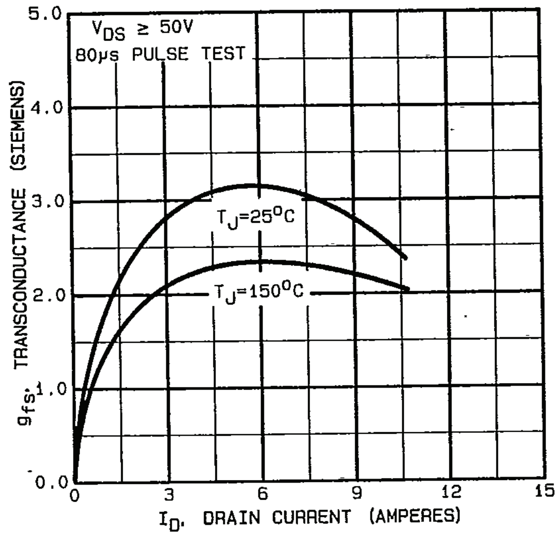


Fig. 12c - Typical Transconductance vs. Drain Current

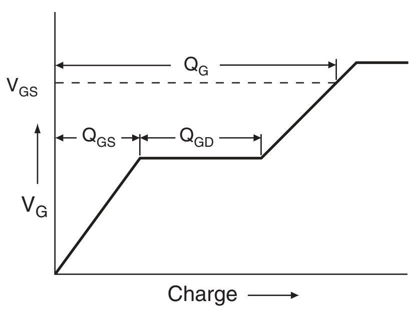


Fig. 13a - Basic Gate Charge Waveform

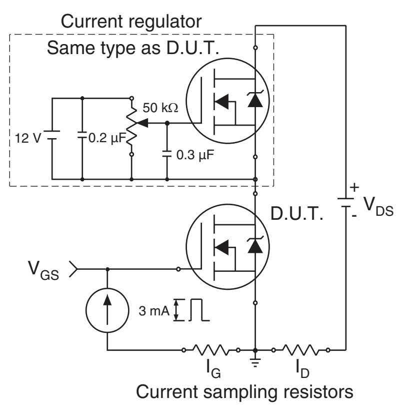
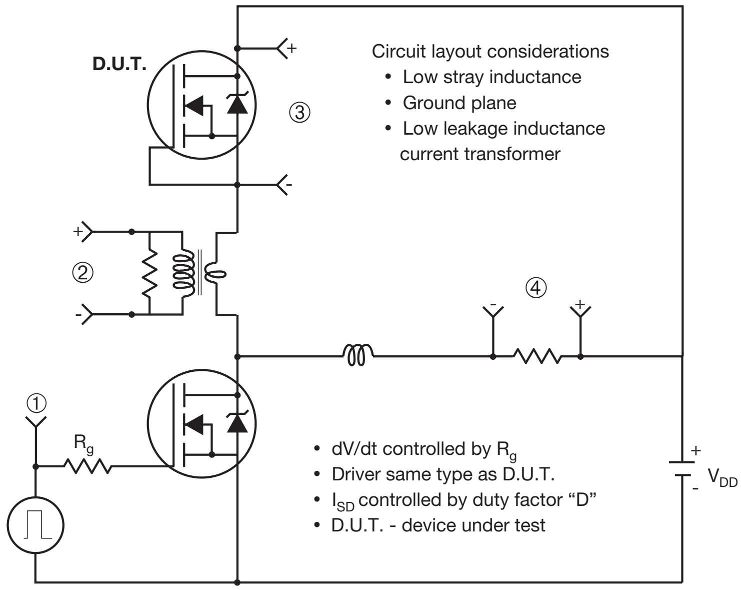
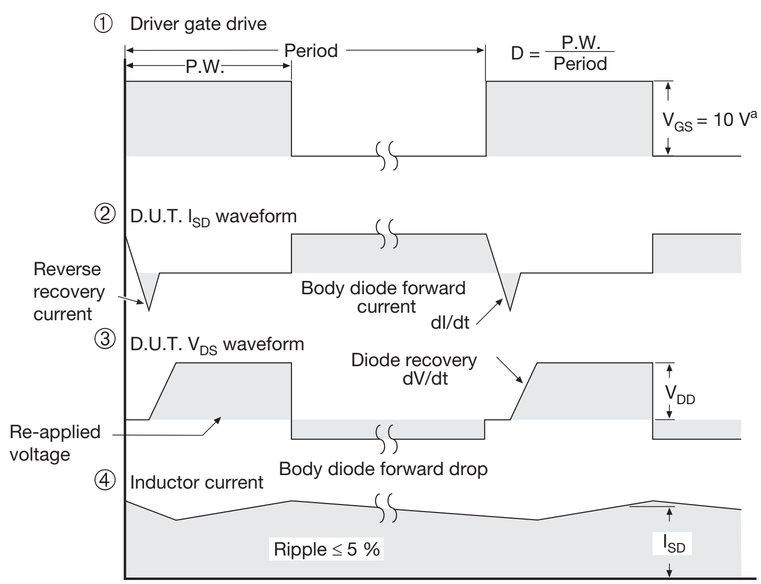


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





Note

a. V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

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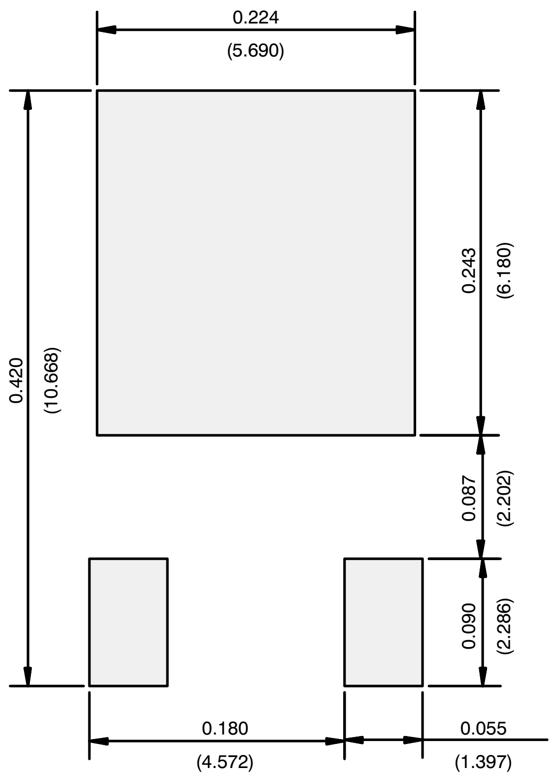
RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads
Dimensions in Inches/(mm)

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