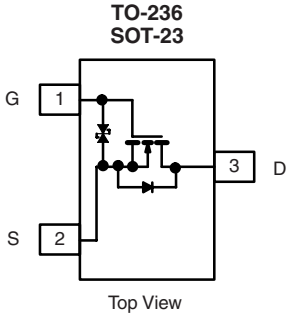
N-Channel 60-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (mA)
60	2 at V_{GS} = 10 V	300



Top View

2N7002K (7K)*
* Marking Code

Ordering Information: 2N7002K-T1
2N7002K-T1-E3 (Lead (Pb)-free)
2N7002K-T1-GE3 (Lead (Pb)-free and Halogen-free)

FEATURES

- **Halogen-free According to IEC 61249-2-21 Definition**
- Low On-Resistance: 2 Ω
- Low Threshold: 2 V (typ.)
- Low Input Capacitance: 25 pF
- Fast Switching Speed: 25 ns
- Low Input and Output Leakage
- TrenchFET® Power MOSFET
- 2000 V ESD Protection
- Compliant to RoHS Directive 2002/95/EC

Pb-free Available
RoHS* COMPLIANT
HALOGEN FREE Available

BENEFITS

- Low Offset Voltage
- Low-Voltage Operation
- Easily Driven Without Buffer
- High-Speed Circuits
- Low Error Voltage

APPLICATIONS

- Direct Logic-Level Interface: TTL/CMOS
- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- Battery Operated Systems
- Solid-State Relays

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C, unless otherwise noted

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	60	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current (T_J = 150 °C)[b]	T_A = 25 °C	I_D	300	mA
	T_A = 100 °C		190	
Pulsed Drain Current[a]		I_{DM}	800	
Power Dissipation[b]	T_A = 25 °C	P_D	0.35	W
	T_A = 100 °C		0.14	
Maximum Junction-to-Ambient[b]		R_{thJA}	350	°C/W
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to 150	°C

Notes:
a. Pulse width limited by maximum junction temperature.
b. Surface Mounted on FR4 board.

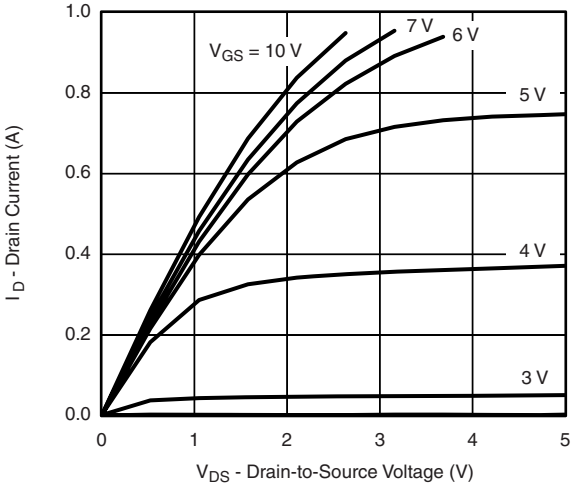
* Pb containing terminations are not RoHS compliant, exemptions may apply.

SPECIFICATIONS T_A = 25 °C, unless otherwise noted						
			Limits			
Parameter	**Symbol**	**Test Conditions**	**Min.**	**Typ.[a]**	**Max.**	**Unit**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 10 µA	60			V
Gate-Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 µA	1		2.5	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V			± 10	µA
		V_{DS} = 0 V, V_{GS} = ± 15 V			1	
		V_{DS} = 0 V, V_{GS} = ± 10 V			± 150	nA
		V_{DS} = 0 V, V_{GS} = ± 10 V, T_J = 85 °C			± 1000	
		V_{DS} = 0 V, V_{GS} = ± 5 V			± 100	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			1	µA
		V_{DS} = 60 V, V_{GS} = 0 V , T_J = 125 °C			500	
On-State Drain Current[a]	$I_{D(on)}$	V_{GS} = 10 V, V_{DS} = 7.5 V	800			mA
		V_{GS} = 4.5 V, V_{DS} = 10 V	500			
Drain-Source On-Resistance[a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 500 mA			2	Ω
		V_{GS} = 4.5 V, I_D = 200 mA			4	
Forward Transconductance[a]	g_{fs}	V_{DS} = 10 V, I_D = 200 mA	100			mS
Diode Forward Voltage	V_{SD}	I_S = 200 mA, V_{GS} = 0 V			1.3	V
Dynamic[a]						
Total Gate Charge	Q_g	V_{DS} = 10 V, V_{GS} = 4.5 V $I_D \cong$ 250 mA		0.4	0.6	nC
Input Capacitance	C_{iss}	V_{DS} = 25 V, V_{GS} = 0 V f = 1 MHz		30		pF
Output Capacitance	C_{oss}			6		
Reverse Transfer Capacitance	C_{rss}			2.5		
Switching[a, b, c]						
Turn-On Time	$t_{d(on)}$	V_{DD} = 30 V, R_L = 150 Ω $I_D \cong$ 200 mA, V_{GEN} = 10 V, R_G = 10 Ω			25	ns
Turn-Off Time	$t_{d(off)}$				35	

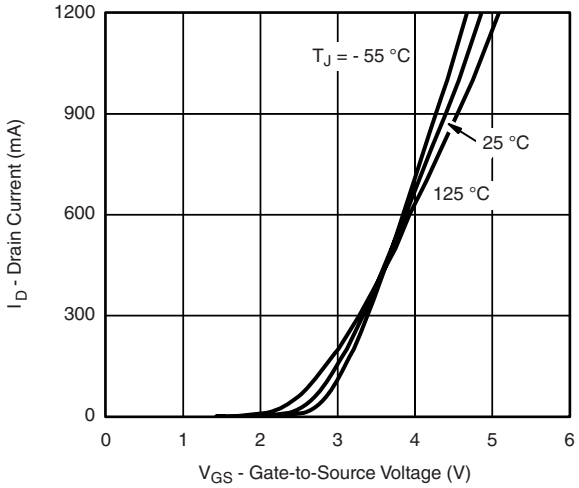
Notes:
a. For DESIGN AID ONLY, not subject to production testing.
b. Pulse test: PW ≤ 300 µs duty cycle ≤ 2 %.
c. Switching time is essentially independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

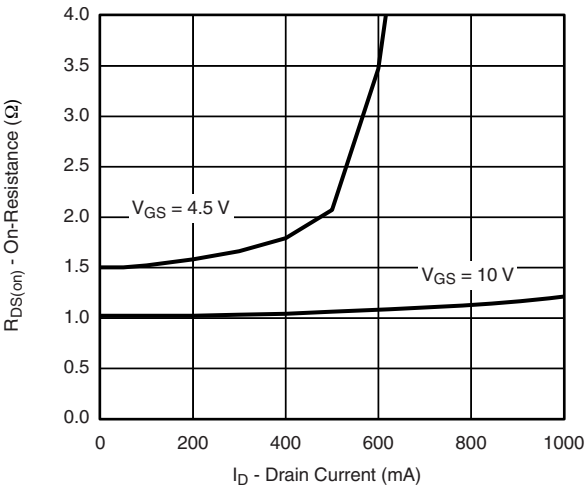
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



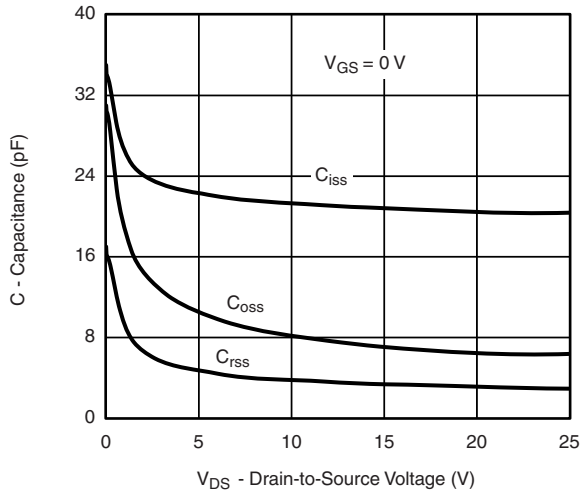
Output Characteristics



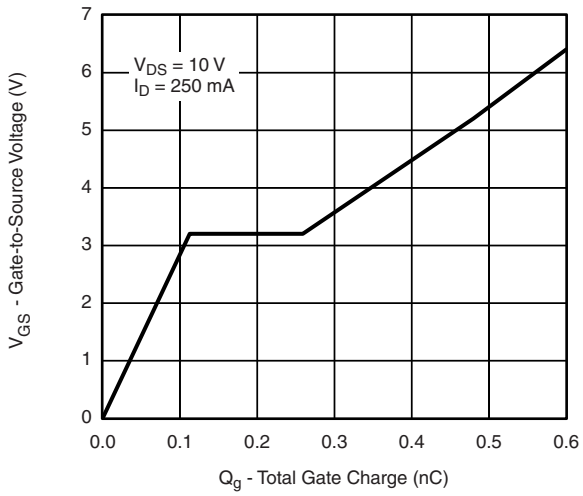
Transfer Characteristics



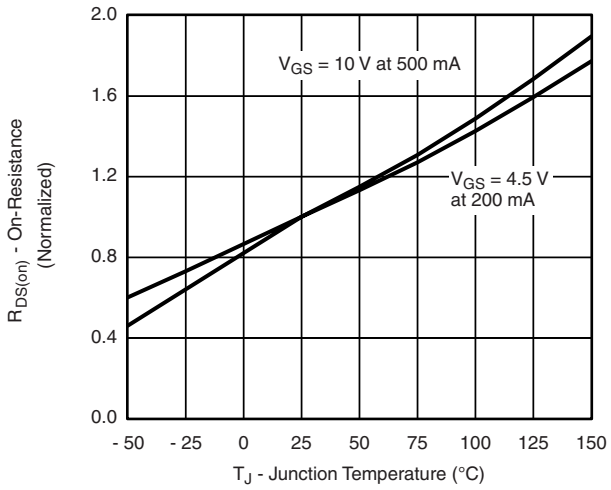
On-Resistance vs. Drain Current



Capacitance

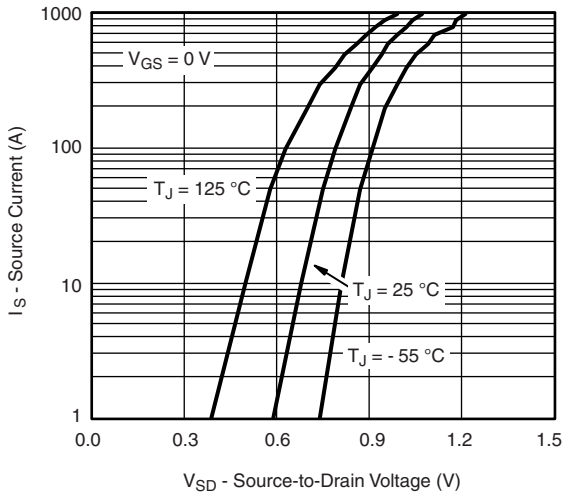


Gate Charge

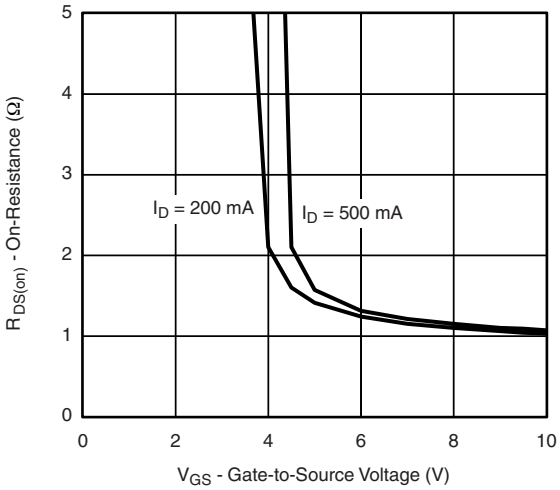


On-Resistance vs. Junction Temperature

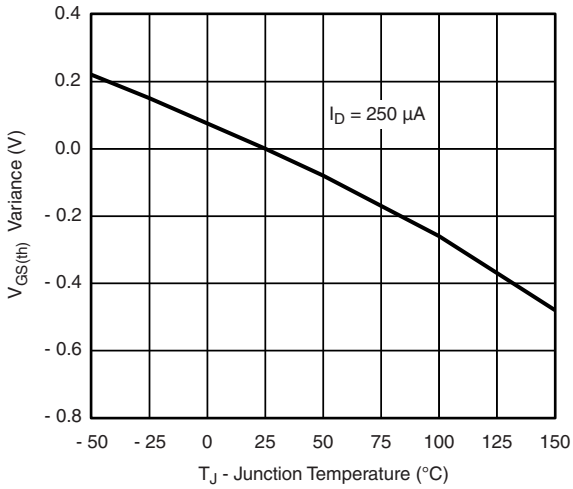
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



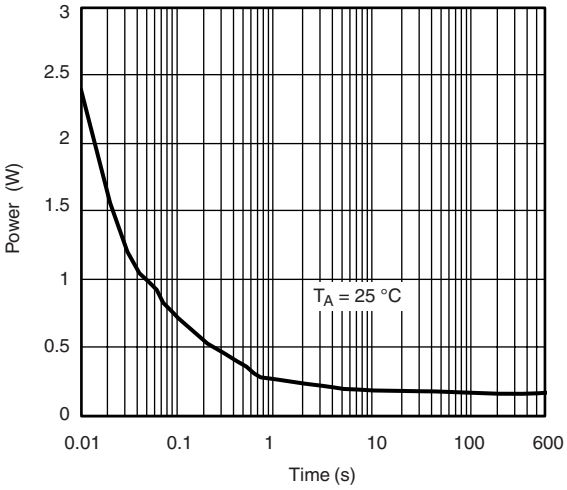
Source-Drain Diode Forward Voltage



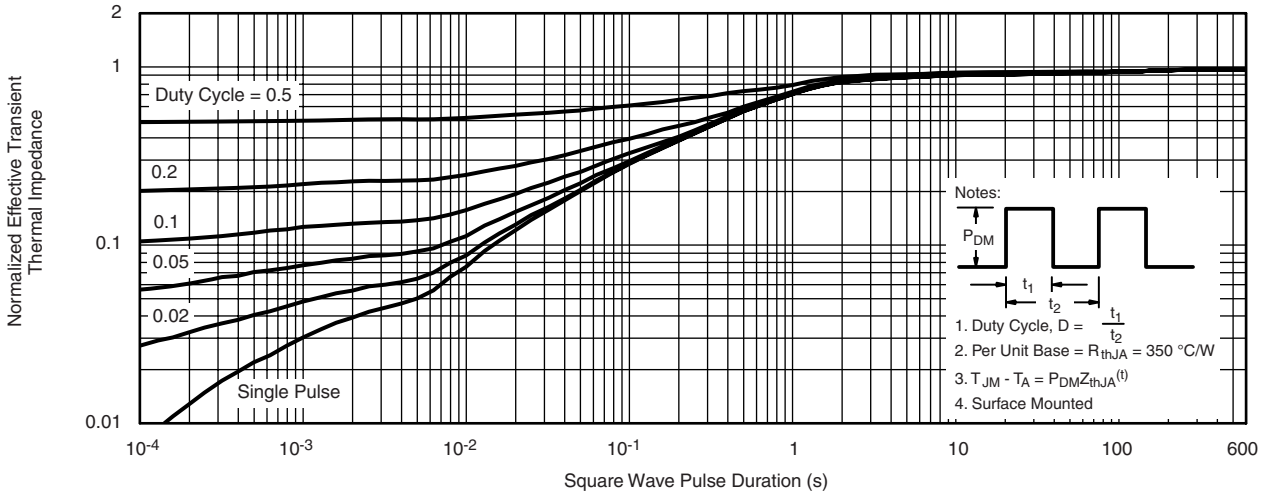
On-Resistance vs. Gate-Source Voltage



Threshold Voltage Variance Over Temperature

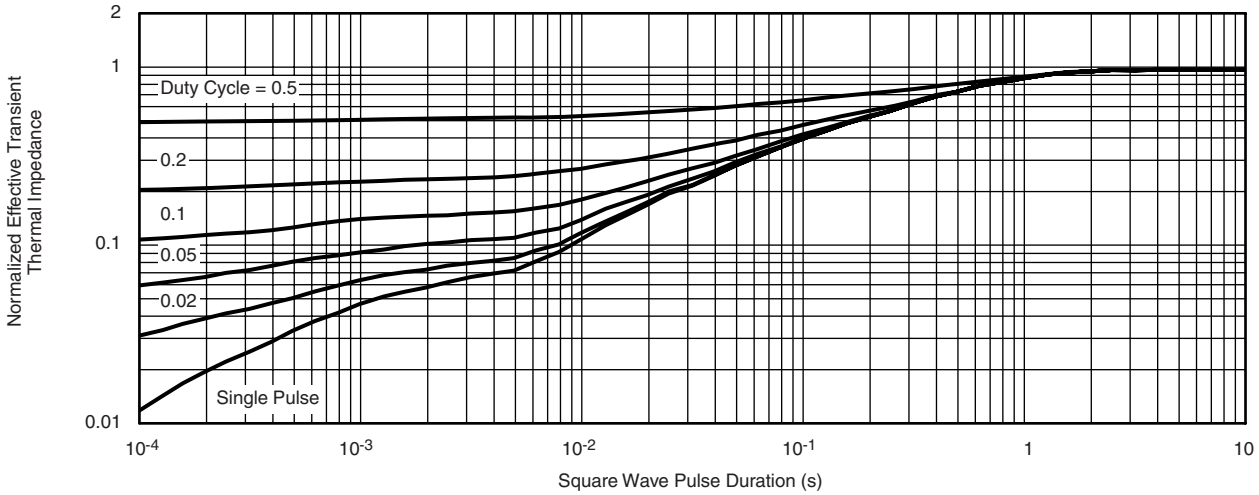


Single Pulse Power, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Ambient

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Foot

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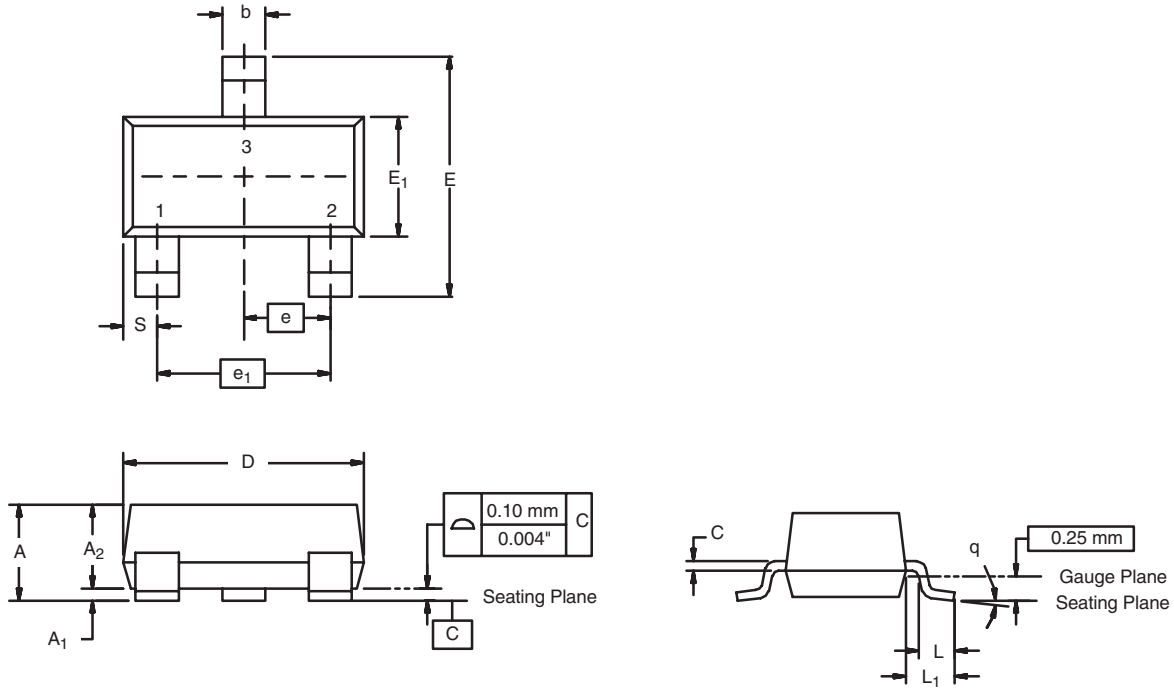
SOT-23 (TO-236): 3-LEAD



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	0.89	1.12	0.035	0.044
A_1	0.01	0.10	0.0004	0.004
A_2	0.88	1.02	0.0346	0.040
b	0.35	0.50	0.014	0.020
c	0.085	0.18	0.003	0.007
D	2.80	3.04	0.110	0.120
E	2.10	2.64	0.083	0.104
E_1	1.20	1.40	0.047	0.055
e	0.95 BSC		0.0374 Ref	
e_1	1.90 BSC		0.0748 Ref	
L	0.40	0.60	0.016	0.024
L_1	0.64 Ref		0.025 Ref	
S	0.50 Ref		0.020 Ref	
q	3°	8°	3°	8°
ECN: S-03946-Rev. K, 09-Jul-01 DWG: 5479				

Mounting LITTLE FOOT® SOT-23 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SOT-23 power MOSFET footprint . In converting this footprint to the pad set for a power device, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

The electrical connections for the SOT-23 are very simple. Pin 1 is the gate, pin 2 is the source, and pin 3 is the drain. As in the other LITTLE FOOT packages, the drain pin serves the additional function of providing the thermal connection from the package to the PC board. The total cross section of a copper trace connected to the drain may be adequate to carry the current required for the application, but it may be inadequate thermally. Also, heat spreads in a circular fashion from the heat source. In this case the drain pin is the heat source when looking at heat spread on the PC board.

Figure 1 shows the footprint with copper spreading for the SOT-23 package. This pattern shows the starting point for utilizing the board area available for the heat spreading copper. To create this pattern, a plane of copper overlies the drain pin and provides planar copper to draw heat from the drain lead and start the process of spreading the heat so it can be dissipated into the ambient air. This pattern uses all the available area underneath the body for this purpose.

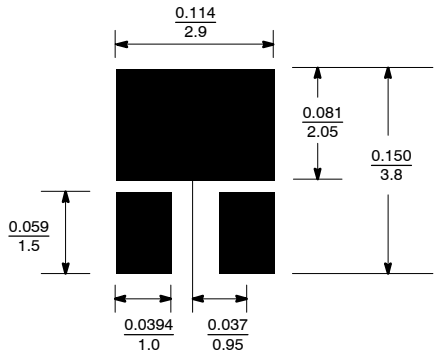
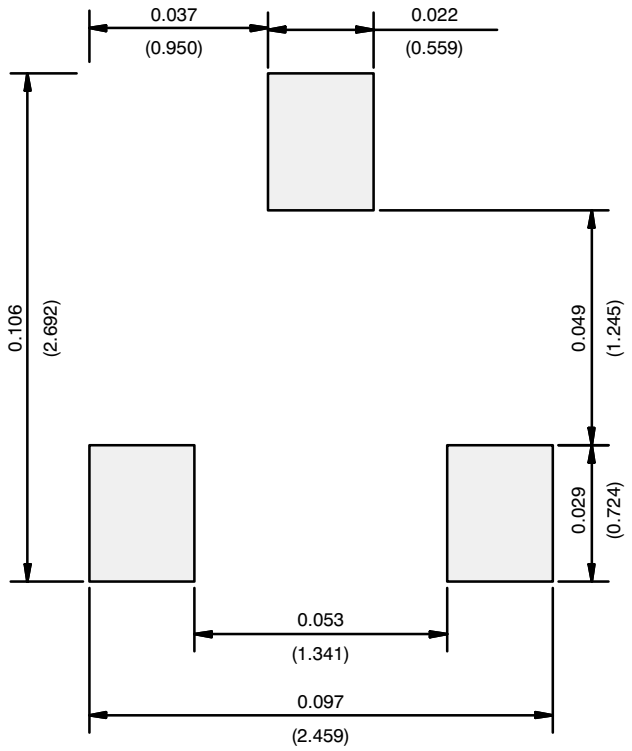


FIGURE 1. Footprint With Copper Spreading

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low-impedance path for heat to move away from the device.

RECOMMENDED MINIMUM PADS FOR SOT-23



Recommended Minimum Pads
Dimensions in Inches/(mm)

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APPLICATION NOTE

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