

Vishay Siliconix

N-Channel 240-V (D-S) MOSFET

PRODUCT SUMMARY								
V _{DS} (V)	$R_{DS(on)}(\Omega)$	I _D (A)	Q _g (Typ.)					
240	2.9 at V _{GS} = 10 V	1.52	2.54 nC					
	2.95 at V _{GS} = 4.5 V	1.5						
	3.5 at V _{GS} = 2.5 V	1.44						

FEATURES

Halogen-free

APPLICATIONS

- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-70 Package

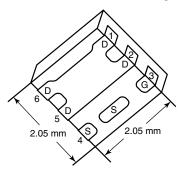
Boost Converter for Portable Devices

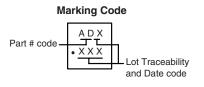
- Small Footprint Area
- Low On-Resistance

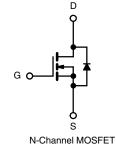


ROHS

PowerPAK SC-70-6L-Single







Ordering Information: SiA450DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS	$T_A = 25 ^{\circ}C$, unles	ss otherwise note	ed			
Parameter		Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	240	V		
Gate-Source Voltage		V_{GS}	± 20	v		
	T _C = 25 °C		1.52			
Continuous Drain Current (T _{.1} = 150 °C)	T _C = 70 °C	I-	1.21			
Continuous Diain Current (1) = 130 °C)	T _A = 25 °C	I _D	0.70 ^{a, b}			
	T _A = 70 °C		0.56 ^{a, b}	Α		
Pulsed Drain Current	•	I _{DM}	1.5			
Continuous Source-Drain Diode Current	T _C = 25 °C	l _a	12.8			
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	2.74 ^{a, b}			
	T _C = 25 °C		15			
Maximum Power Dissipation	T _C = 70 °C	P _D	9.8	w		
Maximum Fower Dissipation	T _A = 25 °C	' D	3.3 ^{a, b}	VV		
	T _A = 70 °C		2.1 ^{a, b}			
Operating Junction and Storage Temperature Ra	ange	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperature	e) ^{c, d}		260			

THERMAL RESISTANCE RATINGS									
Parameter		Symbol	Typical	Maximum	Unit				
Maximum Junction-to-Ambient ^{a, e} t ≤		R_{thJA}	30	38	°C/W				
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	6.5	8.1					

Notes:

- a. Surface Mounted on 1" x 1" FR4 board.
- b. t = 5 s.
- c. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- d. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- e. Maximum under Steady State conditions is 80 °C/W.

SiA450DJ

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SPECIFICATIONS $T_J = 25 ^{\circ}\text{C}_s$	Symbol	Test Conditions	Min.	Typ.	Max.	Unit			
Static									
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	240			V			
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$			247.4					
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	I _D = - 250 μA		4.22		mV/°C			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = - 250 μA	0.8		2.4	V			
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA			
		V _{DS} = 240 V, V _{GS} = 0 V			- 1				
Zero Gate Voltage Drain Current	IDSS	V _{DS} = 240 V, V _{GS} = 0 V, T _J = 55 °C			- 10	μΑ			
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \le 10 \text{ V}, V_{GS} = 10 \text{ V}$	1.5			Α			
		V _{GS} = 10 V, I _D = 0.70 A		2.4	2.9				
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 0.65 \text{ A}$		2.46	2.95	Ω			
	, ,	$V_{GS} = 2.5 \text{ V}, I_D = 0.50 \text{ A}$		2.85	85 3.5				
Forward Transconductance ^a	9 _{fs}	V _{DS} = 120 V, I _D = 0.70 A		3.14		S			
Dynamic ^b									
Input Capacitance	C _{iss}			167					
Output Capacitance	C _{oss}	$V_{DS} = 120 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		10		pF			
Reverse Transfer Capacitance	C _{rss}			3.4					
	Q _g	V _{DS} = 120 V, V _{GS} = 10 V, I _D = 0.70 A		4.69	7.035	 			
Total Gate Charge				2.54	3.81				
Gate-Source Charge		$V_{DS} = 120 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 0.70 \text{ A}$		0.58		nC			
Gate-Drain Charge	Q_{gd}			1.14					
Gate Resistance	R_{g}	f = 1 MHz		2		Ω			
Turn-On Delay Time	t _{d(on)}			13.7	21				
Rise Time	t _r	V_{DD} = 120 V, R_L = 200 Ω		22	33	_			
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 0.60$ A, V_{GEN} = 4.5 V, R_g = 1 Ω		23	35				
Fall Time	t _f			19	29				
Turn-On Delay Time	t _{d(on)}			4.5	6.75	ns			
Rise Time	t _r	V_{DD} = 120 V, R_L = 184 Ω		11	16.5				
Turn-Off Delay Time	t _{d(off)}	$I_D\cong 0.70$ A, $V_{GEN}=10$ V, $R_g=1$ Ω		12	18				
Fall Time	t _f			15	22.5				
Drain-Source Body Diode Characterist	ics			•	•				
Continuous Source-Drain Diode Current	I _S	$T_C = 25 ^{\circ}C$			2.7	А			
Pulse Diode Forward Current	I _{SM}				12.8				
Body Diode Voltage	V _{SD}	$I_S = 0.5 \text{ A}, V_{GS} = 0 \text{ V}$		0.8	1.2	V			
Body Diode Reverse Recovery Time	t _{rr}			50.2	75.3	ns			
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 0.5 A, di/dt = 100 A/μs, T _J = 25 °C		68	102	nC			
Reverse Recovery Fall Time	ta	$I_{F} = 0.5 \text{ A}$, $I_{J} = 25 \text{ C}$		25		ns			
Reverse Recovery Rise Time	t _b			25.2					

Notes:

- a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$
- b. Guaranteed by design, not subject to production testing.

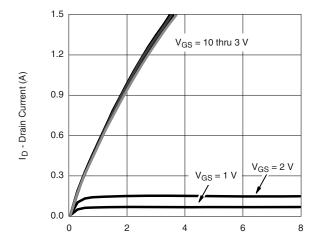
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



R_{DS(on)} - On-Resistance (᠒)

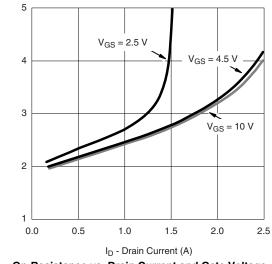
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

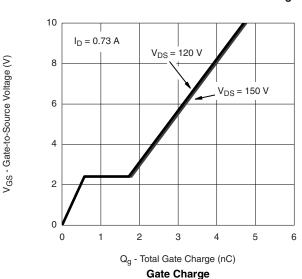


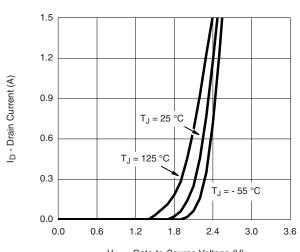
V_{DS} - Drain-to-Source Voltage (V)

Output Characteristics



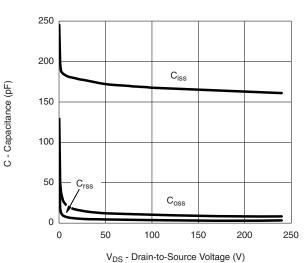
On-Resistance vs. Drain Current and Gate Voltage





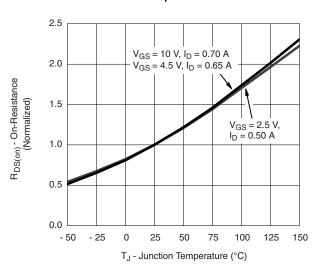
 $V_{\mbox{\footnotesize GS}}$ - Gate-to-Source Voltage (V)

Transfer Characteristics



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Capacitance



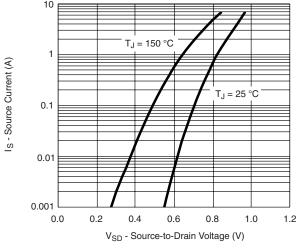
On-Resistance vs. Junction Temperature

SiA450DJ

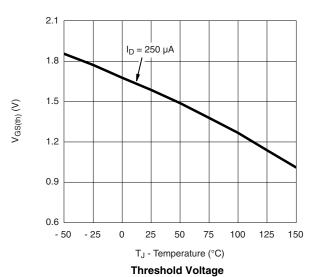
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

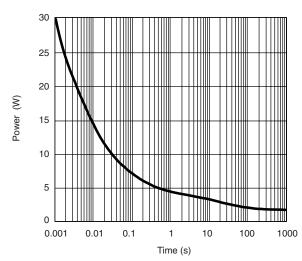


Soure-Drain Diode Forward Voltage

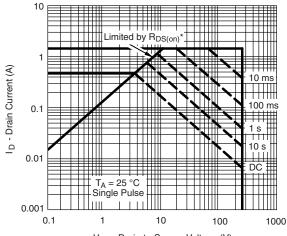


 $I_{D} = 0.70 \text{ A}$ $I_{D} = 0.70 \text{ A}$ $I_{D} = 0.70 \text{ A}$ $I_{A} = 125 \text{ °C}$ $I_{A} = 25 \text{ °C}$

On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient



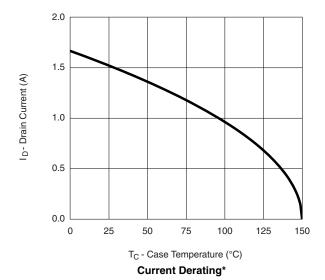
 $$V_{DS}$$ - Drain-to-Source Voltage (V) $$^*\ V_{GS} > $minimum\ V_{GS}$$ at which $R_{DS(on)}$ is specified

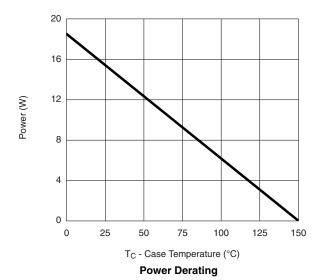
Safe Operating Area, Junction-to-Ambient



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





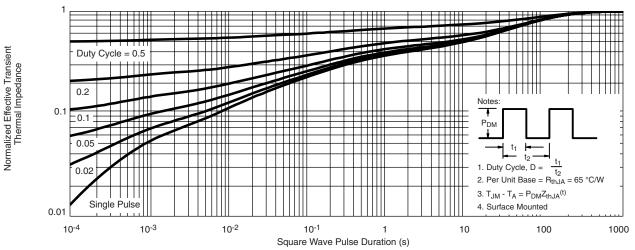
^{*} The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SiA450DJ

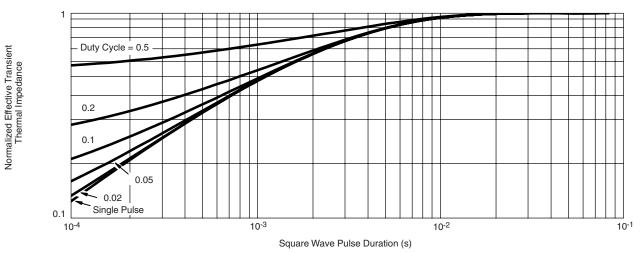
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

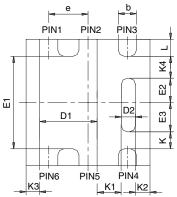
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?73603.

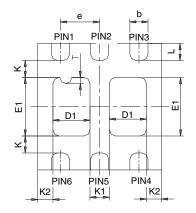




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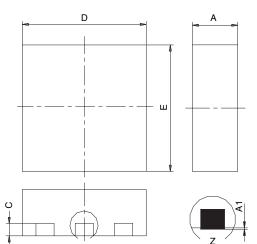
PowerPAK® SC70-6L





BACKSIDE VIEW OF SINGLE

BACKSIDE VIEW OF DUAL



- All dimensions are in millimeters
 Package outline exclusive of mold flash and metal burr
 Package outline inclusive of plating

			SINGL	E PAD		DUAL PAD						
DIM	M	IILLIMETER	RS		INCHES		M	MILLIMETERS			INCHES	
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
Α	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
С	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
Е	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
е		0.65 BSC			0.026 BSC	;	0.65 BSC			0.026 BSC		
K		0.275 TYP 0.011 TYP			0.275 TYP 0.011 TYP							
K1	0.400 TYP 0.016 TYP		0.320 TYP			0.013 TYP						
K2	0.240 TYP 0.009 TYP		0.252 TYP			0.010 TYP						
К3		0.225 TYP	1	0.009 TYP								
K4		0.355 TYP 0.014 TYP										
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
Т							0.05	0.10	0.15	0.002	0.004	0.006
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DETAIL Z

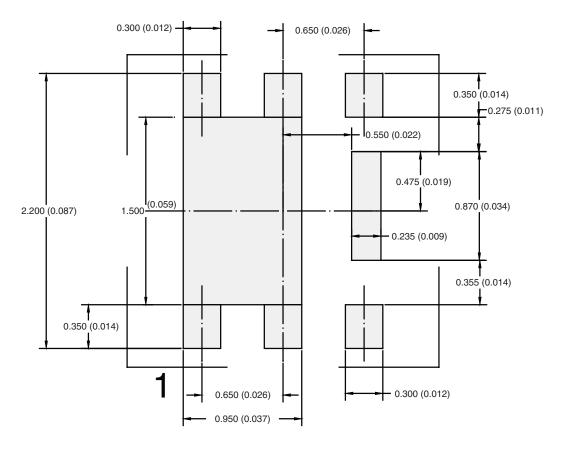
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DWG: 5934

Document Number: 73001 06-Aug-07



RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Single



Dimensions in mm/(Inches)

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ATTLICATION NOT



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