RoHS

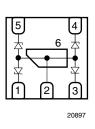
GREEN

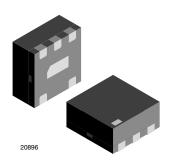
(5-2008)



Vishay Semiconductors

4-Line (Quad) ESD Protection Diode Array in LLP1010-6L





FEATURES

- Ultra compact LLP1010-6L package
- Low package height < 0.4 mm
- 4-line ESD protection (quad)
- Low leakage current < 0.1 μA
- Low load capacitance C_D = 12 pF
- ESD-protection acc. IEC 61000-4-2
 - ± 15 kV contact discharge ± 17 kV air discharge
- Surge current acc. IEC 6100-4-5 I_{PP} > 2.5 A
- Soldering can be checked by standard vision inspection.
 No X-ray necessary
- Pin plating NiPdAu (e4) no whisker growth
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

MARKING (example only)



Dot = pin 1 marking X = date code Y = type code (see table below)

| ORDERING INFORMATION | | | | | | |
|----------------------|--------------------|--|------------------------|--|--|--|
| DEVICE NAME | ORDERING CODE | TAPED UNITS PER REEL (8 mm TAPE ON 7" REEL) | MINIMUM ORDER QUANTITY | | | |
| VESD05A4A-HS4 | VESD05A4A-HS4-GS08 | 5000 | 5000 | | | |

| PACKAGE DATA | | | | | | | |
|---------------|-----------------|--------------|---------|--------------------------------------|--------------------------------------|--------------------------|--|
| DEVICE NAME | PACKAGE NAME | TYPE CODE | WEIGHT | MOLDING COMPOUND FLAMMABILITY RATING | MOISTURE SENSITIVITY LEVEL | SOLDERING CONDITIONS | |
| VESD05A4A-HS4 | LLP1010-6L | Α | 1.07 mg | UL 94 V-0 | MSL level 1 (according J-STD-020) | 260 °C/10 s at terminals | |



| ABSOLUTE MAXI | MUM RATINGS | | | | |
|-----------------------|---|-------------------|--------------------|---------------|------|
| PARAMETER | TEST CONDITIONS | | | VALUE | UNIT |
| Book nulse gurrent | BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6); acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot | | | 2.5 | Α |
| Peak pulse current | BiSy-mode: each input (pin 1, 3 to 5) to any other input pin. Pin 2 and 6 not connected. Acc. IEC 61000-4-5; $t_p = 8/20 \mu s$; single shot | | | 2.5 | Α |
| Pook pulso power | BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and acc. IEC 61000-4-5; t_p = 8/20 μ s; single shot | l 6); | P _{PP} | 30 | W |
| Peak pulse power | BiSy-mode: each input (pin 1, 3 to 5) to any other input pin. Pin 2 and 6 not connected. Acc. IEC 61000-4-5; $t_p = 8/20~\mu s$; single shot | | | 33 | W |
| ESD immunity | Acc. IEC61000-4-2; 10 pulses BiAs-mode: each input (pin 1, 3 to 5) to ground (pin 2 and 6) | Contact discharge | - V _{ESD} | ± 15 | kV |
| | | Air discharge | | ± 17 | kV |
| | Acc. IEC 61000-4-2; 10 pulses BiSy-mode: each input (pin 1, 3 to 5) to any other input pin. Pin 2 and 6 not connected. | Contact discharge | - V _{ESD} | ± 15 | kV |
| | | Air discharge | | ± 17 | kV |
| Operating temperature | Junction temperature | | TJ | - 40 to + 125 | °C |
| Storage temperature | | | T _{STG} | - 55 to + 150 | °C |

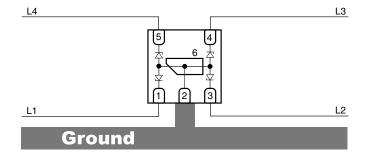
BIAS-MODE (4-LINE BIDIRECTIONAL ASYMMETRICAL PROTECTION MODE)

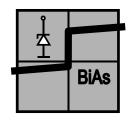
With the VESD05A4A-HS4 up to 4 signal- or data-lines (L1 to L4) can be protected against voltage transients. With pin 2 and 6 connected to ground and pin 1, 3, 4 and 5 connected to a signal- or data-line which has to be protected. As long as the voltage level on the data- or signal-line is between 0 V (ground level) and the specified Maximum Reverse Working Voltage (V_{RWM}) the protection diode between data line and ground offer a high isolation to the ground line. The protection device behaves like an open switch.

As soon as any positive transient voltage signal exceeds the break through voltage level of the protection diode, the diode becomes conductive and shorts the transient current to ground. Now the protection device behaves like a closed switch. The Clamping Voltage (V_C) is defined by the BReakthrough Voltage (V_{BR}) level plus the voltage drop at the series impedance (resistance and inductance) of the protection device.

Any negative transient signal will be clamped accordingly. The negative transient current is flowing in the forward direction of the protection diode. The low Forward Voltage (V_F) clamps the negative transient close to the ground level.

Due to the different clamping levels in forward and reverse direction the VESD05A4A-HS4 clamping behaviour is Bidirectional and Asymmetrical (BiAs).





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2.5

15

8.5

12

7.5

٧

рF

рF

| ELECTRICAL CHARACTERISTICS BiAs mode: each input (pin 1, 3, 4 and 5) to ground (pin 2 and/or 6) (T _{amb} = 25 °C, unless otherwise specified) | | | | | | |
|---|--|----------------------|------|--------|------|-------|
| PARAMETER | TEST CONDITIONS/REMARKS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Protection paths | Number of lines which can be protected | N _{channel} | - | - | 4 | lines |
| Reverse stand-off voltage | Max. reverse working voltage | V_{RWM} | - | - | 5 | V |
| Reverse voltage | at I _R = 0.1 μA | V_R | 5 | - | - | V |
| Reverse current | at V _{RWM} = 5 V | I _R | - | < 0.01 | 0.1 | μA |
| Reverse breakdown voltage | at I _R = 1 mA | V_{BR} | 6 | =. | 8 | V |
| Reverse clamping voltage | at I _{PP} = 2.5 A | V _C | - | - | 12 | V |

If a higher surge current or peak pulse current (I_{PP}) is needed, some protection diodes in the VESD05A4A-HS4 can also be used in parallel in order to "multiply" the performance.

 V_{F}

 C_D

at $I_{PP} = 2.5 A$

at V_R = 0 V; f = 1 MHz

at $\overline{V_R} = 2.5 \text{ V}$; f = 1 MHz

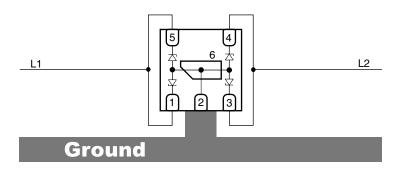
If two diodes are switched in parallel you get

- double surge power = double peak pulse current (2 x I_{PPM})
- half of the line inductance = reduced clamping voltage
- half of the line resistance = reduced clamping voltage
- double line Capacitance (2 x C_D)

Forward clamping voltage

Capacitance

• double Reverse leakage current (2 x I_R)



20900

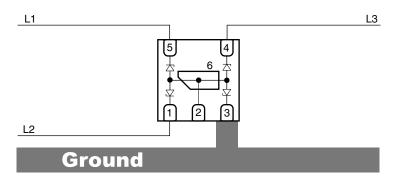


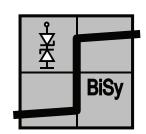
BISY-MODE (3-LINE BIDIRECTIONAL SYMMETRICAL PROTECTION MODE)

If a bipolar symmetrical protection device is needed the VESD05A4A-HS4 can also be used as a three-line protection device. Therefore three pins (example: pin 1, 3, and 5) has to be connected to the signal- or data-line (L1 to L3) and pin 3 to ground. Pin 2 and 6 must not be connected!

Positive and negative voltage transients will be clamped in the same way. The clamping current from one data line through the VESD05A4A-HS4 to the ground passes one diode in forward direction and the other one in reverse direction. The Clamping Voltage (V_C) is defined by the BReakthrough Voltage (V_{BR}) level of one diode plus the forward voltage of the other diode plus the voltage drop at the series impedances (resistances and inductances) of the protection device.

Due to the same clamping levels in positive and negative direction the VESD05A4A-HS4 voltage clamping behaviour is also Bidirectional and Symmetrical (BiSy).





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ELECTRICAL CHARACTERISTICS

BiSy mode: pin 1, 3, 4 or 5 to any other pin (1, 3, 4 or 5) (pin 2 and 6 not connected) (T_{amb} = 25 °C, unless otherwise specified)

| , | | | | | | |
|---------------------------|--|----------------------|------|--------|------|-------|
| PARAMETER | TEST CONDITIONS/REMARKS | SYMBOL | MIN. | TYP. | MAX. | UNIT |
| Protection paths | Number of lines which can be protected | N _{channel} | - | - | 3 | lines |
| Reverse stand-off voltage | Max. reverse working voltage | V_{RWM} | - | - | 5.5 | V |
| Reverse voltage | at I _R = 0.1 μA | V_R | 5.5 | - | - | V |
| Reverse current | at V _R = V _{RWM} = 5.5 V | I _R | - | < 0.01 | 0.1 | μΑ |
| Reverse breakdown voltage | at I _R = 1 mA | V_{BR} | 6.5 | - | 8.7 | V |
| Clamping voltage | at I _{PP} = 2.5 A | V _C | - | 11.5 | 13 | V |
| Capacitance | at $V_R = 0 V$; $f = 1 MHz$ | C_D | - | 6 | 8 | pF |
| | at V _R = 2.5 V; f = 1 MHz | | - | 5 | 7 | pF |



TYPICAL CHARACTERISTICS (T_{amb} = 25 °C, unless otherwise specified)

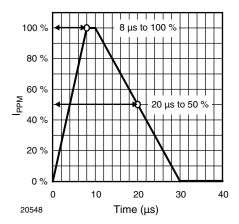


Fig. 1 - 8/20 µs Peak Pulse Current Wave Form acc. IEC 61000-4-5

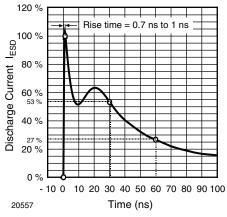


Fig. 2 - ESD Discharge Current Wave Form acc. IEC 61000-4-2 (330 Ω /150 pF)

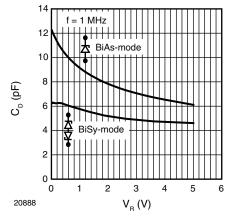


Fig. 3 - Typical Capacitance CD vs. Reverse Voltage VR

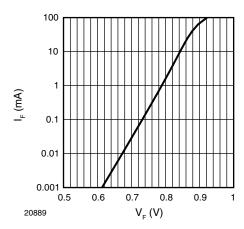


Fig. 4 - Typical Forward Current I_F vs. Forward Voltage V_F

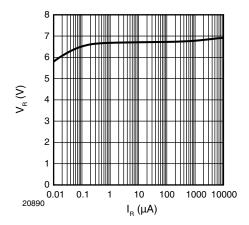


Fig. 5 - Typical Reverse Voltage V_R vs. Reverse Current I_R

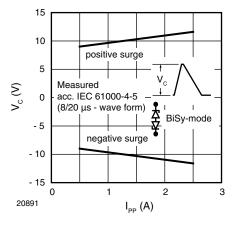


Fig. 6 - Typical Peak Clamping Voltage V_{C} vs. Peak Pulse Current IPP

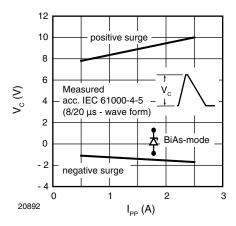


Fig. 7 - Typical Peak Clamping VoltageV $_{\rm C}$ vs. Peak Pulse Current I $_{\rm PP}$

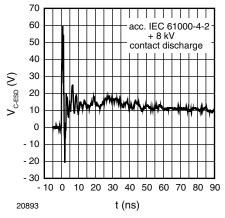


Fig. 8 - Typical Clamping Performance at + 8 kV Contact Discharge (acc. IEC 61000-4-2)

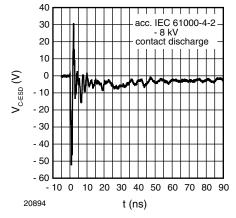


Fig. 9 - Typical Clamping Performance at - 8 kV Contact Discharge (acc. IEC 61000-4-2)

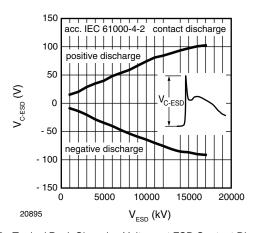
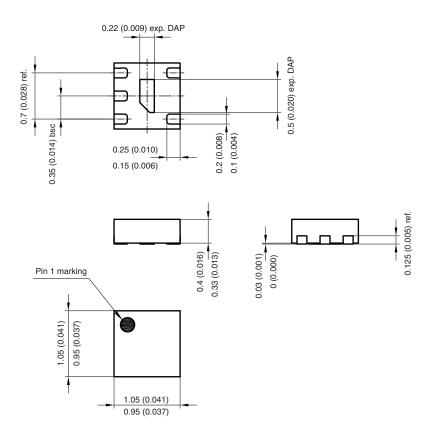
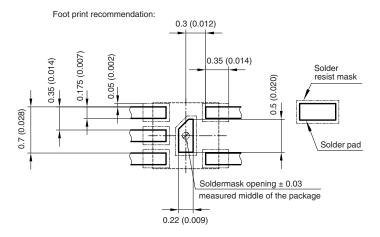


Fig. 10 - Typical Peak Clamping Voltage at ESD Contact Discharge (acc. IEC 61000-4-2)

PACKAGE DIMENSIONS in millimeters (inches): LLP1010-6L





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Vishay

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