AK4342

24-Bit Stereo DAC with HP-AMP & 2V Line-Out

GENERAL DESCRIPTION

The AK4342 is a 24-bit stereo DAC with 2Vrms lineout, an integrated headphone amplifier, and an auxiliary line output. The AK4342 features an analog mixing circuit that enables a simple interface to external analog audio sources. The integrated headphone amplifier features "click-free" power-on/off, a mute control and delivers 62.5mW of power at 16Ω @ 3.3V. The AK4342 is controlled via an I^2C or 3-wire interface, and is available in a 32-pin QFN package.

FEATURE

- ☐ **Multi-bit 24-bit ΔΣ DAC**
- ☐ **Sampling Rate: 8kHz to 96kHz**
- ☐ **8 times Oversampling FIR interpolator**
  - **Passband: 20kHz**
  - **Passband Ripple: ±0.02dB**
  - **Stopband Attenuation: 54dB**
- ☐ **Audio I/F Format: MSB First, 2's Complement**
  - **I^2S, 24bit MSB justified, 24bit/20bit/16bit LSB justified**
- ☐ **Master Clock:**
  - **Normal Speed Mode: 256fs/384fs/512fs/768fs**
  - **Double Speed Mode: 128fs/192fs/256fs/384fs**
  - **Half Speed Mode: 512fs/768fs**
- ☐ **Digital De-emphasis Filter: 32kHz, 44.1kHz and 48kHz**
- ☐ **Analog volume control:**
  - **Headphone: +6dB to – 48dB, Variable Step Size**
  - **Lineout: 0dB to – 31dB, 1dB step**
- ☐ **Digital Linear Attenuator**
- ☐ **Digital Soft Mute**
- ☐ **Analog Mixing Circuit**
- ☐ **µP Interface: 3-wire/I^2C (400kHz mode)**
- ☐ **Pop Noise Free at Power-ON/OFF and Mute**
- ☐ **DAC Performance (Lineout)**
  - **THD+N: -88dB**
  - **Dynamic Range: 100dB**
  - **Output Level: 2Vrms**
- ☐ **DAC Performance (Aux-Out)**
  - **THD+N: -87dB**
  - **Dynamic Range: 95dB**
- ☐ **Headphone Amplifier (Cap-less)**
  - **Output Power: 62.5mW x 2ch @16Ω, 3.3V**
  - **THD+N: -60dB @ 25mW**
  - **Dynamic Range: 95dB**
- ☐ **Power Supply:**
  - **DAC & Output Buffers: 2.7V ~ 3.6V**
  - **Digital Interface: 1.6V ~ 3.6V**
- ☐ **Power Supply Current: 30.5mA (Headphone amp off)**
- ☐ **Ta: –30 ~ 85°C**
- ☐ **Package: 32pin QFN**

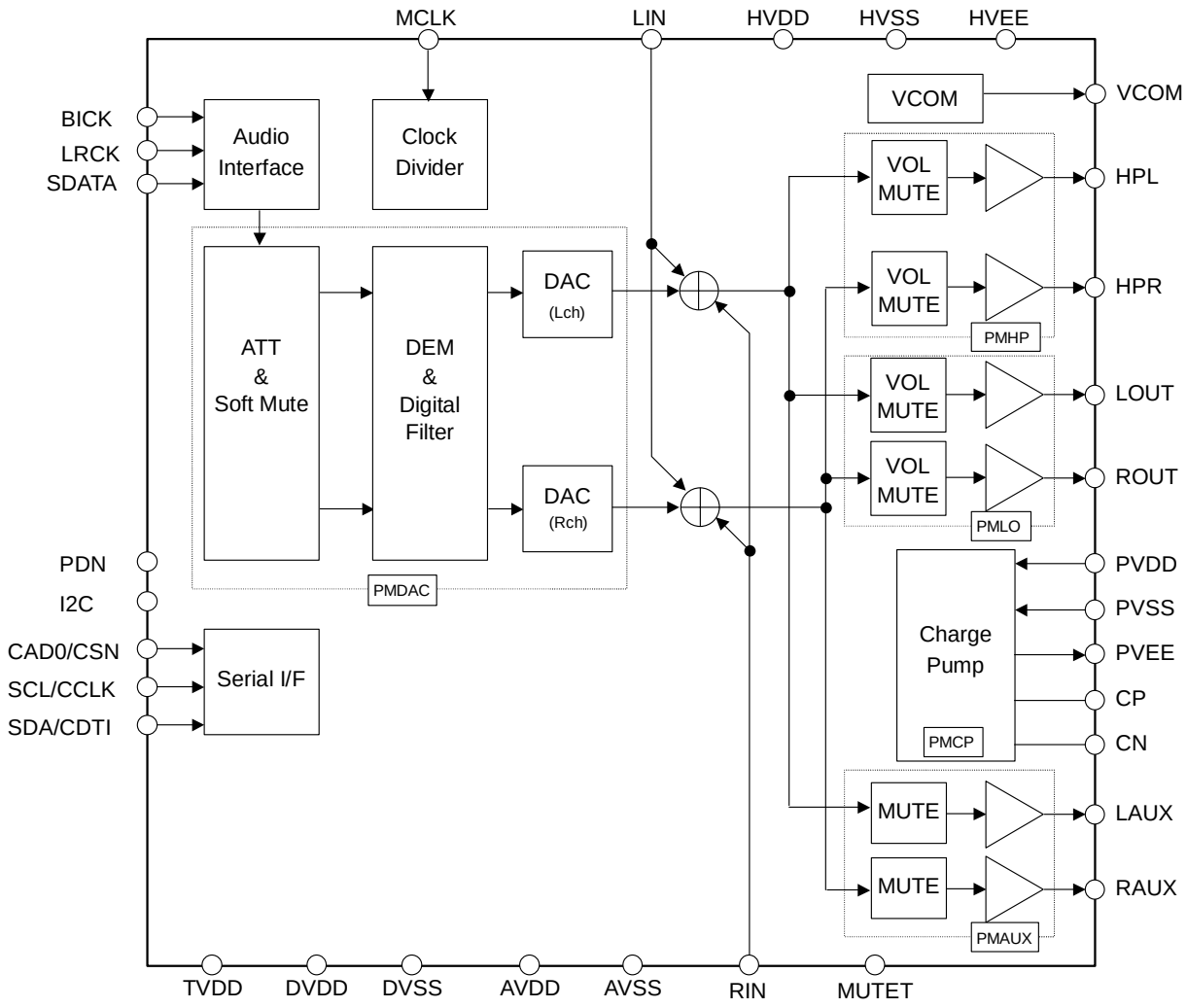
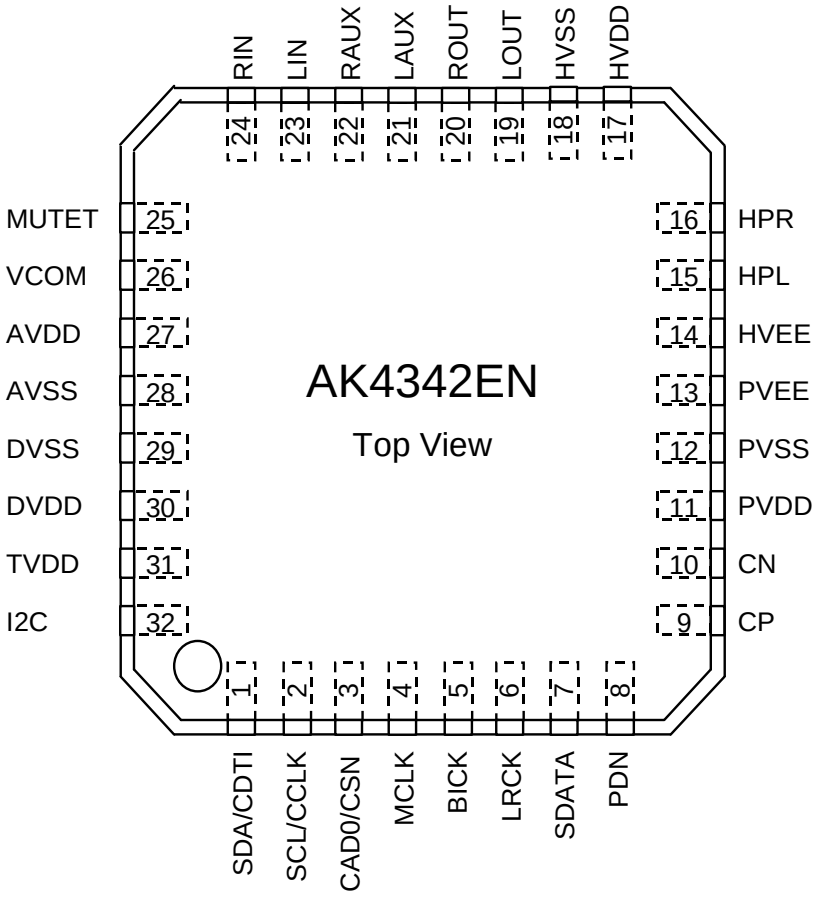


Figure 1. AK4342 Block Diagram

■ Ordering Guide

AK4342EN	–30 ~ +85°C	32pin QFN (0.5mm pitch)
AKD4342	Evaluation board for AK4342	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SDA	I/O	Control Data Input/Output Pin (I2C pin = "H") An external pull-up resister is required.
	CDTI	I	Control Data Input Pin (I2C pin = "L")
2	SCL	I	Control Data Clock Pin (I2C pin = "H") An external pull-up resistor is required.
	CCLK	I	Control Data Clock Pin (I2C pin = "L")
3	CAD0	I	Chip Address 0 Select Pin (I2C pin = "H") (Internal Pull-up Pin to TVDD pin)
	CSN	I	Control Data Chip Select Pin (I2C pin = "L") (Internal Pull-up Pin to TVDD pin)
4	MCLK	I	Master Clock Input Pin
5	BICK	I	Serial Bit Clock Pin This clock is used to latch audio data.
6	LRCK	I	L/R Clock Pin This clock determines which audio channel is currently being input on SDATA pin.
7	SDATA	I	Audio Serial Data Input Pin
8	PDN	I	Power-down & Reset Pin When at "L", the AK4342 is in power-down mode and is held in reset. The AK4342 must be reset once upon power-up.
9	CP	O	Positive Charge Pump Capacitor Terminal Pin
10	CN	I	Negative Charge Pump Capacitor Terminal Pin
11	PVDD	-	Charge Pump Circuit Positive Power Supply Pin
12	PVSS	-	Charge Pump Circuit Ground Pin
13	PVEE	O	Charge Pump Circuit Negative Voltage Output Pin
14	HVEE	-	Headphone Amp Negative Power Supply Pin Connected to PVEE pin
15	HPL	O	Lch Headphone Amp Output Pin
16	HPR	O	Rch Headphone Amp Output Pin
17	HVDD	-	Headphone Amp Positive Power Supply Pin
18	HVSS	-	Headphone Amp Ground Pin
19	LOUT	O	Lch Lineout Output Pin
20	ROUT	O	Rch Lineout Output Pin
21	LAUX	O	Lch Auxiliary Output Pin
22	RAUX	O	Rch Auxiliary Output Pin
23	LIN	I	Lch Analog Input Pin
24	RIN	I	Rch Analog Input Pin
25	MUTET	O	Mute Time Constant Control Pin Connected to AVSS pin through a 1μF capacitor for mute time constant.
26	VCOM	O	Common Voltage Output Pin Normally connected to AVSS pin with 0.1μF ceramic capacitor in parallel with a 2.2μF electrolytic capacitor.
27	AVDD	-	Analog Power Supply Pin
28	AVSS	-	Analog Ground Pin
29	DVSS	-	Digital Ground Pin
30	DVDD	-	Digital Power Supply Pin
31	TVDD	-	Digital Interface Power Supply Pin
32	I2C	I	Control Mode Select Pin (Internal Pull-up Pin to TVDD pin) "H": I^2C Bus, "L": 3-wire Serial

Note: Do not allow digital input pins except analog input pins (RIN and LIN) and internal pull-up pins (CAD0/CSN and I2C) to float.

■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Analog	MUTET, HPL, HPR, LOUT, ROUT, LAUX, RAUX, RIN, LIN	These pins should be open.

ABSOLUTE MAXIMUM RATING

(AVSS, DVSS, HVSS, PVSS = 0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	–0.3	4.0	V
	Digital	DVDD	–0.3	4.0	V
	HP-Amp	HVDD	–0.3	4.0	V
	Charge Pump	PVDD	–0.3	4.0	V
	Digital I/F	TVDD	–0.3	4.0	V
	|AVSS – DVSS | (Note 2)	ΔGND1		0.3	V
	|AVSS – HVSS | (Note 2)	ΔGND2		0.3	V
	|AVSS – PVSS | (Note 2)	ΔGND3		0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		AVIN	–0.3	AVDD+0.3 or 4.0	V
Digital Input Voltage (Note 4)		DVIN	–0.3	TVDD+0.3 or 4.0	V
Ambient Temperature		Ta	–30	85	°C
Storage Temperature		Tstg	–65	150	°C
Maximum Power Dissipation (Note 5)		Pd	-	700	mW

Note 1. All voltages with respect to ground.

Note 2. AVSS, DVSS, HVSS and PVSS must be connected to the same analog plane.

Note 3. LIN and RIN pins. The maximum value is low value either “AVDD+0.3V” or “4.0V”.

Note 4. MCLK, BICK, LRCK, SDATA, CAD0/CSN, SCL/CCLK, SDA/CDTI, I2C and PDN pins. The maximum value is low value either “TVDD+0.3V” or “4.0V”.
Pull-up resistors at SDA and SCL pins should be connected to (TVDD+0.3)V or less voltage.

Note 5. In case that PCB wiring density is 100%. This power is the AK4342 internal dissipation that does not include power of externally connected headphone.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(AVSS, DVSS, HVSS, PVSS = 0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies	Analog	AVDD	2.7	3.3	3.6	V
(Note 6)	Digital	DVDD	2.7	3.3	3.6	V
	HP-Amp	HVDD	2.7	3.3	3.6	V
	Charge Pump	PVDD	2.7	3.3	3.6	V
	Digital I/F	TVDD	1.6	1.8	DVDD	V
	Difference	DVDD – AVDD	-0.3	0	0.3	V
		DVDD – HVDD	-0.3	0	0.3	V
		DVDD – PVDD	-0.3	0	0.3	V

Note 1. All voltages with respect to ground.

Note 6. Power up sequence among AVDD, DVDD, HVDD, PVDD and TVDD is not critical. But PDN pin must keep “L” until all power supply pins are applied. After that, PDN pin should be set to “H”. Each power supply cannot be partially powered OFF.

* AKM assumes no responsibility for usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=HVDD=PVDD=3.3V, TVDD=1.8V, AVSS=DVSS=HVSS=PVSS=0V; fs=44.1kHz; Signal Frequency =1kHz; Measurement band width=10Hz ~ 20kHz; Headphone-Amp: R_L =16Ω; Line output: R_L =10kΩ, Aux output: R_L =10kΩ; Charge Pump Circuit External Capacitance: C1=C2= 2.2μF (see Figure 2); unless otherwise specified)

Parameter			min	typ	max	Units
DAC Resolution			-	-	24	bit
LINEIN: (LIN/RIN pins)						
Analog Input Characteristics:						
Maximum Input Voltage (Note 7)			-	-	1.98	Vpp
Feedback Resistance			14	20	26	kΩ
Gain (LIN/RIN pins: External resistor = 20kΩ) (Note 8)						
Vin = 1Vpp	LIN/RIN → HPL/HPR (Note 9)		–1.5	1.5	4.5	dB
	LIN/RIN → LOUT/ROUT (Note 10)		4.5	7.5	10.5	dB
	LIN/RIN → LAUX/RAUX		–4.7	–1.7	1.3	dB
Headphone-Amp: (DAC → HPL/HPR pins) (Note 11)						
Analog Output Characteristics						
THD+N	fs=44.1kHz	0dBFS Output, Po=62.5mW	-	–40	-	dB
	BW=20kHz	–4dBFS Output, Po=25mW	-	–60	–50	dB
	fs=96kHz	0dBFS Output, Po=62.5mW	-	–40	-	dB
	BW=40kHz	–4dBFS Output, Po=25mW	-	–60	–50	dB
Dynamic Range (–60dBFS Output, A-weighted)			87	95	-	dB
S/N (A-weighted)			87	95	-	dB
Interchannel Isolation			60	80	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.2	1.0	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance			16	-	-	Ω
Load Capacitance			-	-	300	pF
Output Voltage (0dBFS Output) (Note 12)			0.9	1.0	1.1	Vrms
Line Output: (DAC → LOUT/ROUT pins) (Note 13)						
Analog Output Characteristics						
THD+N	fs=44.1kHz	0dBFS Output	-	–88	–78	dB
	BW=20kHz	-60dBFS Output	-	–37	-	dB
	fs=96kHz	0dBFS Output	-	–88	–78	dB
	BW=40kHz	-60dBFS Output	-	–35	-	dB
Dynamic Range (–60dBFS Output, A-weighted)			92	100	-	dB
S/N (A-weighted)			92	100	-	dB
Interchannel Isolation			80	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.2	0.8	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance			10	-	-	kΩ
Load Capacitance (C3 in Figure 3)			-	-	25	pF
Output Voltage (Note 14)			1.8	2.0	2.2	Vrms

Note 7. Maximum Input Voltage of LIN/RIN pins is proportional to AVDD voltage. Since the internal feedback resistor is 20kΩ±30%, the external resistor should determine that the value does not exceed the maximum input voltage.
Note 8. The gain is inverse proportion to external input resistance.
Note 9. PGAL4-0=PGAR4-0= 0dB
Note 10. LPGA4-0= 0dB
Note 11. PMVCM=PMCP=PMDAC=PMHP bits = "1", PMLO=PMAUX bits= "0", LINL=LINR=RINL=RINR bits = "0", ATTL7-0=ATTR7-0= 0dB, PGAL4-0=PGAR4-0= 0dB.
Note 12. Output voltage is proportional to AVDD voltage. Vout (typ.) = 0.303 x AVDD [Vrms] @ 0dBFS
Note 13. PMVCM=PMCP=PMDAC=PMLO bits = "1", PMHP=PMAUX bits= "0", LINL=LINR=RINL=RINR bits = "0", ATTL7-0=ATTR7-0= 0dB, LPGA4-0= 0dB.
Note 14. Output voltage is proportional to AVDD voltage. Vout (typ.) = 0.606 x AVDD [Vrms] @ 0dBFS

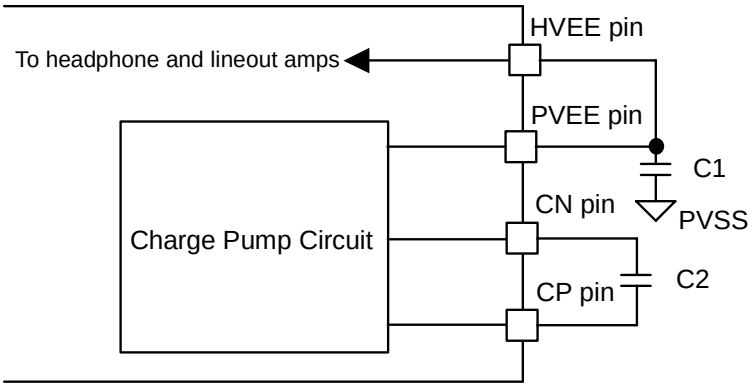


Figure 2. Charge Pump Circuit External Capacitor

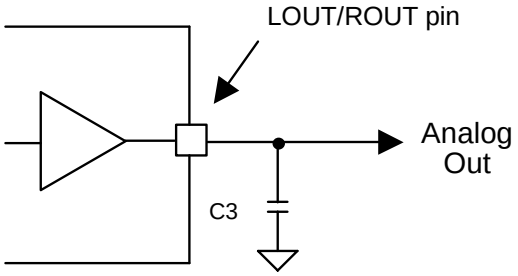


Figure 3. Line out circuit example

Parameter			min	typ	max	Units
Aux Output: (DAC → LAUX/RAUX pins) (Note 15)						
Analog Output Characteristics						
THD+N	fs=44.1kHz	0dBFS Output	-	–87	–77	dB
	BW=20kHz	–60dBFS Output	-	–32	-	dB
	fs=96kHz	0dBFS Output	-	–87	–77	dB
	BW=40kHz	–60dBFS Output	-	–30	-	dB
Dynamic Range (–60dBFS Output, A-weighted)			87	95	-	dB
S/N (A-weighted)			87	95	-	dB
Interchannel Isolation			80	100	-	dB
DC Accuracy						
Interchannel Gain Mismatch			-	0.2	0.8	dB
Gain Drift			-	200	-	ppm/°C
Load Resistance		(Note 16)	10	-	-	kΩ
Load Capacitance		(C4 in Figure 4)	-	-	25	pF
Output Voltage		(Note 17)	0.63	0.70	0.77	Vrms
Output Volume for Headphone-amp (PGAL, PGAR):						
Step Size	+6dB to –10dB		0.1	1	1.9	dB
	–10dB to –32dB		0.1	2	3.9	dB
	–32dB to –48dB		0.1	4	7.9	dB
Output Volume for Lineout-amp (LPGA):						
Step Size	0dB to –31dB		0.1	1	1.9	dB
Power Supplies						
Power Supply Current						
Normal Operation (PDN pin = "H")		(Note 18)				
AVDD+HVDD+PVDD			-	28	45	mA
DVDD+TVDD (fs = 44.1kHz)			-	2.5	4	mA
DVDD+TVDD (fs = 96kHz)			-	3.5	5.5	mA
Power-Down Mode (PDN pin = "L")		(Note 19)				
AVDD+HVDD+PVDD+DVDD+TVDD			-	10	100	μA

Note 15. PMVCM=PMDAC=PMAUX bits = "1", PMHP=PMLO bits= "0", LINL=LINR=RINL=RINR bits = "0", ATTL7-0=ATTR7-0= 0dB

Note 16. For AC load

Note 17. Output voltage is proportional to AVDD voltage. Vout (typ) = 0.212 x AVDD [Vrms] @ 0dBFS

Note 18. PMVCM=PMDAC=PMHP=PMLO=PMAUX bits = "1" and HP-Amp output is off.

Note 19. All digital input pins including clock pins (MCLK, BICK and LRCK) except I2C and CSN/CAD0 pins are held at DVSS. I2C and CSN/CAD0 pins are held at TVDD.

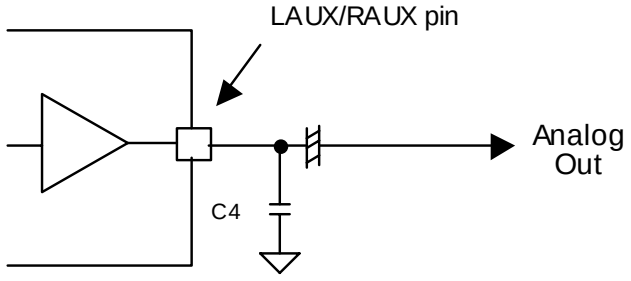


Figure 4. Aux-out circuit example

FILTER CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD, PVDD=2.7 ~ 3.6V, TVDD=1.6 ~ 3.6V; fs=44.1kHz; De-emphasis = "OFF")

Parameter		Symbol	min	typ	max	Units
DAC Digital Filter:						
Passband	±0.05dB (Note 20)	PB	0	-	20.0	kHz
	–6.0dB		-	22.05	-	kHz
Stopband (Note 20)		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.02	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay (Note 21)		GD	-	21	-	1/fs
Group Delay Distortion		ΔGD	-	0	-	μs
Digital Filter + Analog Filter: (Note 22)						
Frequency Response	20.0kHz (fs=44.1kHz)	FR	-	–0.5	-	dB
	40.0kHz (fs=96kHz)	FR	-	–1.5	-	dB
Analog Filter: (Note 23)						
Frequency Response	20.0kHz	FR	-	±1.0	-	dB
	40.0kHz	FR	-	±1.0	-	dB

Note 20. The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@±0.05dB), SB=0.546*fs(@–54dB).

Note 21. Delay time caused by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

Note 22. DAC → HPL/HPR/LOUT/ROUT/LAUX/RAUX

Note 23. LIN → HPL/LOUT/LAUX, RIN → HPR/ROUT/RAUX

DC CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD, PVDD=2.7 ~ 3.6V; TVDD=1.6 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
High-Level Input Voltage	(2.7V ≤ TVDD ≤ 3.6V)	VIH	70%TVDD	-	-	V
	(1.6V ≤ TVDD < 2.7V)	VIH	80%TVDD	-	-	V
Low-Level Input Voltage	(2.7V ≤ TVDD ≤ 3.6V)	VIL	-	-	30%TVDD	V
	(1.6V ≤ TVDD < 2.7V)	VIL	-	-	20%TVDD	V
Low-Level Output Voltage (Iout = 3mA)		VOL	-	-	0.4	V
Input Leakage Current (Note 24)		Iin	-	-	±10	μA

Note 24. Except I2C and CSN/CAD0 pins. These pins have internal pull-up device, nominally 100kΩ.

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD, DVDD, HVDD, PVDD=2.7 ~ 3.6V; TVDD=1.6 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
Master Clock Timing (2.7V ≤ TVDD ≤ 3.6V)					
Half Speed Mode (512/768fs)	fCLK	4.096		18.432	MHz
Normal Speed Mode (256/384/512/768fs)	fCLK	2.048		36.864	MHz
Double Speed Mode (128/192/256/384fs)	fCLK	6.144		36.864	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
Master Clock Timing (1.6V ≤ TVDD < 2.7V)					
Half Speed Mode (512/768fs)	fCLK	4.096		18.432	MHz
Normal Speed Mode (256/384fs)	fCLK	2.048		18.432	MHz
Double Speed Mode (128/192fs)	fCLK	6.144		18.432	MHz
Pulse Width Low	tCLKL	0.4/fCLK	-	-	ns
Pulse Width High	tCLKH	0.4/fCLK	-	-	ns
LRCK Timing					
Frequency					
Half Speed Mode (DFS1-0 bits = "10")	fsh	8		24	kHz
Normal Speed Mode (DFS1-0 bits = "00")	fsn	8		48	kHz
Double Speed Mode (DFS1-0 bits = "01")	fsd	60		96	kHz
Duty Cycle	Duty	45	-	55	%
Serial Interface Timing (Note 25)					
BICK Period					
Half Speed Mode	tBCK	1/128fsh	-	-	ns
Normal Speed Mode	tBCK	1/128fsn	-	-	ns
Double Speed Mode	tBCK	1/64fsd	-	-	ns
BICK Pulse Width Low	tBCKL	70	-	-	ns
Pulse Width High	tBCKH	70	-	-	ns
LRCK Edge to BICK "↑" (Note 26)	tLRB	40	-	-	ns
BICK "↑" to LRCK Edge (Note 26)	tBLR	40	-	-	ns
LRCK Edge to BICK "↓" (Note 27)	tLRB	40	-	-	ns
BICK "↓" to LRCK Edge (Note 27)	tBLR	40	-	-	ns
SDATA Hold Time	tSDH	40	-	-	ns
SDATA Setup Time	tSDS	40	-	-	ns
Control Interface Timing (3-wire Serial mode)					
CCLK Period	tCCK	200	-	-	ns
CCLK Pulse Width Low	tCCKL	80	-	-	ns
Pulse Width High	tCCKH	80	-	-	ns
CDTI Setup Time	tCDS	40	-	-	ns
CDTI Hold Time	tCDH	40	-	-	ns
CSN "H" Time	tCSW	150	-	-	ns
CSN "↓" to CCLK "↑"	tCSS	50	-	-	ns
CCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Power-down & Reset Timing					
PDN Pulse Width (Note 28)	tPD	150	-	-	ns

Note 25. Refer to "Serial Data Interface".
Note 26. When BCKP bit is set to "0", BICK rising edge must not occur at the same time as LRCK edge.
Note 27. When BCKP bit is set to "1", BICK falling edge must not occur at the same time as LRCK edge.
Note 28. The AK4342 can be reset by bringing PDN pin = "L" to "H" only upon power up.

SWITCHING CHARACTERISTICS (Continued)

(Ta=25°C; AVDD, DVDD, HVDD, PVDD=2.7 ~ 3.6V; TVDD=2.7 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
Control Interface Timing (I^2C Bus mode): (Note 29)					
SCL Clock Frequency	fSCL	-	-	400	kHz
Bus Free Time Between Transmissions	tBUF	1.3	-	-	μs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6	-	-	μs
Clock Low Time	tLOW	1.3	-	-	μs
Clock High Time	tHIGH	0.6	-	-	μs
Setup Time for Repeated Start Condition	tSU:STA	0.6	-	-	μs
SDA Hold Time from SCL Falling (Note 30)	tHD:DAT	0		-	μs
SDA Setup Time from SCL Rising	tSU:DAT	0.1	-	-	μs
Rise Time of Both SDA and SCL Lines	tR	-	-	0.3	μs
Fall Time of Both SDA and SCL Lines	tF	-	-	0.3	μs
Setup Time for Stop Condition	tSU:STO	0.6	-	-	μs
Capacitive load on bus	Cb	-		400	pF
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0	-	50	ns

Note 29. I^2C is a registered trademark of Philips Semiconductors.

TVDD voltage must be 2.7V ~ 3.6V in I^2C mode.

Note 30. Data must be held long enough to bridge the 300ns-transition time of SCL.

■ Timing Diagram

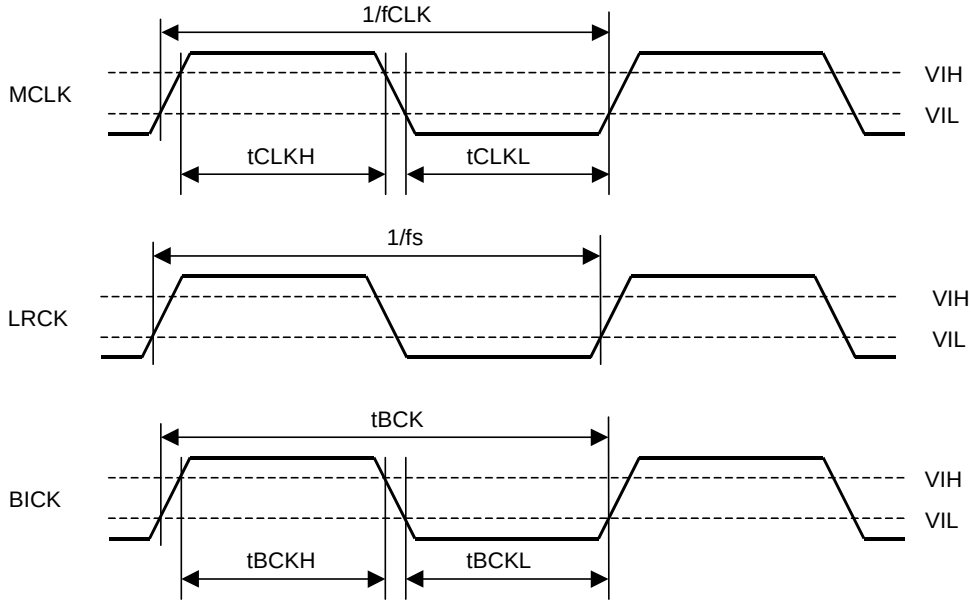


Figure 5. Clock Timing

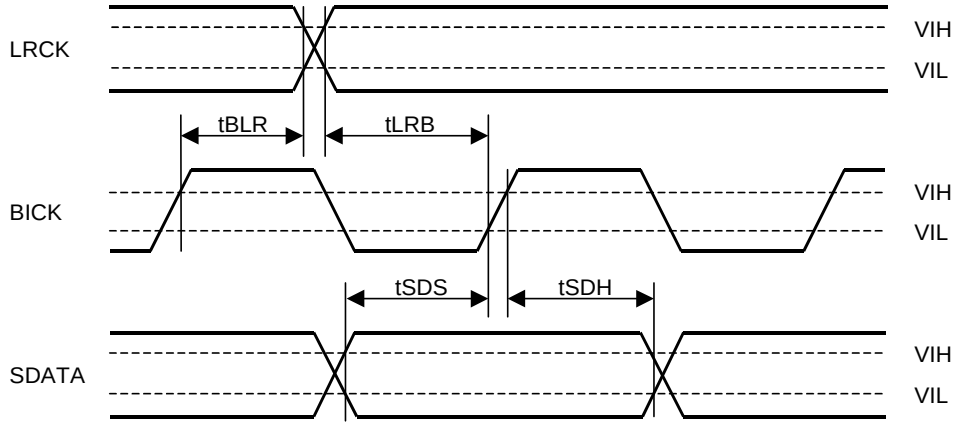


Figure 6. Serial Interface Timing (BCKP bit = “0”)

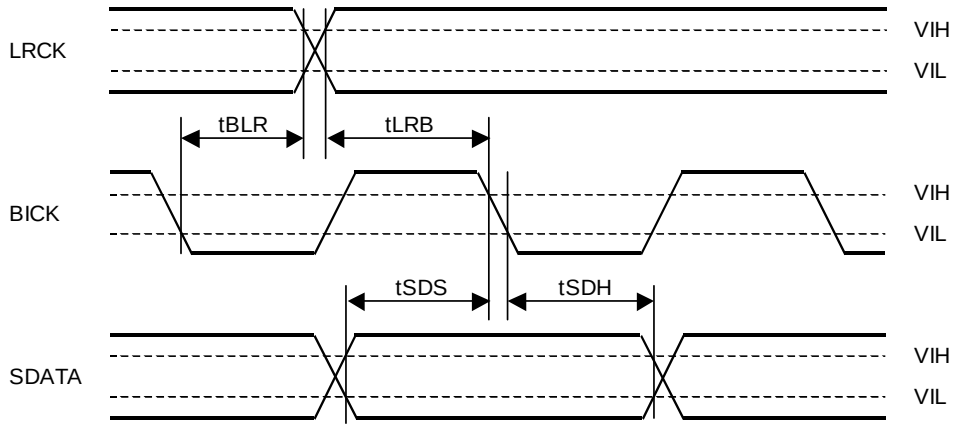


Figure 7. Serial Interface Timing (BCKP bit = "1")

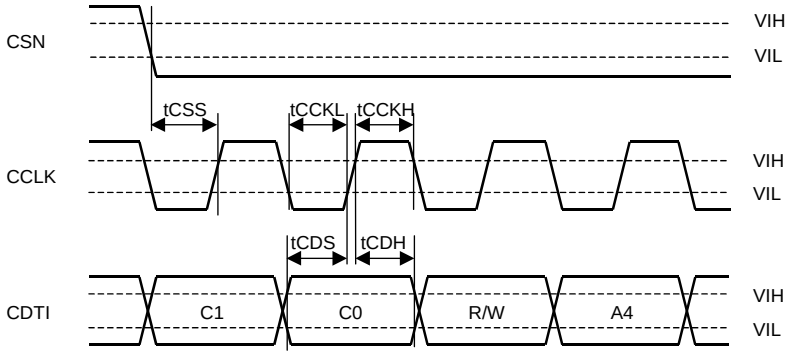


Figure 8. WRITE Command Input Timing

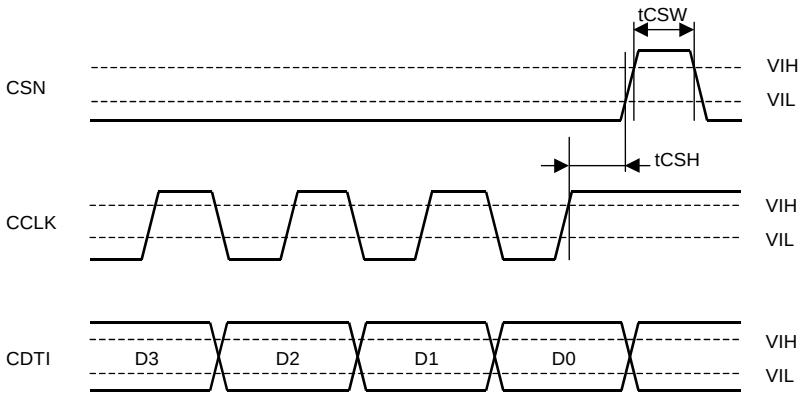


Figure 9. WRITE Data Input Timing

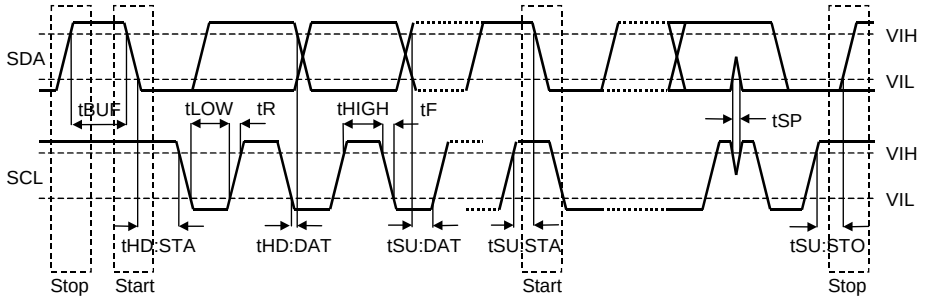


Figure 10. I^{2}C Bus Mode Timing

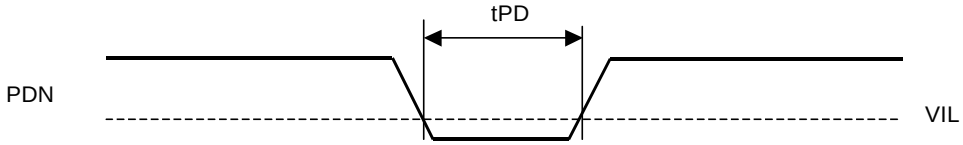


Figure 11. Power-down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks required to operate the AK4342 are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter, delta-sigma modulator, charge pump circuit and counter for transition time. The MCLK frequency is detected from the relation between MCLK and LRCK automatically. The Half speed, the Normal speed and the Double speed mode are selected with the DFS1-0 pins (Table 1). The sampling frequency is selected with the FS3-0 bits. (Table 2)

When the states of DFS1-0 bits change in the normal operation mode, the AK4342 should be reset by PDN pin or PMDAC bit.

DFS1 bit	DFS0 bit	Mode	fs	MCLK Frequency	
0	0	Normal Speed	8 ~ 48kHz	256/384/512/768fs	Default
0	1	Double Speed	60 ~ 96kHz	128/192/256/384fs	
1	0	Half Speed	8 ~ 24kHz	512/768fs	
1	1	Reserve			

Table 1. System Clock Example

FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	
0	0	0	0	44.1kHz	Default
0	0	0	1	32kHz	
0	0	1	0	48kHz	
0	0	1	1	(Reserve)	
0	1	0	0	88.2kHz	
0	1	0	1	64kHz	
0	1	1	0	96kHz	
0	1	1	1	(Reserve)	
1	0	0	0	22.05kHz	
1	0	0	1	16kHz	
1	0	1	0	24kHz	
1	0	1	1	(Reserve)	
1	1	0	0	11.025kHz	
1	1	0	1	8kHz	
1	1	1	0	12kHz	
1	1	1	1	(Reserve)	

Table 2. Set up of Sampling Frequency

For low sampling rates, DR and S/N degrade because of the out-of-band noise. DR and S/N are improved by setting the half speed mode (DFS1-0 bits = “10”)

Mode	S/N (fs=8kHz, 20kLPF + A-weighted)		
	Lineout	Headphone	Aux-out
Normal Speed	89dB	87dB	87dB
Half Speed	99dB	95dB	95dB

Table 3. Relationship between Clock Mode and S/N of Lineout, Headphone and Aux-out

External clocks (MCLK, BICK and LRCK) should always be present whenever the DAC, headphone amp, lineout amp or charge pump circuits is in normal operation mode (PMDAC bit = “1”, PMHP bit = “1”, PMLO bit = “1” or PMCP bit = “1”). If these clocks are not provided, the AK4342 is not operated normally, especially, DAC may draw excess current due to dynamic refresh of internal logic. If the external clocks are not present, the DAC, headphone amp, charge pump circuit and lineout amp should be in the power-down mode (PMDAC bit = PMHP bit = PMLO bit = PMCP bit = “0”).

■ Serial Data Interface

The AK4342 interfaces with external system via the SDATA, BICK and LRCK pins. Five data formats are supported and are selected by the DIF2, DIF1 and DIF0 bits (Table 4). Mode 0 is compatible with existing 16bit DACs and digital filters. Mode 1 is a 20bit version of Mode 0. Mode 4 is a 24bit version of Mode 0. Mode 2 is similar to AKM ADCs and many DSP serial ports. Mode 3 is compatible with the I^2S serial data protocol. In Modes 2 and 3 with BICK≥48fs, the following formats are also valid: 16-bit data followed by eight zeros (17th to 24th bits) and 20-bit data followed by four zeros (21st to 24th bits). In all modes, the serial data is MSB first and 2's complement format. The polarity of BICK can be inverted by the BCKP bit, the polarity of LRCK can be inverted by the LRP bit. PMDAC bit should be set to "0" when BCKP or LRP bits are changed.

DIF2 bit	DIF1 bit	DIF0 bit	MODE	BICK	Figure	
0	0	0	0: 16bit, LSB justified	32fs ≤ BICK ≤ 128fs (Half/Normal Speed Mode) 32fs ≤ BICK ≤ 64fs (Double Speed Mode)	Figure 12	
0	0	1	1: 20bit, LSB justified	40fs ≤ BICK ≤ 128fs (Half/Normal Speed Mode) 40fs ≤ BICK ≤ 64fs (Double Speed Mode)	Figure 13	
0	1	0	2: 24bit, MSB justified	48fs ≤ BICK ≤ 128fs (Half/Normal Speed Mode) 48fs ≤ BICK ≤ 64fs (Double Speed Mode)	Figure 14	Default
0	1	1	3: I^2S Compatible	BICK=32fs (Half/Normal/Double Speed Mode) or 48fs ≤ BICK ≤ 128fs (Half/Normal Speed Mode) 48fs ≤ BICK ≤ 64fs (Double Speed Mode)	Figure 15	
1	0	0	4: 24bit, LSB justified	48fs ≤ BICK ≤ 128fs (Half/Normal Speed Mode) 48fs ≤ BICK ≤ 64fs (Double Speed Mode)	Figure 13	

Table 4. Audio Data Format

BCPKP bit	LRP bit	LRCK Polarity		BICK Polarity (SDATA Latch Timing)	
		Lch Data	Rch Data		
0	0	H: Mode 0,1,2,4 L: Mode 3	L: Mode 0,1,2,4 H: Mode 3	↑	Default
0	1	L: Mode 0,1,2,4 H: Mode 3	H: Mode 0,1,2,4 L: Mode 3	↑	
1	0	H: Mode 0,1,2,4 L: Mode 3	L: Mode 0,1,2,4 H: Mode 3	↓	
1	1	L: Mode 0,1,2,4 H: Mode 3	H: Mode 0,1,2,4 L: Mode 3	↓	

Table 5. LRCK and BICK Polarities

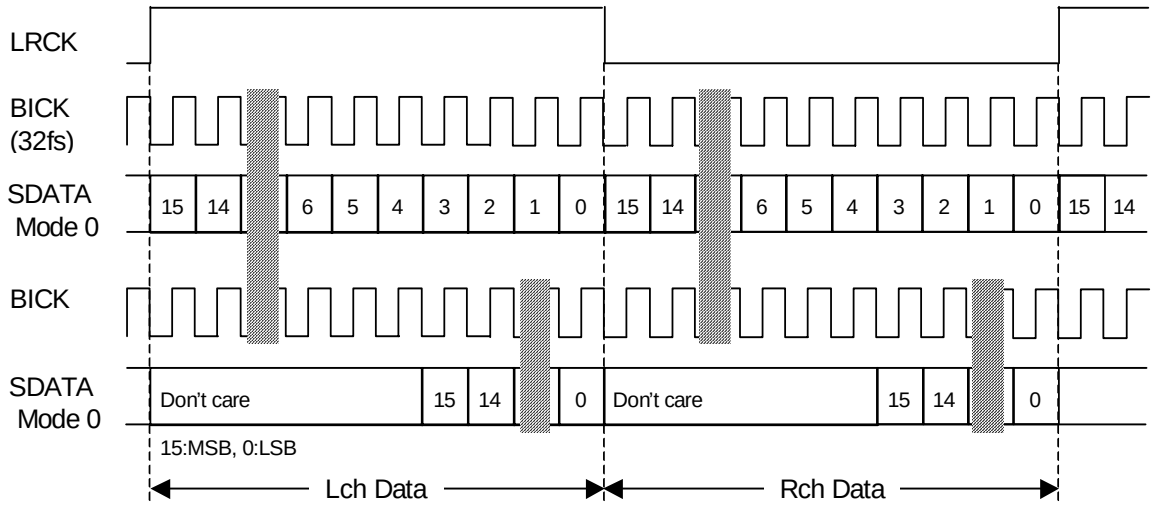


Figure 12. Mode 0 Timing (BCKP bit = "0", LRP bit = "0")

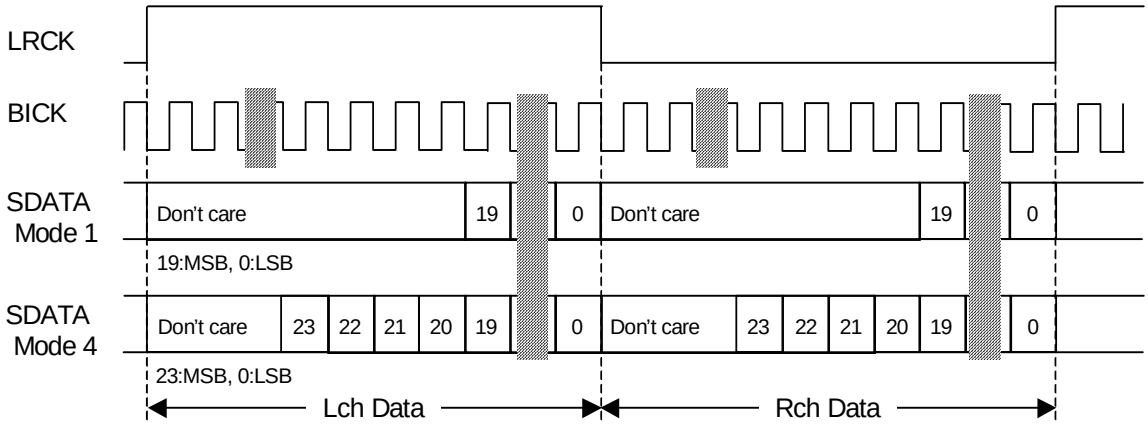


Figure 13. Mode 1, 4 Timing (BCKP bit = "0", LRP bit = "0")

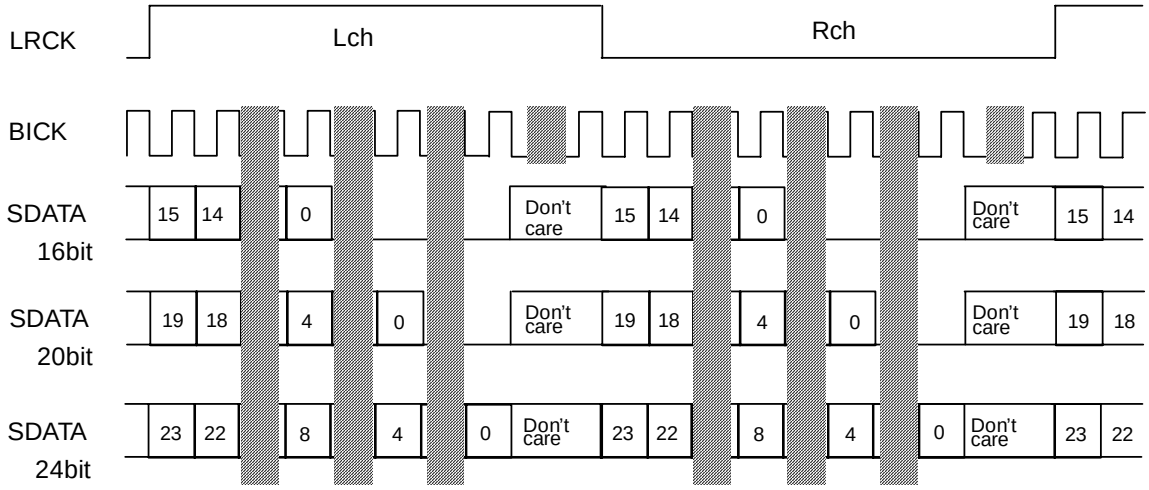


Figure 14. Mode 2 Timing (BCKP bit = "0", LRP bit = "0")

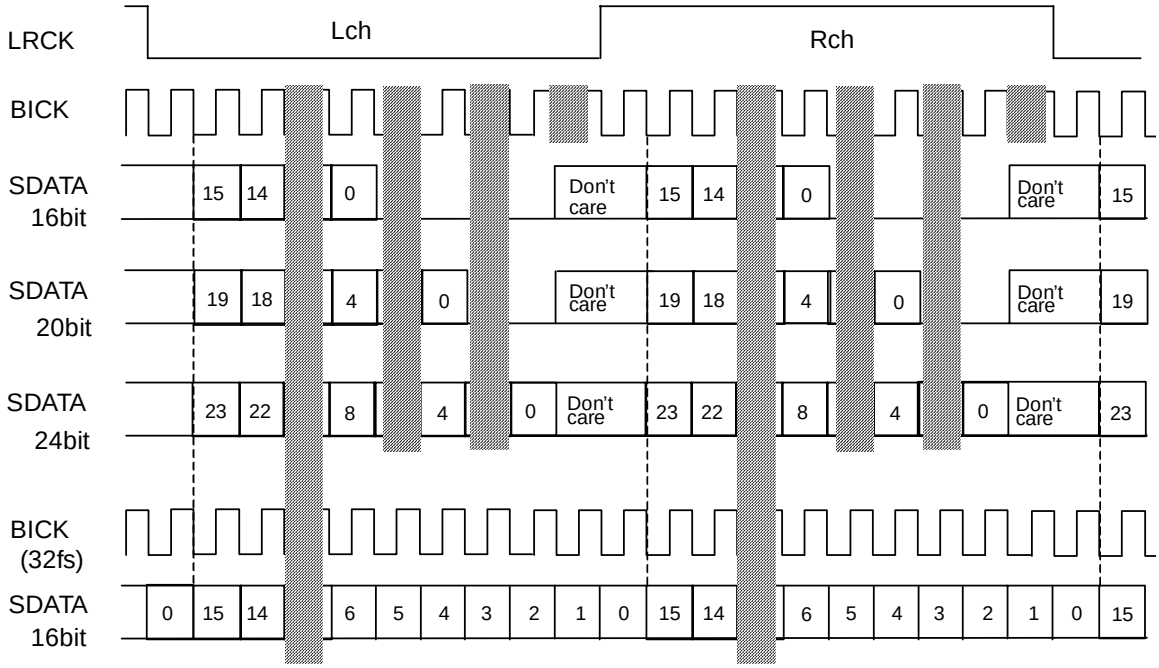


Figure 15. Mode 3 Timing (BCKP bit = “0”, LRP bit = “0”)

■ Digital Volume

The AK4342 includes channel independent digital output volumes (ATT) with 256 levels at linear step including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to –48dB and mute. Changing levels are executed via soft changes without any pop noise. The transition time of 1 level and all 256 levels is shown in Table 7.

At DATTC bit = "1", ATTL7-0 bits control both Lch and Rch attenuation level, while register values of ATTL7-0 bits are not written to ATTR7-0 bits. At DATTC bit = "0", ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level.

ATTL7-0 bits ATTR7-0 bits	ATT (dB)	
FFH • 01H	$20 \log_{10}$ (ATT_DATA / 255)	Default
00H	Mute	

Table 6. Digital Volume Gain Table

STS1 bit	STS0 bit	Sampling Speed	Transition Time		
			1 Level	255 to 0	
0	0	Half Speed Mode	1LRCK	255LRCK	
		Normal Speed Mode	2LRCK	510LRCK	
		Double Speed Mode	4LRCK	1020LRCK	
0	1	Half Speed Mode	2LRCK	510LRCK	
		Normal Speed Mode	4LRCK	1020LRCK	Default
		Double Speed Mode	8LRCK	2040LRCK	
1	0	Half Speed Mode	4LRCK	1020LRCK	
		Normal Speed Mode	8LRCK	2040LRCK	
		Double Speed Mode	16LRCK	4080LRCK	
1	1	Half Speed Mode	8LRCK	2040LRCK	
		Normal Speed Mode	16LRCK	4080LRCK	
		Double Speed Mode	32LRCK	8160LRCK	

Table 7. Transition Time for Digital Volume

■ Soft Mute

Soft mute operation is performed in the digital domain of the DAC input. When the SMUTE bit goes to "1", the output signal is attenuated by –∞ during ATT_DATA×ATT transition time (Figure 16) from the current ATT level. When SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.

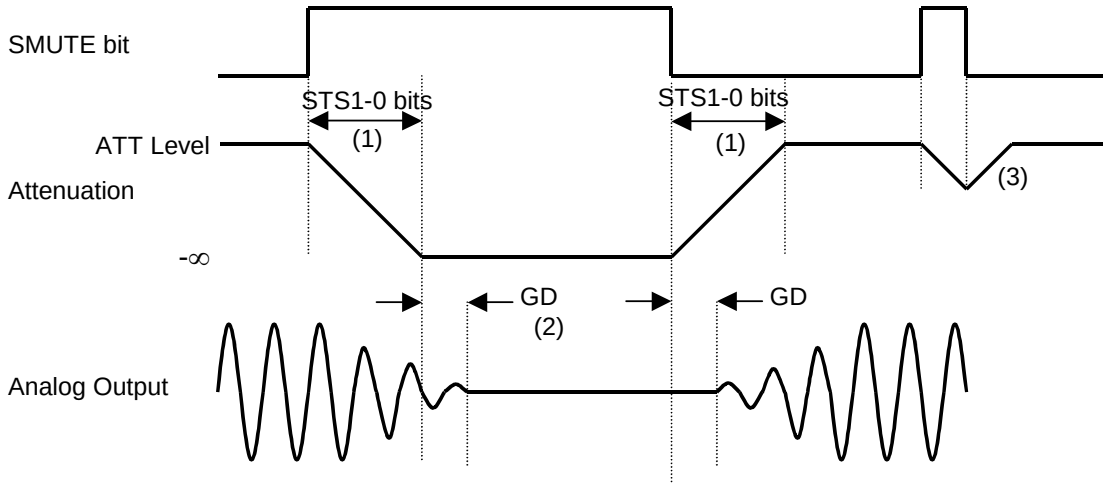


Figure 16. Soft Mute Function

Notes:

(1) ATT_DATA×ATT transition time. For example, this time is 510LRCK cycles at normal speed mode and STS1-0 bit = "01" and ATT_DATA = "128".
(2) Analog output corresponding to digital input has group delay (GD).
(3) If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

■ De-emphasis Filter

The AK4342 includes a digital de-emphasis filter (tc = 50/15μs) via an IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz and 48kHz). This setting is done via control register (DEM1-0 bits). (See Table 8). When the AK4342 is half speed mode or double speed mode, the DEM1-0 bits are ignored and the de-emphasis filter is disabled.

DEM1 bit	DEM0 bit	De-emphasis	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 8. De-emphasis Filter Frequency control

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage from PVDD voltage. The generated voltage is used to lineout and headphone amplifiers. When PMCP bit is set to "1", the charge pump circuit is powered-up. Then all clocks (MCLK, BICK and LRCK) should be supplied. The power up time of charge pump circuit depends on FS3-0 bits (See Table 9).

FS3 bit	FS2 bit	FS1 bit	FS0 bit	Sampling Frequency	Power up time of Charge Pump Circuit	
0	0	0	0	44.1kHz	11.6ms	Default
0	0	0	1	32kHz	8.0ms	
0	0	1	0	48kHz	10.7ms	
0	0	1	1	(Reserve)	(Reserve)	
0	1	0	0	88.2kHz	11.6ms	
0	1	0	1	64kHz	8.0ms	
0	1	1	0	96kHz	10.7ms	
0	1	1	1	(Reserve)	(Reserve)	
1	0	0	0	22.05kHz	11.6ms	
1	0	0	1	16kHz	8.0ms	
1	0	1	0	24kHz	10.7ms	
1	0	1	1	(Reserve)	(Reserve)	
1	1	0	0	11.025kHz	11.6ms	
1	1	0	1	8kHz	8.0ms	
1	1	1	0	12kHz	10.7ms	
1	1	1	1	(Reserve)	(Reserve)	

Table 9. Power up time of Charge Pump Circuit

■ Analog Input

Signal level from LIN/RIN is adjusted by an external resistor (Ri). Internal feedback resistance (Rf) is 20k ± 30% Ω. When PMDAC, PMHP, PMLO or PMAUX bit is set to "1", the left and right channel amplifiers are powered-up. The transition time of signal path (LINL, LINR, RINL and RINR bits) is selected by PTS1-0 bits and FS3-0 bits. The signal path (LINL, LINR, RINL and RINR bits) should not be changed during the transition.

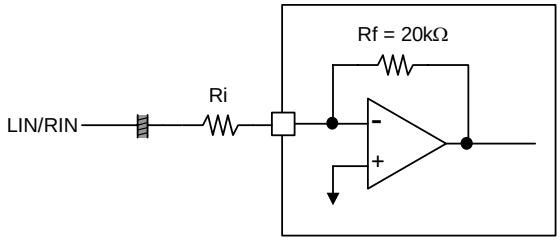


Figure 17. Block diagram of LIN/RIN inputs

■ Headphone Output

Power supply voltage for headphone amplifiers is applied from HVDD and HVEE pins. HVEE pin must be connected with PVEE pin directly. PVEE pin outputs the negative voltage generated by the internal charge pump circuit. The headphone amplifier is single-ended outputs and centered on 0V(HVSS). Therefore, the capacitor for AC-coupling can be removed. The minimum load resistance is 16 Ω.

1. Analog output volume

These volumes are channel independent can gain/attenuate the DAC output signal from +6dB to –48dB. (See Table 10) Changing levels don't have any pop noise. The transition time is selected by PTS1-0 bits and sampling frequency (See Table 2 and Table 15).

At PGAC bit = "1", PGAL4-0 bits control both Lch and Rch attenuation level, while register values of PGAL4-0 bits are not written to PGAR4-0 bits. At PGAC bit = "0", PGAL4-0 bits control Lch level and PGAR4-0 bits control Rch level. When PGAC bit is changed, the transition of volume is executed via soft changes, and PGAL4-0 and PGAR4-0 bits should be changed after the transition time passes.

When changing PGAC bit = "0" → "1" (In case of "PGAL4-0 bit ≠ PGAR4-0 bit"), the gain of right channel is changed to the register setting of PGAL4-0 bits. When changing PGAC bit = "1" → "0" (In case of "PGAL4-0 bit ≠ PGAR4-0 bit"), the gain of right channel is changed to the last register setting which is written into PGAR4-0 bits.

PGAL4-0 bits PGAR4-0 bits	GAIN/ATT (dB)	Step	Level	
1FH	+6	1dB	16	
1EH	+5			
•	•			
1AH	+1			
19H	0			Default
18H	-1			
•	•			
10H	-9			
0FH	-10	2dB	11	
0EH	-12			
•	•			
06H	-28			
05H	-30			
04H	-32	4dB	5	
03H	-36			
02H	-40			
01H	-44			
00H	-48			

Table 10. Volume Setting for headphone amplifier

2. Mute Function

When HMUTEL/HMUTER bit is set to "1", the headphone amplifier (HPL/HPR pins) goes to ground level (0V). This function is independent L/R channels. This mute time depends on the setting of PTS1-0 bits and sampling frequency(FS3-0 bits). When HMUTEL/HMUTER bit is set to "0", the outputs are in normal operation.

3. Power-up/down

Headphone amplifiers are powered-up/down by PMHP bit, HPL and HPR pins go to HVSS(0V). The power-on/off time depends on the setting of PUT1-0 bits and sampling frequency (FS3-0 bits). The power-up/down of headphone amplifiers should be done in the mute state (HMUTEL bit = HMUTER bit = "1").

■ Lineout amp

Power supply voltage for lineout amplifier is applied from HVDD and HVEE pins. HVEE pin must be connected with PVEE pin directly. PVEE pin outputs the negative voltage generated by the internal charge pump circuit. The lineout amplifiers are single-ended outputs and centered on 0V(HVSS). The output level is typically 2Vrms (@ AVDD=3.3V, 0dBFS). The minimum load resistance is 10kΩ.

1. Analog volume for lineout

These volumes are common to L/R channels and can attenuate the DAC output signal from +0dB to –31dB with 1dB step (See Table 11). Changing levels don't have any pop noise. The transition time is selected by PTS1-0 bits and sampling frequency (See Table 2 and Table 15).

LPGA4-0 bits	ATT (dB)	Step	Level	
1FH	0	1dB	32	Default
1EH	-1			
1DH	-2			
1CH	-3			
•	•			
18H	-29			
01H	-30			
00H	-31			

Table 11. Volume Setting for Lineout

2. Mute Function

When LMUTE bit is set to "1", the lineout amplifiers (LOUT and ROUT pins) go to ground level (0V). This mute time depends on the setting of PTS1-0 bits and sampling frequency(FS3-0 bits). This function is common to L/R channels. When LMUTE bit is set to "0", the outputs are in normal operation.

3. Power-up/down

Lineout amplifiers are powered-up/down by PMLO bit. The power-on/off time depends on the setting of PUT1-0 bits and sampling frequency (FS3-0 bits). The power-up/down of lineout amplifiers should be done in the mute state (LMUTE bit = "1").

4. Output circuit

When LOUT/ROUT drives some capacitive load, a resistor should be added in series between LOUT/ROUT and capacitive load. Figure 18 shows an example of 470Ω series resistor. In this case, LOUT/ROUT can drive capacitive load up to 1nF.

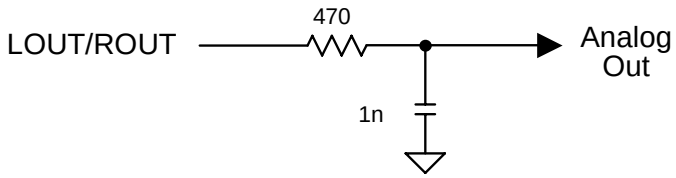


Figure 18. External 1st order LPF Circuit Example
(fc = 339kHz, gain = -0.06dB @ 40kHz)

■ Aux-out amp

Aux-out amplifiers are single-ended outputs and centered on VCOM voltage (0.45 x AVDD). Signal output voltage is typically 700mVrms (@ AVDD = 3.3V, 0dBFS). The minimum load resistance is 10kΩ.

When the AVCMN bit is set to "0", the common voltage of Aux-out amplifiers falls. When the AVCMN bit is set to "1", the common voltage rises to 0.45 x AVDD. A capacitor between the MUTET pin and ground reduces pop noise at power-up. Rise/Fall time constant is in proportional to AVDD voltage and the capacitor at MUTET pin.

[Example]: A capacitor between the MUTET pin and ground = 1.0μF, AVDD=3.3V:
Rise/fall time constant: τ = 100ms(typ), 300ms(max)

When PMAUX bit is set to "0", the Aux-out amplifiers are powered-down, and the outputs (LAUX and RAUX pins) go to "L" (AVSS). When the AMUTE bit is set to "1", the outputs (LAUX and RAUX pins) are muted and become VCOM voltage. When the AMUTE bit is set to "0", the outputs are in normal operation.

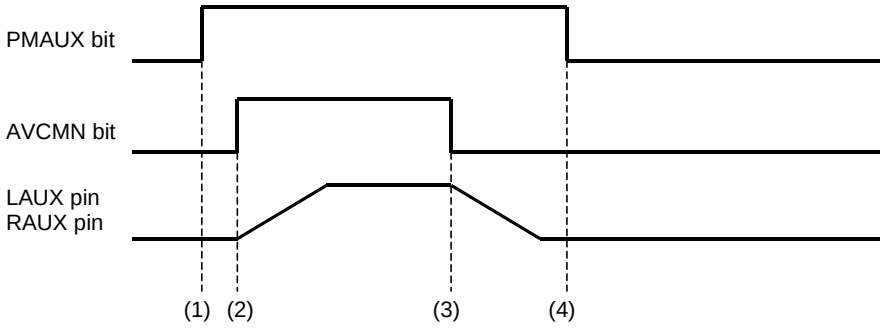


Figure 19. Power-up/Power-down Timing for Aux-out amplifier

(1) Aux-out amplifier power-up (PMAUX bit = "1"). The outputs are still AVSS.
(2) Aux-out amplifier common voltage rises up (AVCMN bit = "1")
(3) Aux-out amplifier common voltage falls down (AVCMN bit = "0")
(4) Aux-out amplifier power-down (PMAUX bit = "0"). The outputs are AVSS. If the power supply is switched off or Aux-out amplifier is powered-down before the common voltage goes to AVSS, some pop noise occurs.

■ Transition Time

Changing volume level, power-up/down and switching signal path don't have any pop noise. The following registers have a transition time shown in Table 13 and Table 15. It depends the sampling frequency (FS3-0 bits) and the setting of PUT1-0 bits and PTS1-0 bits. It is necessary to take the interval time when the register is changed continually. The interval time depends on the transition time. The setting of transition time should not be changed during transition.

	Address	Register Name
PUT1-0 bit	00H	PMHP, PMLO

Table 12. Registers with transition time (PUT1-0 bits)

PUT1 bit	PUT0 bit	Sampling Frequency (FS3-0 bits)	Transition Time	
0	0	8k / 16k / 32k / 64kHz	32ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	34.8ms	
		12k / 24k / 48k / 96kHz	32ms	
0	1	8k / 16k / 32k / 64kHz	64ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	69.7ms	
		12k / 24k / 48k / 96kHz	64ms	
1	0	8k / 16k / 32k / 64kHz	128ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	139ms	Default
		12k / 24k / 48k / 96kHz	128ms	
1	1	8k / 16k / 32k / 64kHz	256ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	278ms	
		12k / 24k / 48k / 96kHz	256ms	

Table 13. Transition Time (PUT1-0 bits)

	Address	Register Name
PTS1-0 bit	01H	AMUTE
	04H	HMUTEL, PGAL4-0
	05H	HMUTER, PGAR4-0
	06H	RINR, RINL, LINR, LINL, DACLR
	07H	LMUTE, LPGA4-0

Table 14. Registers with transition time (PTS1-0 bits)

PTS1 bit	PTS0 bit	Sampling Frequency (FS3-0 bits)	Transition Time	
0	0	8k / 16k / 32k / 64kHz	16ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	17.4ms	Default
		12k / 24k / 48k / 96kHz	16ms	
0	1	8k / 16k / 32k / 64kHz	32ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	34.8ms	
		12k / 24k / 48k / 96kHz	32ms	
1	0	8k / 16k / 32k / 64kHz	64ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	69.7ms	
		12k / 24k / 48k / 96kHz	64ms	
1	1	8k / 16k / 32k / 64kHz	128ms	
		11.025k / 22.05k / 44.1k/ 88.2kHz	139ms	
		12k / 24k / 48k / 96kHz	128ms	

Table 15. Transition Time (PTS1-0 bits)

■ System Reset

PDN pin must keep "L" until all power supply pins (AVDD, DVDD, PVDD, HVDD and TVDD) are applied. After they are applied, PDN pin must be set to "H". After exiting reset (PDN pin: "L" → "H"), all blocks (VCOM, DAC, HPL, HPR, LAUX, RAUX, LOUT, ROUT and charge pump circuit) switch to the power-down state. The contents of the control register are maintained until the reset is done.

DAC exits reset and power down state by MCLK edge after PMDAC bit is changed to "1", and then DAC is powered up and the internal timing starts clocking by LRCK edge. DAC is in power-down mode until MCLK and LRCK are input.

■ Power-Up/Down Sequence

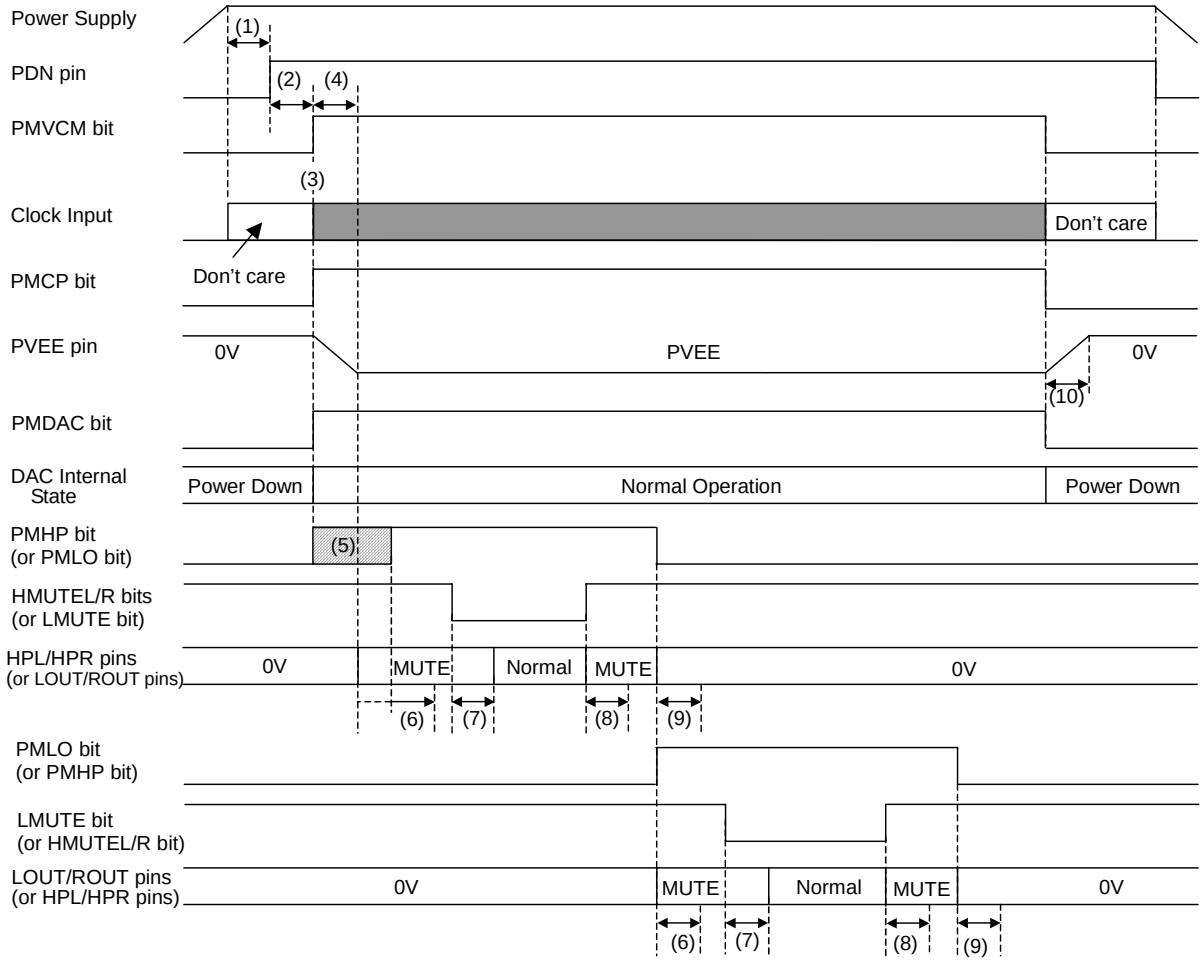


Figure 20. Example of Power-up/down Sequence

(1) After Power Up: PDN pin "L" → "H"
"L" time (1) of 150ns or more is needed to reset the AK4342.
PDN pin must keep "L" until all power supply pins (AVDD, DVDD, PVDD, HVDD and TVDD) are applied. After they are applied, PDN pin must be set to "H".

(2) DFS1-0, DIF2-0, DEM1-0, FS3-0, PTS1-0, STS1-0, PUT1-0, LRP, BCKP and DACLR bits should be set during this period before the DAC and charge pump circuit are powered-up.

(3) Supply the external clocks (MCLK, BICK, LRCK)

(4) Power Up the charge pump circuit, DAC and VCOM; PMCP bit = PMDAC bit = PMVCM bit = "0" → "1"
PVEE pin goes to PVEE voltage according to the setting of FS3-0 bits (See Table 9).

(5) When PMCP bit and PMHP bit (PMLO bit) are set to "1" at the same time or PMHP bit (PMLO bit) is set to "1" during the charge pump circuit is powered-up, headphone (lineout) amplifier is powered-up after the charge pump circuit is powered-up.

(6) Power Up the headphone (lineout) amplifiers; PMHP bit (PMLO bit) = "0" → "1"
The headphone (lineout) amplifiers are in mute state and have some DC offset. The power up time of headphone (lineout) amplifiers depends on PUT1-0 bits and FS3-0 bits.
PMHP and PMLO bits should not be changed during this period.

(7) Release the mute state of headphone (lineout) amplifiers; HMUTEL bit = HMUTER bit (LMUTE bit) = "1" → "0"
The headphone (lineout) amplifiers are in the normal state after the transition time passes. The transition is executed via soft changes. The transition time depends on PTS1-0 bits and FS3-0 bits.
LPGA4-0, PGAL4-0, PGAR4-0 and PGAC bits should not be changed during this period.

(8) Mute headphone (lineout) amplifiers: HMUTEL = HMUTER (LMUTE bit) = "0" → "1"
The headphone (lineout) amplifiers are in the mute state after the transition time passes. The transition is executed via soft changes. The transition time depends on PTS1-0 bits and FS3-0 bits.
LPGA4-0, PGAL4-0, PGAR4-0 and PGAC bits should not be changed during this period.

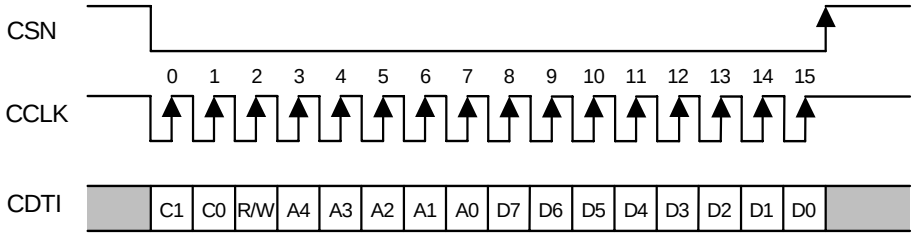
(9) Power-down the headphone (lineout) amp; PMHP bit (PMLO bit) = "1" → "0"
The headphone (lineout) amplifiers are powered-down. The power-down time of headphone (lineout) amplifiers depend on PUT1-0 bits and FS3-0 bits.
PMHP and PMLO bits should not be changed during this period.

(10) Power down the charge pump circuit, DAC and VCOM; PMCP bit = PMDAC bit = PMVCM bit = "1" → "0"
PVEE pin becomes "0V" according to the time constant of internal resistor and capacitor of PVEE and HVEE pins. Internal resistor is typically 17.5kΩ. The charge pump circuit may be powered-up during this period.

■ Serial Control Interface

1. 3-wire Serial Control Mode (I2C pin = "L")

Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The data on this interface consists of a 2-bit Chip address (Fixed to "01"), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Address and data are latched on the CSN falling edge ("↓"). Clock speed of CCLK is 5MHz (max). The value of internal registers are initialized by PDN pin = "L".



C1-C0: Chip Address (Fixed to "01")
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 21. Serial Control I/F Timing

2. I²C-bus Control Mode (I2C pin = "H")

The AK4342 supports a fast-mode I²C-bus system (max: 400kHz).

1. WRITE Operations

Figure 22 shows the data transfer sequence for the I²C-bus mode. All commands are preceded by a START condition. A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition (Figure 28). After the START condition, a slave address is sent. This address is 7 bits long followed by an eighth bit that is a data direction bit (R/W). The most significant five bits of the slave address are fixed as "001000". The next one bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) set these device address bits (Figure 23). If the slave address matches that of the AK4342, the AK4342 generates an acknowledge and the operation is executed. The master must generate the acknowledge-related clock pulse and release the SDA line (HIGH) during the acknowledge clock pulse (Figure 29). A R/W bit value of "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

The second byte consists of the control register address of the AK4342. The format is MSB first, and those most significant 3-bits are fixed to zeros (Figure 24). The data after the second byte contains control data. The format is MSB first, 8bits (Figure 25). The AK4342 generates an acknowledge after each byte has been received. A data transfer is always terminated by a STOP condition generated by the master. A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition (Figure 28).

The AK4342 can perform more than one byte write operation per sequence. After receipt of the third byte the AK4342 generates an acknowledge and awaits the next data. The master can transmit more than one byte instead of terminating the write cycle after the first data byte is transferred. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 09H prior to generating the stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The data on the SDA line must remain stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW (Figure 30) except for the START and STOP conditions.

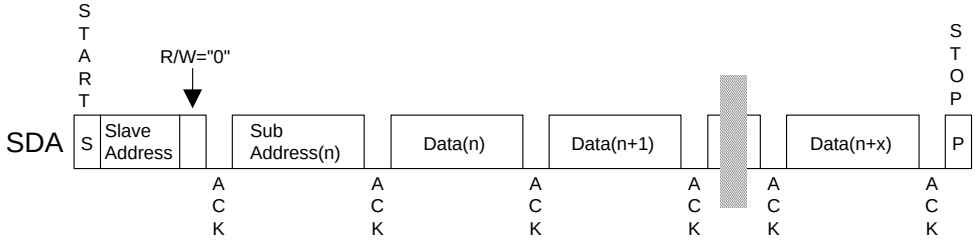


Figure 22. Data Transfer Sequence at the I²C-Bus Mode

0	0	1	0	0	0	CAD0	R/W

Figure 23. The First Byte

0	0	0	A4	A3	A2	A1	A0

Figure 24. The Second Byte

D7	D6	D5	D4	D3	D2	D1	D0

Figure 25. Byte Structure after the second byte

2. READ Operations

Set the R/W bit = "1" for the READ operation of the AK4342. After transmission of data, the master can read the next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After receiving each data packet the internal 5-bit address counter is incremented by one, and the next data is automatically taken into the next address. If the address exceeds 09H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4342 supports two basic read operations: CURRENT ADDRESS READ and RANDOM ADDRESS READ.

2-1. CURRENT ADDRESS READ

The AK4342 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) were to address n, the next CURRENT READ operation would access data from the address n+1. After receipt of the slave address with R/W bit set to "1", the AK4342 generates an acknowledge, transmits 1-byte of data to the address set by the internal address counter and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4342 ceases transmission.

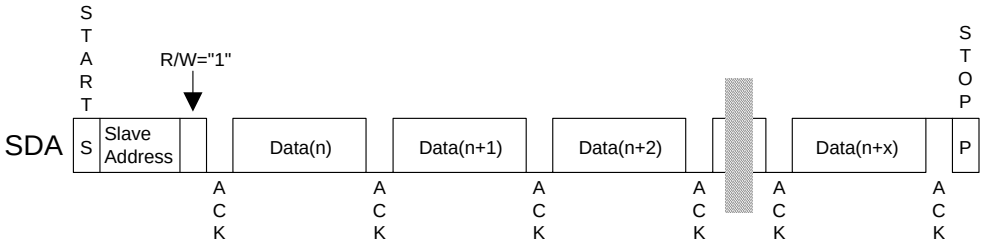


Figure 26. CURRENT ADDRESS READ

2-2. RANDOM ADDRESS READ

The random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation. The master issues a start request, a slave address (R/W bit = "0") and then the register address to read. After the register address is acknowledged, the master immediately reissues the start request and the slave address with the R/W bit set to "1". The AK4342 then generates an acknowledge, 1 byte of data and increments the internal address counter by 1. If the master does not generate an acknowledge to the data but instead generates a stop condition, the AK4342 ceases transmission.

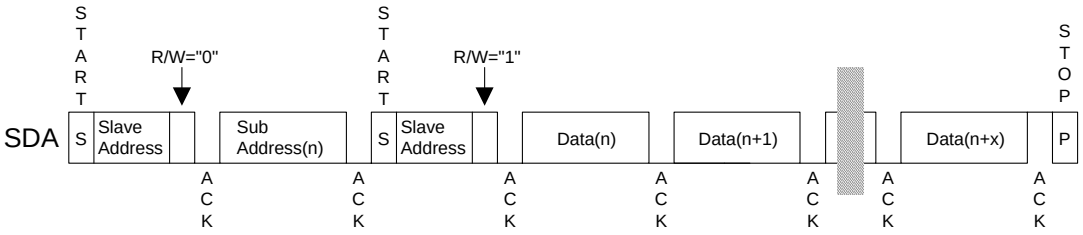


Figure 27. RANDOM ADDRESS READ

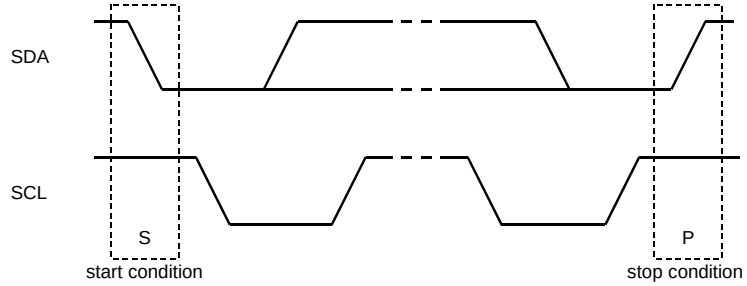


Figure 28. START and STOP Conditions

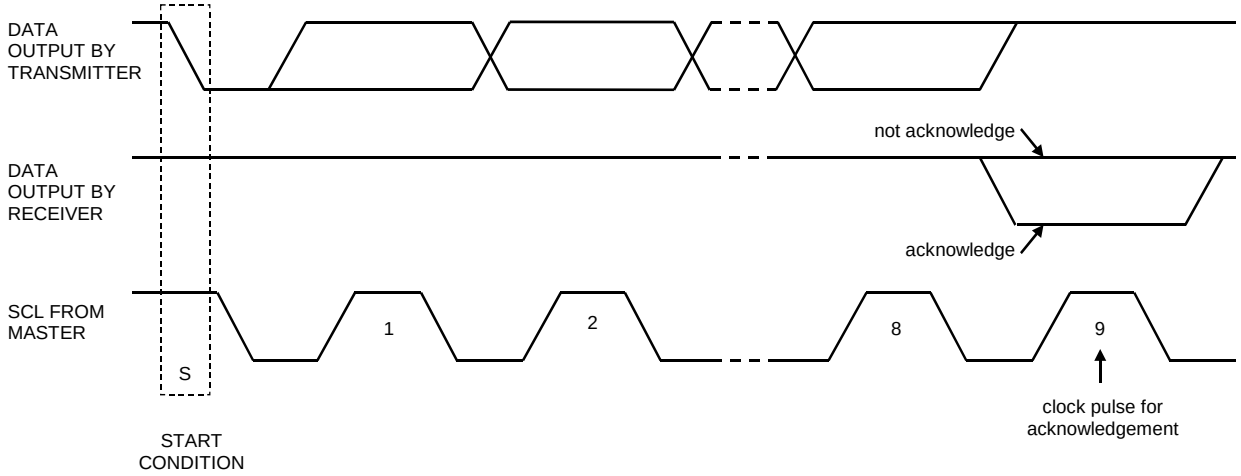


Figure 29. Acknowledge on the I^2C-Bus

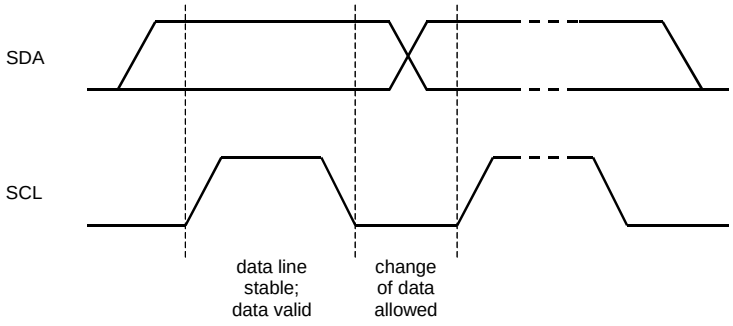


Figure 30. Bit Transfer on the I^2C-Bus

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	PMAUX	PMLO	PMCP	PMHP	PMDAC	PMVCM
01H	Mode Control 0	AMUTE	SMUTE	AVCMN	DIF2	DIF1	DIF0	DFS1	DFS0
02H	Mode Control 1	0	0	FS3	FS2	FS1	FS0	DEM1	DEM0
03H	Mode Control 2	PGAC	PTS1	PTS0	STS1	STS0	DATTC	BCKP	LRP
04H	HP Lch PGA Control	0	0	HMUTEL	PGAL4	PGAL3	PGAL2	PGAL1	PGAL0
05H	HP Rch PGA Control	0	0	HMUTER	PGAR4	PGAR3	PGAR2	PGAR1	PGAR0
06H	Output Select	PUT1	PUT0	RINR	RINL	LINR	LINL	DACLR	0
07H	Lineout PGA control	0	0	LMUTE	LPGA4	LPGA3	LPGA2	LPGA1	LPGA0
08H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
09H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0

All registers inhibit writing at PDN pin = "L".
PDN pin = "L" resets the registers to their default values.

Note 31: The bits indicated to "0" in the register map must contain a "0" value.
Note 32: Only write to address 00H to 09H.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power Management	0	0	PMAUX	PMLO	PMCP	PMHP	PMDAC	PMVCM
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	0

PMVCM: Power Management for VCOM Block
0: Power OFF (Default)
1: Power ON

PMDAC: Power Management for DAC Blocks
0: Power OFF (Default)
1: Power ON
When PMDAC bit is changed from "0" to "1", DAC is powered-up with the current register values (ATT value, sampling rate, etc).

PMHP: Power Management for Headphone Amp
0: Power OFF (Default). HPL/HPR pins become HVSS (0V).
1: Power ON

PMCP: Power Management for Charge Pump Circuit
0: Power OFF (Default)
1: Power ON

PMLO: Power Management for Line-out Amp
0: Power OFF (Default). LOUT/ROUT pins become HVSS (0V).
1: Power ON

PMAUX: Power Management for Aux Out
0: Power OFF (Default) LAUX and RAUAX pins become AVSS (0V).
1: Power ON

All blocks can be powered-down by setting the PDN pin to "L" regardless of register values setup. All blocks can be also powered-down by setting all bits of this address to "0". In this case, control register values are maintained.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Mode Control 0	AMUTE	SMUTE	AVCMN	DIF2	DIF1	DIF0	DFS1	DFS0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	0	0	0	1	0	0	0

DFS1-0: Sampling Speed Select (See Table 1)
Default: “00” (Normal Speed Mode)

DIF2-0: Audio Data Interface Format Select (See Table 4)
Default: “010” (Mode 2; 24bit, MSB justified)

AVCMN: Common Voltage control for LAUX/RAUX
0: LAUX/RAUX pins become AVSS (0V). (Default)
1: LAUX/RAUX pins become “0.45 x AVDD”.

SMUTE: Soft Mute Control
0: Normal operation (Default)
1: DAC outputs soft-muted

AMUTE: Mute control for LAUX/RAUX
0: Normal operation
1: Mute. LAUX/RAUX pins output common voltage. (Default)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Mode Control 1	0	0	FS3	FS2	FS1	FS0	DEM1	DEM0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis Filter Frequency Select (See Table 8)
Default: “01” (OFF)

FS3-0: Sampling Frequency Select (Table 2)
Default: “0000” (fs=44.1kHz)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Mode Control 2	PGAC	PTS1	PTS0	STS1	STS0	DATTC	BCKP	LRP
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	0	0	1	0	0	0

LRP: LRCK Polarity Select
0: Normal (Default)
1: Invert

BCKP: BICK Polarity Select
0: Normal (Default)
1: Invert

DATTC: DAC Digital Attenuator Control Mode Select
0: Independent (Default)
1: Dependent
At DATTC bit = "1", ATTL7-0 bits control both Lch and Rch attenuation level, while register values of ATTL7-0 bits are not written to ATTR7-0 bits. At DATTC bit = "0", ATTL7-0 bits control Lch level and ATTR7-0 bits control Rch level.

STS1-0: Soft mute cycle setting (See Table 7)
Default: "01" (1020LRCK at Normal Speed Mode)

PTS1-0: Select Transition time for AMUTE, LINL, LINR, RINL, RINR, DACLR, LPGA4-0, PGAL4-0, PGAR4-0, LMUTE, HMUTEL and HMUTER (See Table 15)
Default: "00"

PGAC: PGA Control Mode Select
0: Independent (Default)
1: Dependent
At PGAC bit = "1", PGL4-0 bits control both Lch and Rch attenuation level, while register values of PGAL4-0 bits are not written to PGAR4-0 bits. At PGAC bit = "0", PGAL4-0 bits control Lch level and PGAR4-0 bits control Rch level.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	Lch PGA Control	0	0	HMUTEL	PGAL4	PGAL3	PGAL2	PGAL1	PGAL0
05H	Rch PGA Control	0	0	HMUTER	PGAR4	PGAR3	PGAR2	PGAR1	PGAR0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	0	0	1

PGAL4-0: Setting of analog volume for Lch (See Table 10)
HMUTEL: Mute control for HPL
0: Normal operation
PGAL4-0 bits control attenuation value.
1: Mute. (Default)
PGAL4-0 bits are ignored.

PGAR4-0: Setting of analog volume for Rch (See Table 10)
HMUTER: Mute control for HPR
0: Normal operation
PGAR4-0 bits control attenuation value.
1: Mute. (Default)
PGAR4-0 bits are ignored.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
06H	Output Select 0	PUT1	PUT0	RINR	RINL	LINR	LINL	DACLR	0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	RD
Default		1	0	0	0	0	0	0	0

DACLR: DAC output signal is added to MIX amp.
0: OFF (Default)
1: ON

LINL: Input signal to LIN pin is added to Lch of MIX amp.
0: OFF (Default)
1: ON

LINR: Input signal to LIN pin is added to Rch of MIX amp.
0: OFF (Default)
1: ON

RINL: Input signal to RIN pin is added to Lch of MIX amp.
0: OFF (Default)
1: ON

RINR: Input signal to RIN pin is added to Rch of MIX amp.
0: OFF (Default)
1: ON

PUT1-0: Select Transition Time for PMHP and PMLO bits (See Table 13)
Defaults: "10"

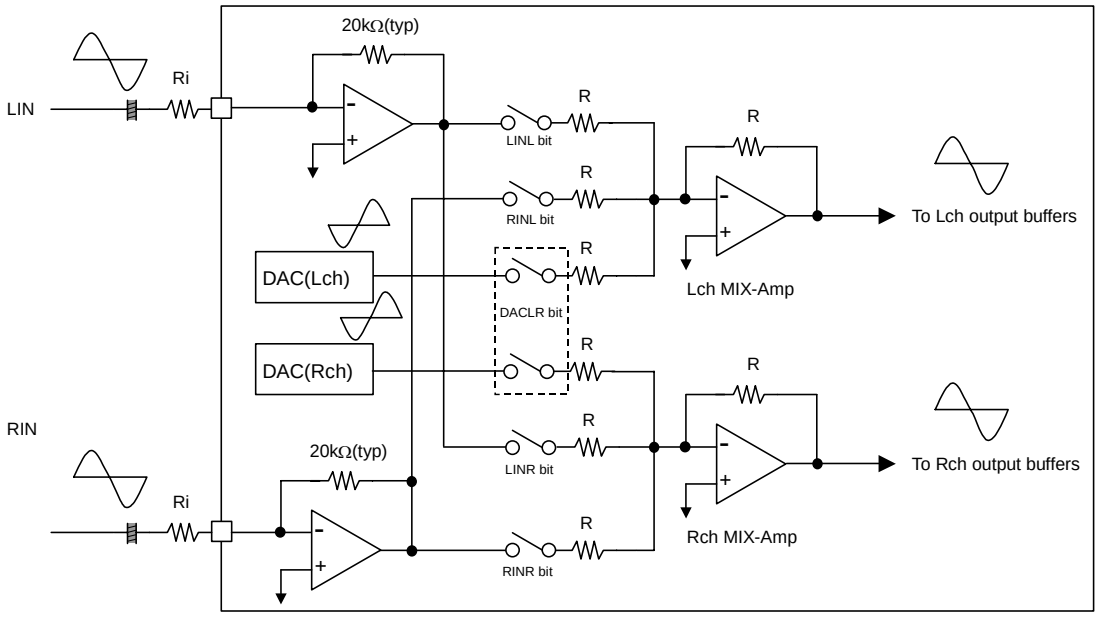


Figure 31. Analog Mixing Circuit

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
07H	Lineout PGA Control	0	0	LMUTE	LPGA4	LPGA3	LPGA2	LPGA1	LPGA0
R/W		RD	RD	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	0	1	1	1	1	1	1

LPGA4-0: Setting of the analog volume for Lineout
Default: "1FH" (0dB) (See Table 11)

LMUTE: Mute control for LOUT/ROUT
0: Normal operation
LPGA4-0 bits control attenuation value.
1: Mute. (Default)
LPGA4-0 bits are ignored.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
08H	DAC Lch ATT	ATTL7	ATTL6	ATTL5	ATTL4	ATTL3	ATTL2	ATTL1	ATTL0
09H	DAC Rch ATT	ATTR7	ATTR6	ATTR5	ATTR4	ATTR3	ATTR2	ATTR1	ATTR0
R/W		R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		1	1	1	1	1	1	1	1

ATTL7-0: Setting of the attenuation value of output signal from DAC Lch
ATTR7-0: Setting of the attenuation value of output signal from DAC Rch
ATT = 20 $\log_{10}$ (ATT_DATA / 255) [dB]
FFH: 0dB (Default)
00H: Mute

SYSTEM DESIGN

Figure 32 shows the system connection diagram. An evaluation board [AKD4342] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

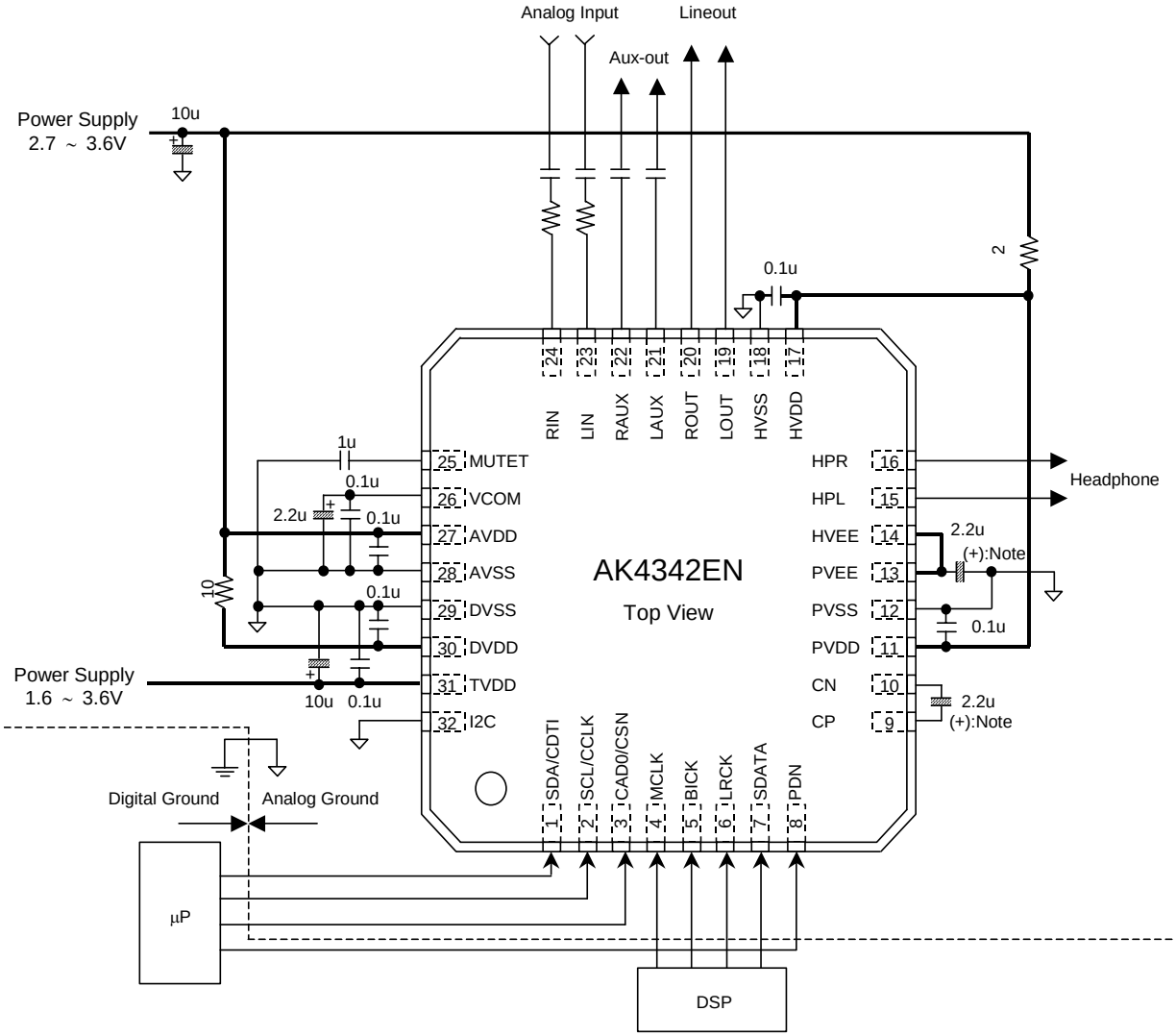


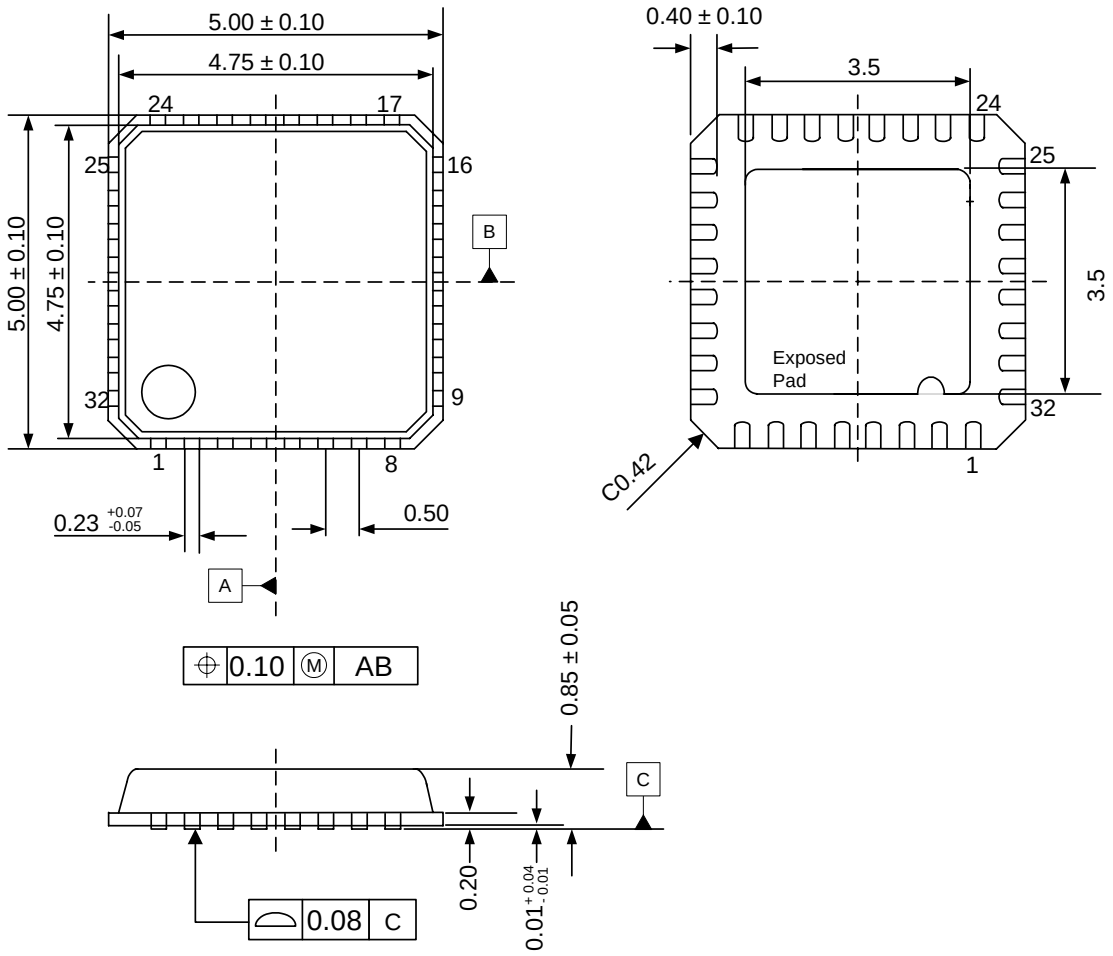
Figure 32. Typical Connection Diagram in 3-wire mode

Note:

- **A 2Ω resistor should be added in series between HVDD/PVDD pins and power supply line in order to limit the current.**
- These capacitors should use low ESR (Equivalent Series Resistance) over all temperature range. When these capacitors are not bipolar, the positive side should be connected CP pin or analog ground.
- AVSS, DVSS, PVSS and HVSS of the AK4342 should be distributed separately from the ground of external controllers.
- All digital input except for pull-up pins should not be left floating.
- If TVDD voltage is the same as DVDD voltage, TVDD pin is directly connected to DVDD pin and the capacitor (10μF and 0.1μF) connected to TVDD pin can be removed.

PACKAGE

● 32pin QFN (Unit: mm)

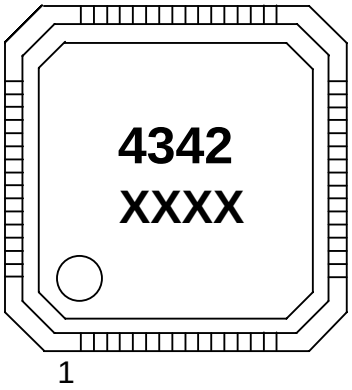


Note) The exposed pad on the bottom surface of the package must be connected to the ground.

■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



XXXXX : Date code identifier (4 digits)

Revision History

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/04/26	00	First Edition		
06/05/09	01	Change description	39	SYSTEM DESIGN: Figure 32: A 2Ω resistor was added between PVDD and HVDD pins and power supply line. Note: "A 2Ω resistor should be added in series ~ the current." was added.
06/07/07	02	Error Correct	7	ANALOG CHARACTERISTICS: Headphone-Amp; THD+N (fs=44.1kHz, 0dBFS output): typ. -20dB ➔ -40dB THD+N (fs=96kHz, 0dBFS output): typ. -20dB ➔ -40dB Line Output; THD+N (fs=96kHz, 0dBFS output): typ. -85dB ➔ -88dB
			23	Headphone Output 1. Analog output volume; See Table 12 and Table 15 ➔ See Table 2 and Table 15
			24	Lineout amp 1. Analog volume for lineout; See Table 12 and Table 15 ➔ See Table 2 and Table 15
			25	Aux-out amp Figure 19: (2) [AVCMN bit = "0"] ➔ [AVCMN bit = "1"] (3) [AVCMN bit = "1"] ➔ [AVCMN bit ="0"]
			27	Power-Up/Down Sequence: Figure 20; The location of (4) in Figure 20 was changed.
			29	3-wire Serial Control Mode: ~ 2-bit Chip address (Fixed to "10") ➔ ~ 2-bit Chip address (Fixed to "01")
			30	I^2C –bus Control Mode: a. [The AK4342 supports ~ (max.100kHz).] was deleted. b. [The AK4342 does not support a fast-mode I2C-bus system (max.400kHz).] ➔ [The AK4342 supports a fast-mode I2C-bus system (max.400kHz).] c. WRITE Operations; [If the address exceeds 08H prior to ~.] ➔ [If the address exceeds 09H prior to ~.]
			37	Addr=06H, PUT1-0: See Table 12 ➔ See Table 13

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