AK4390

Ultra Low Latency 32-Bit ΔΣ DAC

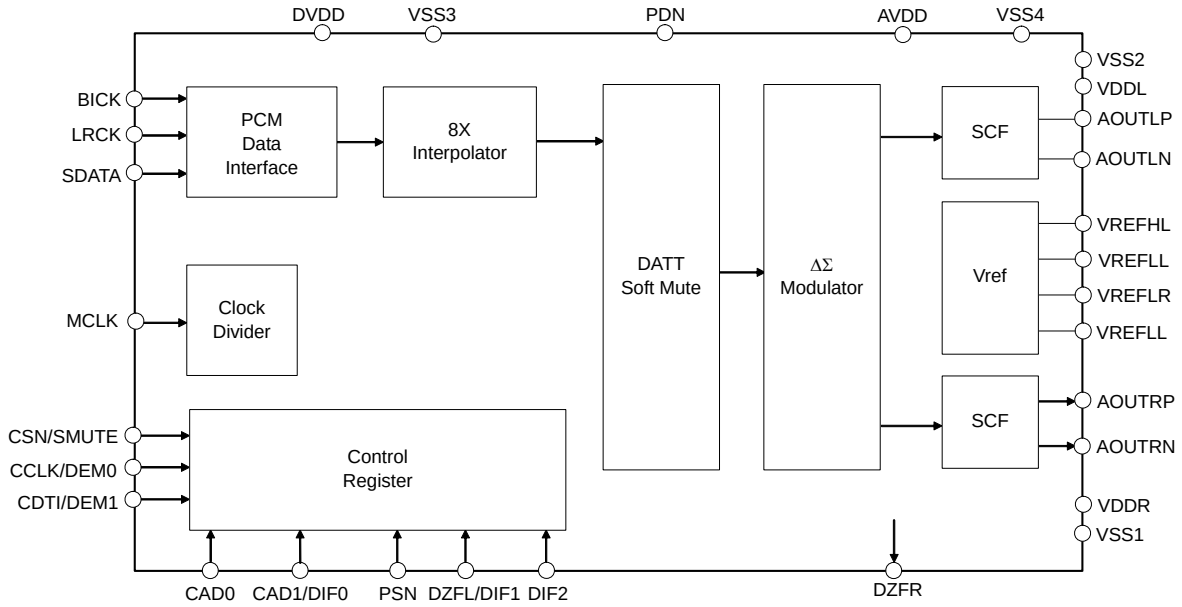
GENERAL DESCRIPTION

The AK4390 is a high performance stereo DAC capable of sampling up to 216kHz including a 32-bit digital filter. The modulator uses AKM's multi-bit architecture, delivering wide dynamic range while preserving linearity for improved THD+N performance. The AK4390 has fully differential switched-cap filter outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4390 accepts 192kHz PCM data, ideal for a wide range of applications including Blu-Ray, DVD-Audio, high end sound cards, digital audio Firewire and USB interface boxes, and digital mixers.

FEATURES

- **128-times Oversampling**
- **Sampling Rate: 30kHz ~ 216kHz**
- **32Bit 8x Digital Filter**
  - **Ripple: ±0.005dB, Attenuation: 100dB**
  - **Low latency option: 7/fs**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **Digital De-emphasis for 32, 44.1, 48kHz sampling**
- **Soft Mute**
- **Digital Attenuator (255 levels and 0.5dB step)**
- **THD+N: –103dB**
- **DR, S/N: 120dB**
- **Audio Format: 24/32bit MSB justified, 16/20/24/32bit LSB justified, I^2S**
- **Master Clock:**
  - **30kHz ~ 32kHz: 1152fs**
  - **30kHz ~ 54kHz: 512fs or 768fs**
  - **30kHz ~ 108kHz: 256fs or 384fs**
  - **108kHz ~ 216kHz: 128fs or 192fs**
- **Power Supply: 5V ± 5%**
- **TTL Level Digital I/F**
- **Package: 30pin VSOP**

■ Block Diagram

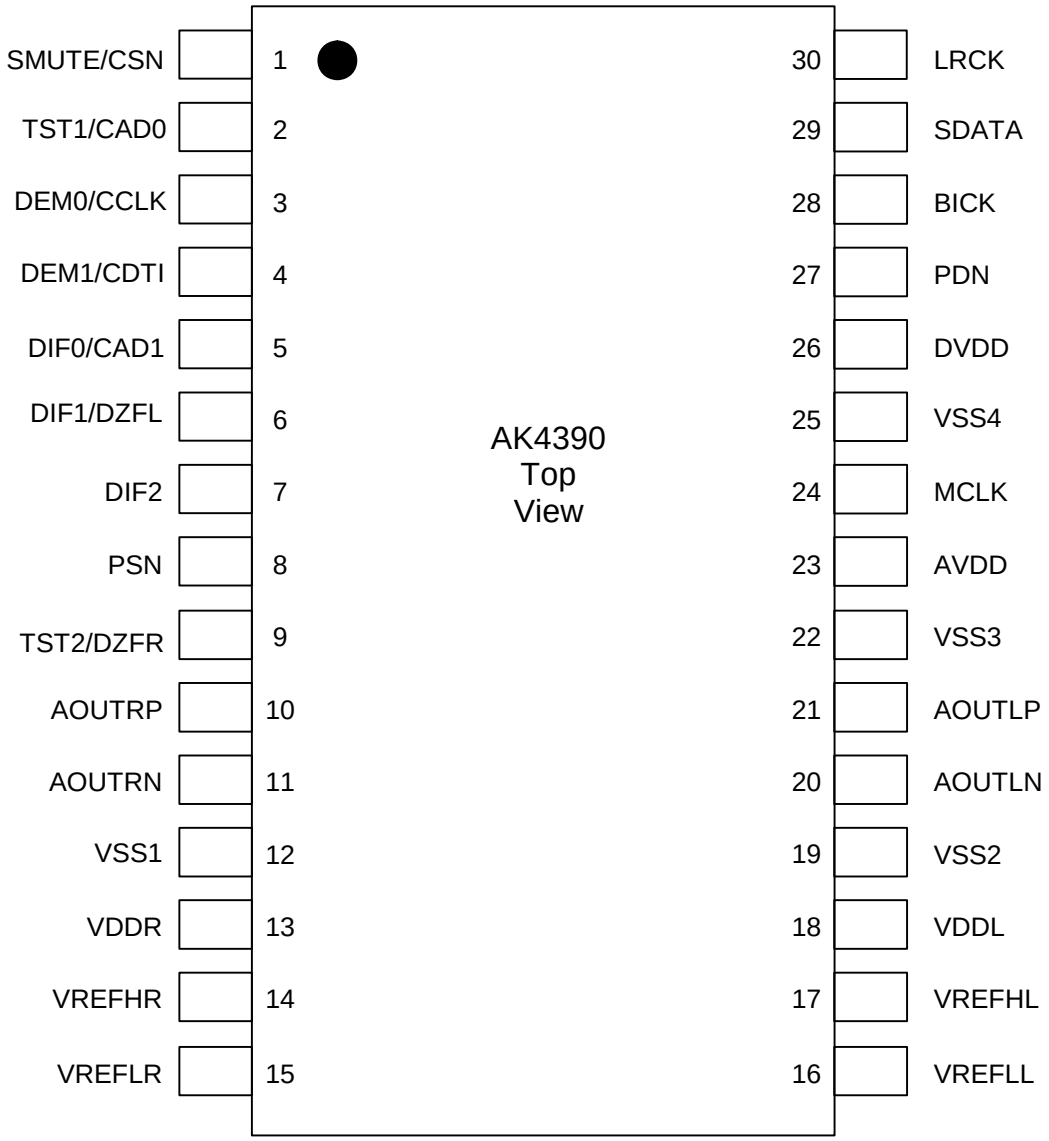


Block Diagram

■ Ordering Guide

AK4390EF	–10 ~ +70°C	30pin VSOP (0.65mm pitch)
AKD4390	Evaluation Board for AK4390	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SMUTE	I	Soft Mute in Parallel Control Mode When this pin goes to "H", soft mute cycle is initiated. When returning to "L", the output mute releases.
	CSN	I	Chip Select in Serial Control Mode
2	TST1	I	Test Pin in Parallel Control Mode (Internal pull-down pin)
	CAD0	I	Chip Address 0 in Serial Control Mode (Internal pull-down pin)
3	DEM0	I	De-emphasis Enable 0 in Parallel Control Mode
	CCLK	I	Control Data Clock in Serial Control Mode
4	DEM1	I	De-emphasis Enable 1 in Parallel Control Mode
	CDTI	I	Control Data Input in Serial Control Mode
5	DIF0	I	Digital Input Format 0 in Parallel Control Mode
	CAD1	I	Chip Address 1 in Serial Control Mode
6	DIF1	I	Digital Input Format 1 Parallel Control Mode
	DZFL	O	Left Channel Zero Input Detect in Serial Control Mode
7	DIF2	I	Digital Input Format 2 in Parallel Control Mode
8	PSN	I	Parallel/Serial Select (Internal pull-up pin) "L": Serial Control Mode, "H": Parallel Control Mode
9	TST2	I	Test pin in Parallel Control Mode. Connect to GND.
	DZFR	O	Rch Zero Input Detect in Serial Control Mode
10	AOUTRP	O	Right Channel Positive Analog Output
11	AOUTRN	O	Right Channel Negative Analog Output
12	VSS1	-	Connected to VSS2/3/4 Ground
13	VDDR	-	Right Channel Analog Power Supply, 4.75~5.25V
14	VREFHR	I	Right Channel High Level Voltage Reference Input
15	VREFLR	I	Right Channel Low Level Voltage Reference Input
16	VREFLL	I	Left Channel Low Level Voltage Reference Input
17	VREFHL	I	Left Channel High Level Voltage Reference Input
18	VDDL	-	Left Channel Analog Power Supply, 4.75~5.25V
19	VSS2	-	Ground (connected to VSS1/3/4 ground)
20	AOUTLN	O	Left Channel Negative Analog Output
21	AOUTLP	O	Left Channel Positive Analog Output
22	VSS3	-	Ground (connected to VSS1/2/4 ground)
23	AVDD	-	Analog Power Supply, 4.75 to 5.25V
24	MCLK	I	Master Clock Input
25	VSS4	-	Connected to VSS1/2/3 Ground
26	DVDD	-	Digital Power Supply, 4.75 ~ 5.25V
27	PDN	I	Power-Down Mode When at "L", the AK4390 is in power-down mode and is held in reset. The AK4390 should always be reset upon power-up.
28	BICK	I	Audio Serial Data Clock
29	SDATA	I	Audio Serial Data Input
30	LRCK	I	L/R Clock

Note: All input pins except internal pull-up/down pins should not be left floating.

■ Handling of Unused Pin

The following tables illustrate recommended states for open pins:

(1) Parallel Control Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	Leave open.
	AOUTRP, AOUTRN	Leave open.
Digital	SMUTE	Connect to VSS4.

(2) Serial Control Mode

Classification	Pin Name	Setting
Analog	AOUTLP, AOUTLN	Leave open.
	AOUTRP, AOUTRN	Leave open.
Digital	DIF2	Connect to VSS4.
	DZFL, DZFR	Leave open.

ABSOLUTE MAXIMUM RATINGS

(VSS1 = VSS2 = VSS3 = VSS4 = 0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	6.0	V
	Analog	VDDL/R	–0.3	6.0	V
	Digital	DVDD	–0.3	6.0	V
Input Current, Any pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (Power applied)		Ta	–10	70	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS1/2/3/4 must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(VSS1 = VSS2 = VSS3 = VSS4 =0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	AVDD	4.75	5.0	5.25	V
(Note 3)	Analog	VDDL/R	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	5.25	V
Voltage Reference	"H" voltage reference	VREFHL/R	AVDD-0.5	-	AVDD	V
(Note 4)	"L" voltage reference	VREFLL/R	VSS3	-	-	V
	VREFH-VREFL	Δ VREF	3.0	-	AVDD	V

Note 1. All voltages with respect to ground.
Note 3. The power up sequence between AVDD and DVDD is not critical.
Note 4. Analog output voltage scales with the voltage of (VREFH – VREFL).
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp× (VREFHL/R – VREFLL/R)/5.

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=DVDD=5.0V; VSS1 = VSS2 = VSS3 = VSS4 =0V; VREFHL/R=AVDD, VREFLL/R= VSS1=VSS2=VSS3; Input data=24bit; $R_L \geq 1k\Omega$; BICK=64fs; Input Signal Frequency = 1kHz; Sampling Frequency = 44.1kHz; Measurement bandwidth = 20Hz ~ 20kHz; External Circuit: Figure 15; unless otherwise specified.)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics (Note 5)						
THD+N	fs=44.1kHz	0dBFS		–103	93	dB
	BW=20kHz	–60dBFS		–57	-	dB
	fs=96kHz	0dBFS		–100	-	dB
	BW=40kHz	–60dBFS		–54	-	dB
	fs=192kHz	0dBFS		–100	-	dB
	BW=40kHz	–60dBFS		–54	-	dB
	BW=80kHz	–60dBFS		–51	-	dB
Dynamic Range (–60dBFS with A-weighted) (Note 6)			114	120		dB
S/N (A-weighted) (Note 7)			114	120		dB
Interchannel Isolation (1kHz)			110	120		dB
DC Accuracy						
Interchannel Gain Mismatch				0.15	0.3	dB
Gain Drift (Note 8)				20	-	ppm/°C
Output Voltage (Note 9)			±2.65	±2.8	±2.95	Vpp
Load Capacitance					25	pF
Load Resistance (Note 10)			1			kΩ
Power Supplies						
Power Supply Current						
Normal operation (PDN pin = "H")						
AVDD, VDDL/R				60	90	mA
DVDD (fs ≤ 96kHz)				43	-	mA
DVDD (fs = 192kHz)				46	70	mA
Power down (PDN pin = "L") (Note 11)						
AVDD+DVDD				10	100	μA

Note 5. Measured by Audio Precision, System Two. Averaging mode. Refer to the evaluation board manual.
Note 6. By Figure 15. External LPF Circuit Example 2.101dB for 16-bit data and 118dB for 20-bit data.
Note 7. By Figure 15. External LPF Circuit Example 2. S/N does not depend on input word length.
Note 8. The voltage on (VREFHL/R – VREFLL/R) is held +5V externally.
Note 9. Full-scale voltage(0dB). Output voltage scales with the voltage of (VREFHL/R – VREFLL/R).
AOUT (typ.@0dB) = (AOUT+) – (AOUT–) = ±2.8Vpp × (VREFHL/R – VREFLL/R)/5.
Note 10. For AC-load. 1.5kΩ for DC-Load
Note 11. In the power-down mode. PSN pin = DVDD, and all other digital input pins including clock pins (MCLK, BICK and LRCK) are held VSS4.
Note 12. PSR is applied to AVDD, DVDD with 1kHz, 100mVpp. The VREFHL/R pin is held +5V.

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit ="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 14)	±0.01dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 13)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 14)		GD	-	36	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 13)	±0.01dB	PB	0		43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 13)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	95			dB
Group Delay (Note 14)		GD	-	36	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

SHARP ROLL-OFF FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="0")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 13)	±0.01dB	PB	0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 13)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	90			dB
Group Delay (Note 14)		GD	-	36	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/−1	-	dB

Note 13. The passband and stopband frequencies scale with fs. For example, PB=0.4535×fs (@±0.01dB), SB=0.546×fs.
Note 14. The calculating delay time which occurred by digital filtering. This time is from setting the 16/20/24bit data of both channels to input register to the output of analog signal.

Minimum Delay FILTER CHARACTERISTICS (fs = 44.1kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Normal Speed Mode; DEM=OFF; SD bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 14)	±0.01dB	PB	0		20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 13)		SB	24.1			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	100			dB
Group Delay (Note 14)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 20.0kHz			-	±0.2	-	dB

Minimum Delay FILTER CHARACTERISTICS (fs = 96kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Double Speed Mode; DEM=OFF; SD bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 13)	±0.01dB	PB	0		43.5	kHz
	−6.0dB		-	48.0	-	kHz
Stopband (Note 13)		SB	52.5			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	95			dB
Group Delay (Note 14)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 40.0kHz			-	±0.3	-	dB

Minimum Delay FILTER CHARACTERISTICS (fs = 192kHz)

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V; Quad Speed Mode; DEM=OFF; SD bit="1")

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband (Note 13)	±0.01dB	PB	0		87.0	kHz
	−6.0dB		-	96.0	-	kHz
Stopband (Note 13)		SB	105			kHz
Passband Ripple		PR			±0.005	dB
Stopband Attenuation		SA	90			dB
Group Delay (Note 14)		GD	-	7	-	1/fs
Digital Filter + SCF						
Frequency Response : 0 ~ 80.0kHz			-	+0/−1	-	dB

DC CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	2.4	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout = −100μA)	VOH	DVDD−0.5	-	-	V
Low-Level Output Voltage (Iout = 100μA)	VOL	-	-	0.5	V
Input Leakage Current (Note 15)	Iin	-	-	±10	μA

Note 15. TST1/CAD0 and PSN pins have internal pull-up devices, nominally 100kΩ. Therefore, TST1/CAD0 and PSN pins are not included in this specification.

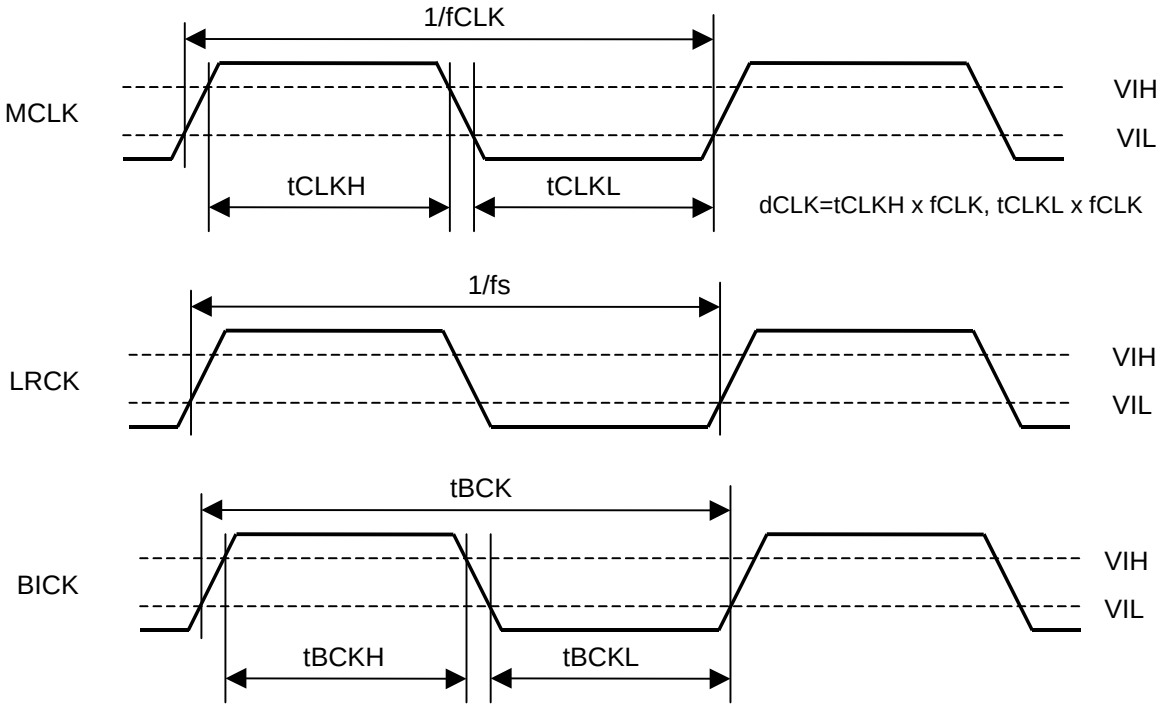
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=VDDL/R=4.75 ~ 5.25V, DVDD=4.75 ~ 5.25V)

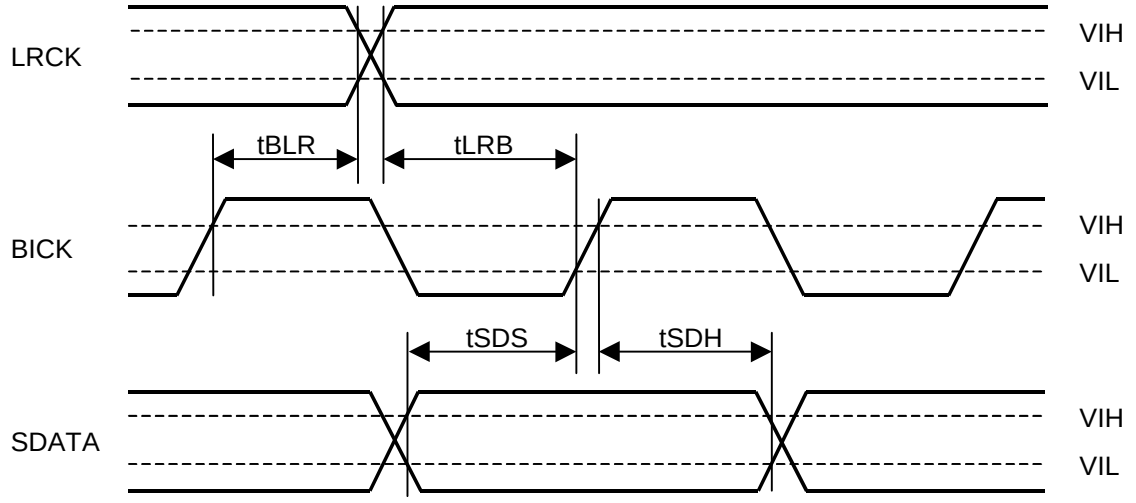
Parameter		Symbol	min	typ	max	Units
Master Clock Timing						
Frequency		fCLK	7.7		41.472	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency	(Note 16)					
Normal Speed Mode		fsn	30		54	kHz
Double Speed Mode		fsd	30		108	kHz
Quad Speed Mode		fsq	108		216	kHz
Duty Cycle		Duty	45		55	%
PCM Audio Interface Timing						
BICK Period						
Normal Speed Mode		tBCK	1/128fn			ns
Double Speed Mode		tBCK	1/64fd			ns
Quad Speed Mode		tBCK	1/64fq			ns
BICK Pulse Width Low		tBCKL	30			ns
BICK Pulse Width High		tBCKH	30			ns
BICK "↑" to LRCK Edge	(Note 17)	tBLR	20			ns
LRCK Edge to BICK "↑"	(Note 17)	tLRB	20			ns
SDATA Hold Time		tSDH	20			ns
SDATA Setup Time		tSDS	20			ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	50			ns
CDTI Hold Time		tCDH	50			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 18)	tPD	150			ns

Note 16. When the frequency (1152fs, 512fs or 768fs /256fs or 384fs /128fs or 192fs) is switched, the AK4390 should be reset by the PDN pin or RSTN bit.
Note 17. BICK rising edge must not occur at the same time as LRCK edge.
Note 18. The AK4390 can be reset by bringing the PDN pin "L" to "H".

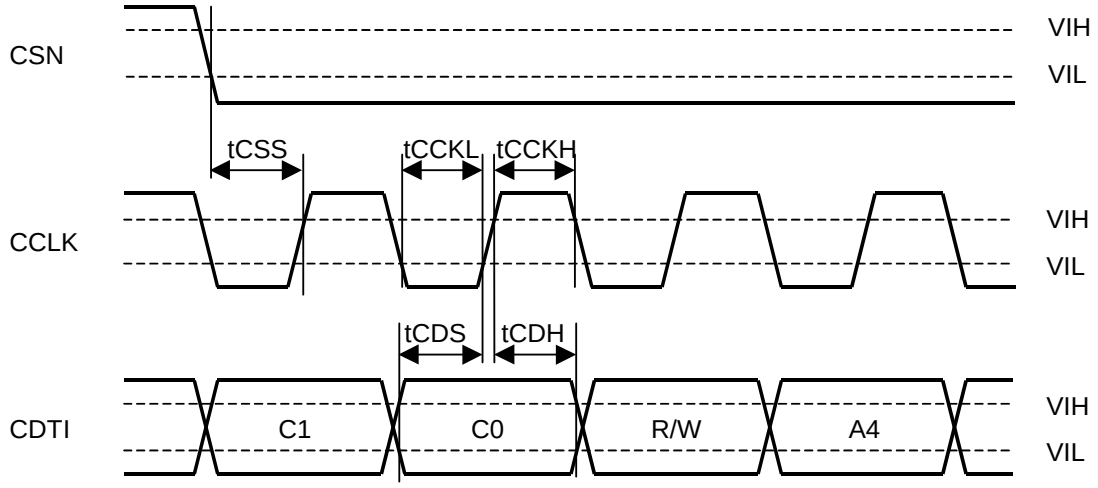
■ **Timing Diagram**



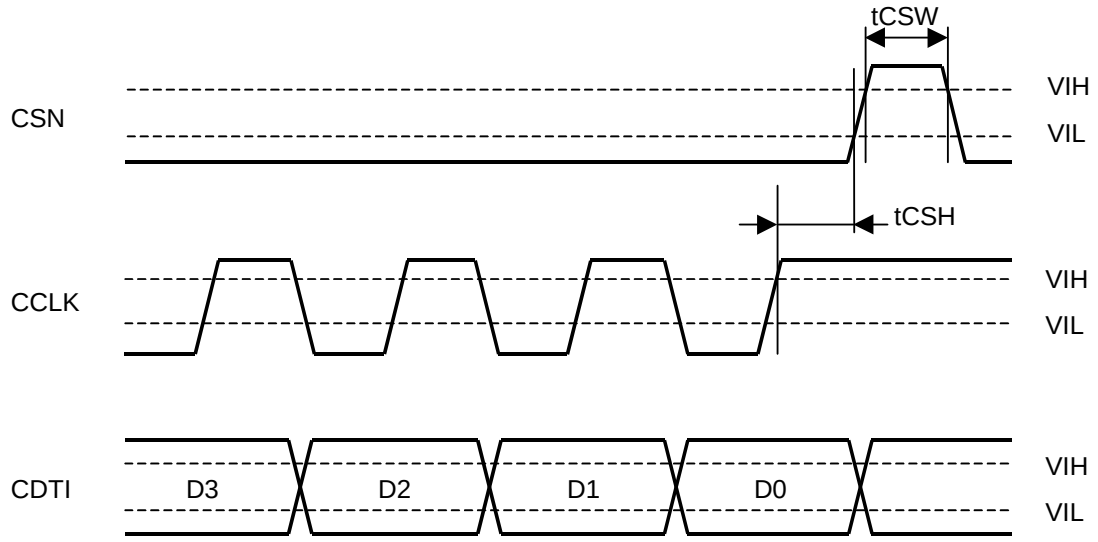
Clock Timing



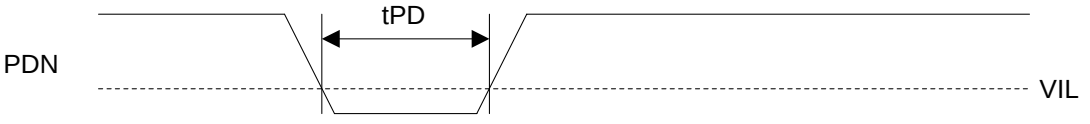
Audio Interface Timing (PCM Mode)



WRITE Command Input Timing



WRITE Data Input Timing



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock

The external clocks, which are required to operate the AK4390, are MCLK, BICK and LRCK. MCLK should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. Sampling speed and MCLK frequency are detected automatically and then the initial master clock is set to the appropriate frequency (Table 1). When external clocks are changed, the AK4390 should be reset by the PDN pin or RSTN bit. After exiting reset (PDN pin = "L" → "H") at power-up etc., the AK4390 is in power-down mode until MCLK is supplied.

The AK4390 is automatically placed in power saving mode when MCLK and LRCK stop during normal operation mode, and the analog output is AVDD/2 (typ). When MCLK and LRCK are input again, the AK4390 is powered up. After power-up, the AK4390 is in the power-down mode until MCLK and LRCK are input.

The MCLK frequency corresponding to each sampling speed should be provided (Table 2).

MCLK		Mode	Sampling Rate
1152fs		Normal	30kHz~32kHz
512fs	768fs	Normal	30kHz~54kHz
256fs	384fs	Double	30kHz~108kHz
128fs	192fs	Quad	108kHz~216kHz

Table 1. Sampling Speed

LRCK	MCLK (MHz)						
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs
32.0kHz	N/A	N/A	8.1920	12.2880	16.3840	24.5760	36.8640
44.1kHz	N/A	N/A	11.2896	16.9344	22.5792	33.8688	N/A
48.0kHz	N/A	N/A	12.2880	18.4320	24.5760	36.8640	N/A
88.2kHz	N/A	N/A	22.5792	33.8688	N/A	N/A	N/A
96.0kHz	N/A	N/A	24.5760	36.8640	N/A	N/A	N/A
176.4kHz	22.5792	33.8688	N/A	N/A	N/A	N/A	N/A
192.0kHz	24.5760	36.8640	N/A	N/A	N/A	N/A	N/A

Table 2. System Clock Example (N/A: Not available)

MCLK= 256fs/384fs supports sampling rate of 30kHz~108kHz (Table 3). But, when the sampling rate is 30kHz~54kHz, DR and S/N will degrade by approximately 3dB as compared to when MCLK= 512fs/768fs.

MCLK	DR,S/N
256fs/384fs	117dB
512fs/768fs	120dB

Table 3. Relationship between MCLK frequency and DR, S/N (fs= 44.1kHz)

■ Audio Interface Format

Data is shifted in via the SDATA pin using the BICK and LRCK inputs. Eight data formats are supported, selected by the DIF2-0 pins (Parallel control mode) or DIF2-0 bits (Serial control mode) as shown in Table 4. In all formats the serial data is MSB-first, 2's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 20-bit and 16-bit MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	Input Format	BICK	Figure	
0	0	0	0	16bit LSB justified	≥ 32fs	Figure 1	
1	0	0	1	20bit LSB justified	≥ 48fs	Figure 2	
2	0	1	0	24bit MSB justified	≥ 48fs	Figure 3	(default)
3	0	1	1	24bit I^2S Compatible	≥ 48fs	Figure 4	
4	1	0	0	24bit LSB justified	≥ 48fs	Figure 2	
5	1	0	1	32bit LSB justified	≥ 64fs	Figure 5	
6	1	1	0	32bit MSB justified	≥ 64fs	Figure 5	
7	1	1	1	32bit I^2S Compatible	≥ 64fs	Figure 6	

Table 4. Audio Interface Format

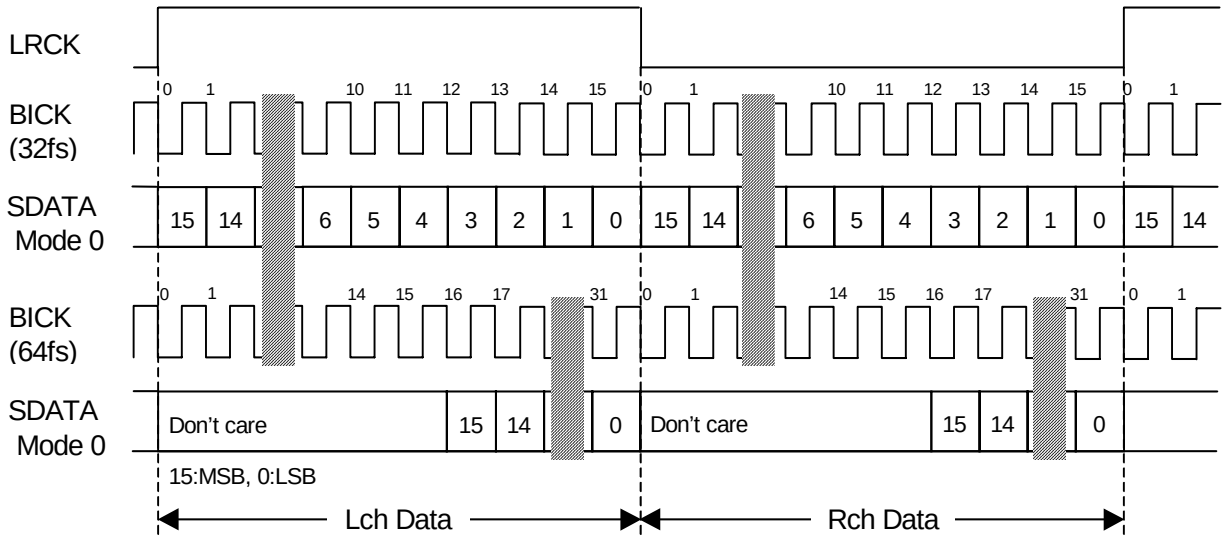


Figure 1. Mode 0 Timing

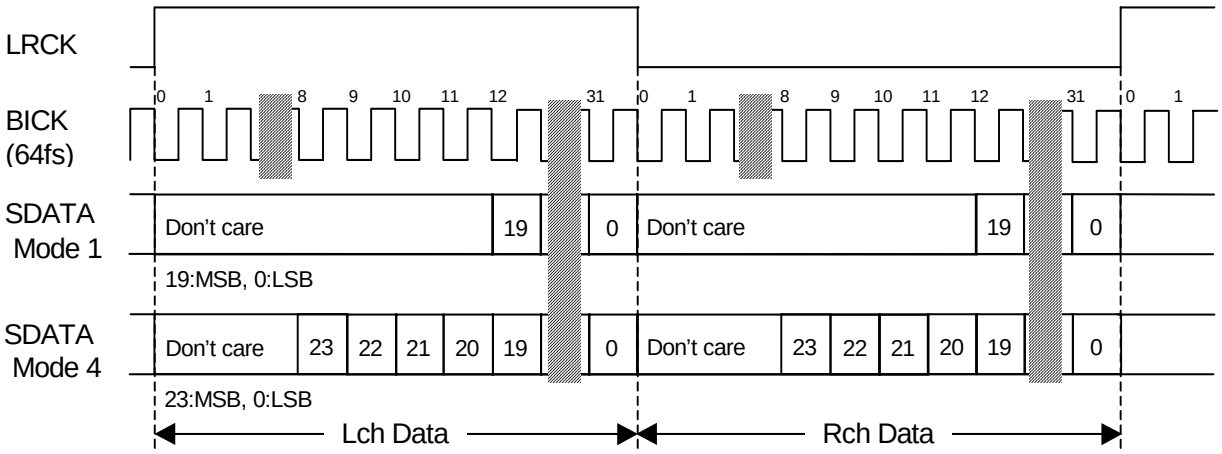


Figure 2. Mode 1/4 Timing

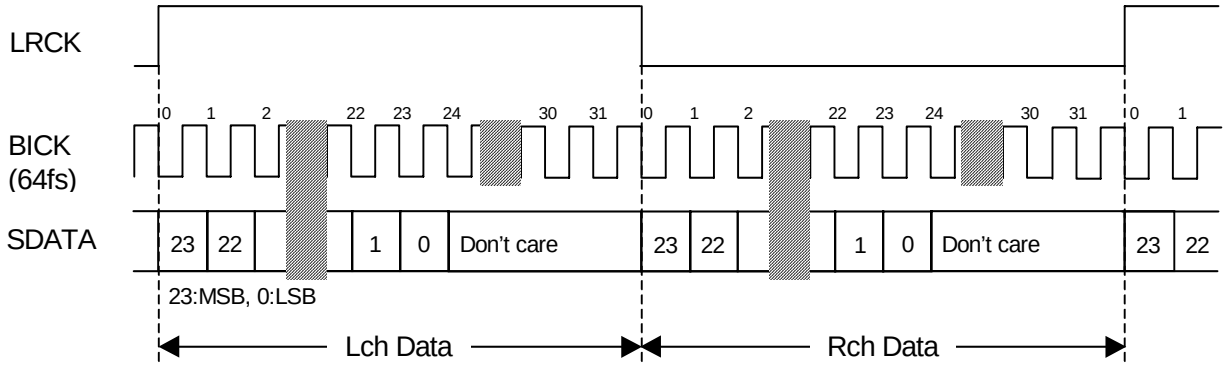


Figure 3. Mode 2 Timing

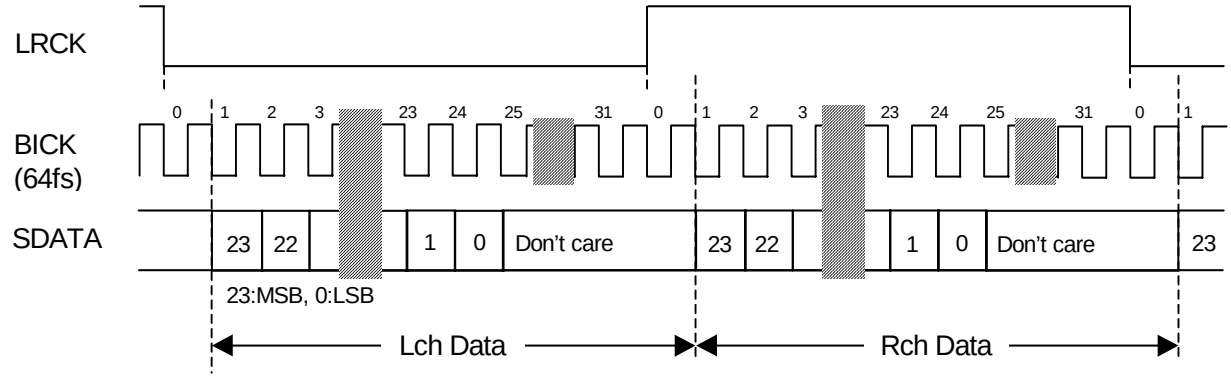


Figure 4. Mode 3 Timing

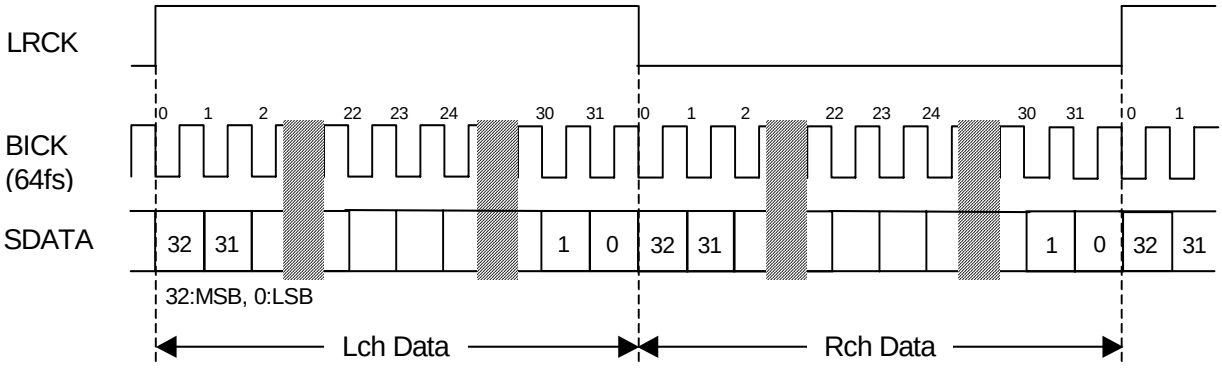


Figure 5. Mode 5/6 Timing

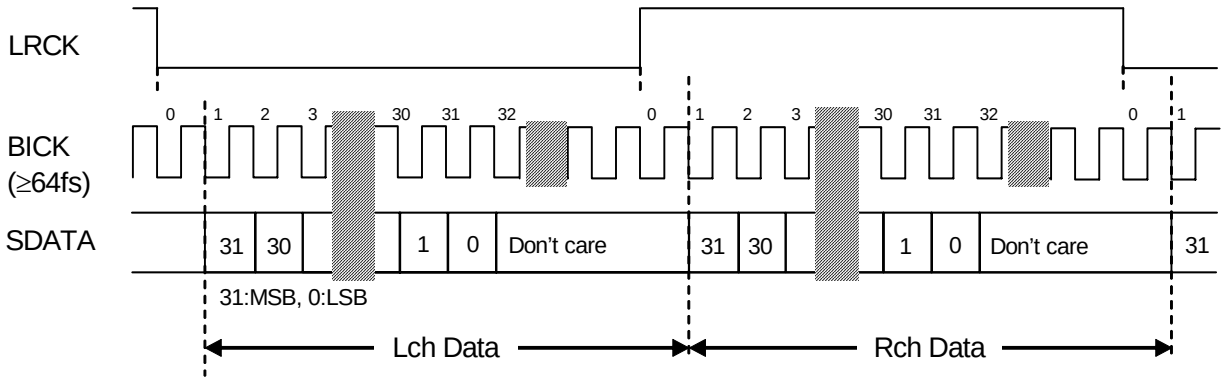


Figure 6. Mode 7 Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32kHz, 44.1kHz or 48kHz sampling rates (tc = 50/15μs) and it is enabled or disabled with the DEM1-0 pins or DEM1-0 bits. For 256fs/384fs and 128fs/192fs, the digital de-emphasis filter is always off.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	(default)
1	0	48kHz	
1	1	32kHz	

Table 5. De-emphasis Control

■ Output Volume Control

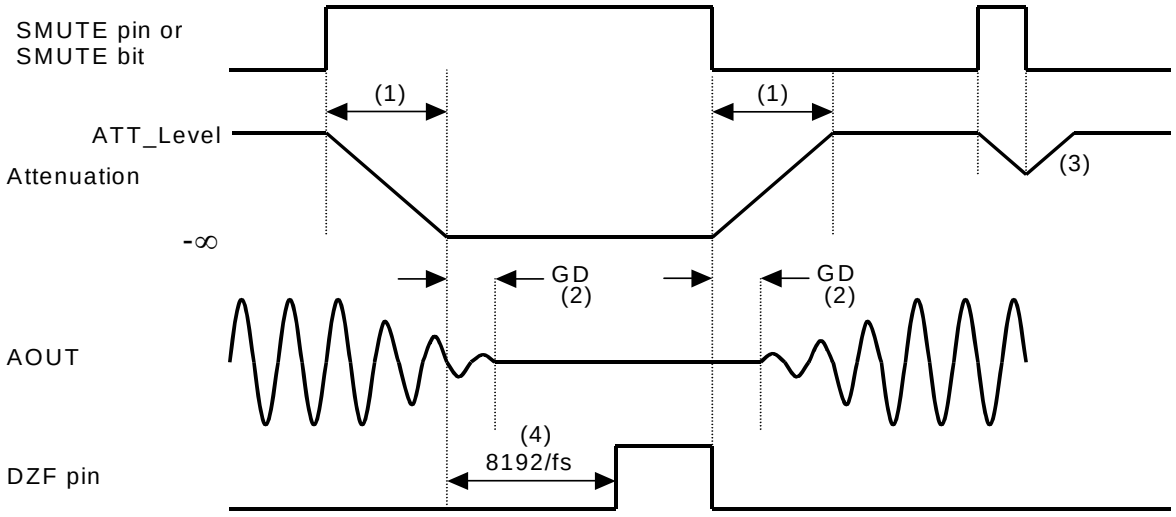
The AK4390 includes channel independent digital output volume control (ATT) with 256 levels at 0.5dB steps including MUTE. The volume control is in front of the DAC, and it can attenuate the input data from 0dB to –127dB and mute. When changing output levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions.

■ Zero Detection

The AK4390 has a channel-independent zero detect function. When the input data for each channel is continuously zero for 8192 LRCK cycles, the DZF pin of each channel goes to "H". The DZF pin of each channel immediately returns to "L" if the input data of either channel is not zero after going to "H". If the RSTN bit is "0", the DZF pins for both channels go to "H". The DZF pins of both channels go to "L" 4 ~ 5/fs after the RSTN bit returns to "1". If the DZFM bit is set to "1", the DZF pins of both channels go to "H" only when the input data for both channels are continuously zero for 8192 LRCK cycles. The zero detect function can be disabled by setting the DZFE bit. In this case, DZF pins of both channels are always "L". The DZFB bit can invert the polarity of the DZF pin.

■ Soft Mute Operation

The soft mute operation is performed in the digital domain. When the SMUTE pin changes to "H" or the SMUTE bit set to "1", the output signal is attenuated by –∞ during ATT_DATA × ATT transition time from the current ATT level. When the SMUTE pin is returned to "L" or the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA × ATT transition time. If the soft mute is cancelled before attenuating –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA × ATT transition time (Table 9). For this example, the time is 1020LRCK cycles (1020/fs) at ATT_DATA=255 in Normal Speed Mode.

(2) Analog output corresponding to digital input has group delay (GD).

(3) If the soft mute is cancelled before attenuating –∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data for each channel is continuously zero for 8192 LRCK cycles, the DZF pin for each channel goes to "H". The DZF pin immediately returns to "L" if the input data are not zero after going "H".

Figure 7. Soft Mute Function

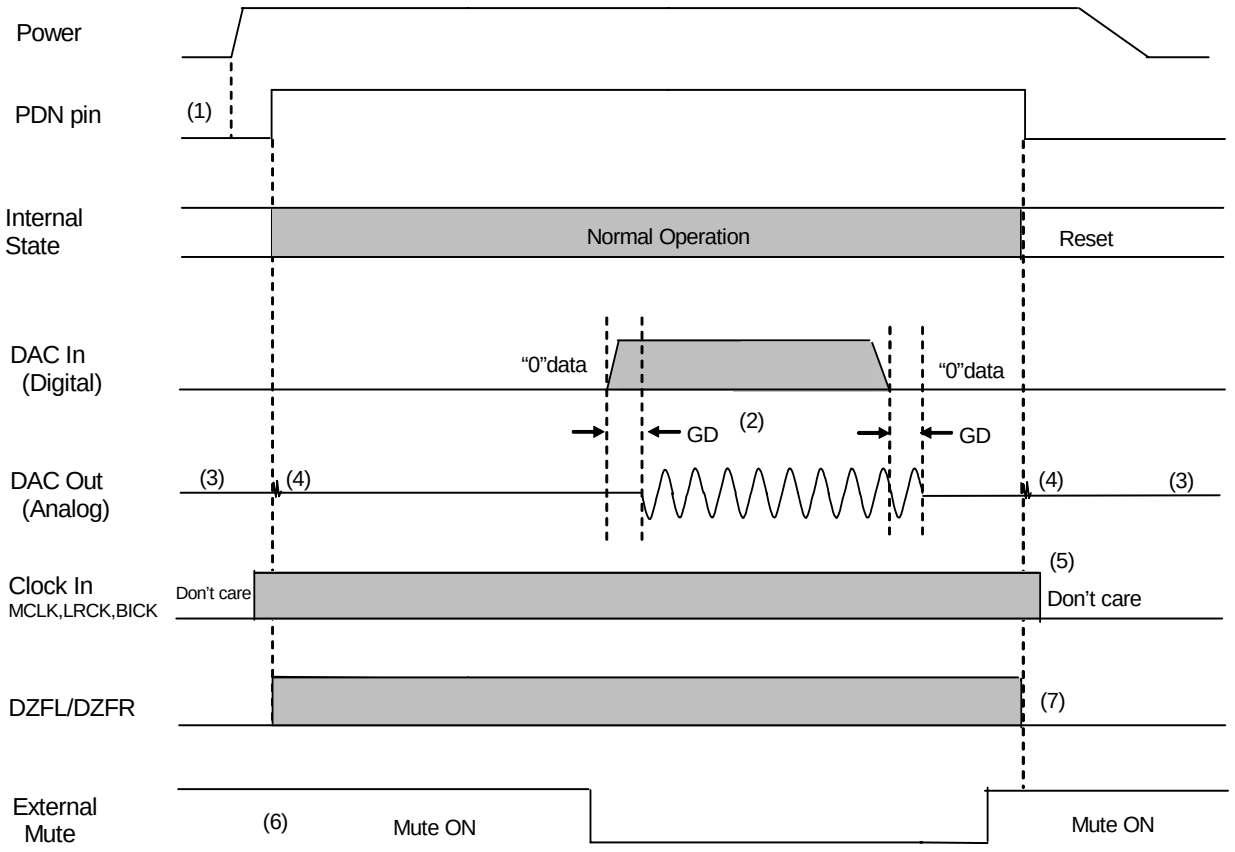
■ System Reset

The AK4390 should be reset once by bringing the PDN pin = "L" upon power-up. The analog section exits power-down mode by MCLK input and then the digital section exits power-down mode after the internal counter counts MCLK during 4/fs.

■ Power ON/OFF timing

The AK4390 is placed in the power-down mode by bringing the PDN pin "L" and the registers are initialized. the analog outputs are floating (Hi-Z). As some click noise occurs at the edge of the PDN pin signal, the analog output should be muted externally if the click noise influences system application.

The DAC can be reset by setting RSTN bit to "0". In this case, the registers are not initialized and the corresponding analog outputs go to AVDD/2 (typ). As some click noise occurs at the edge of RSTN signal, the analog output should be muted externally if click noise aversely affect system performance.



Notes:

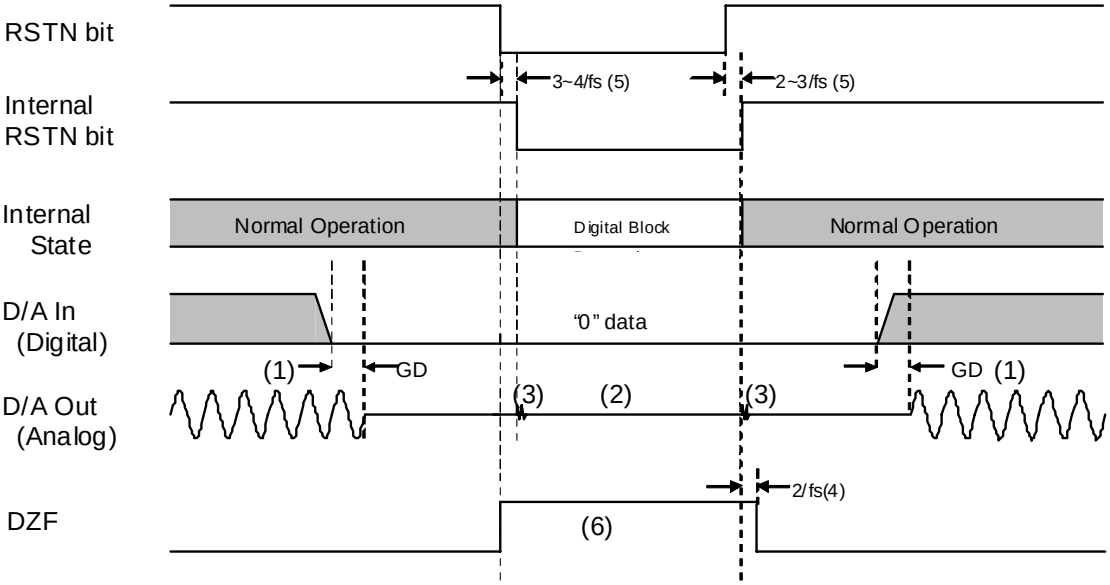
(1) After AVDD and DVDD are powered-up, the PDN pin should be "L" for 150ns.
(2) The analog output corresponding to digital input has group delay (GD).
(3) Analog outputs are floating (Hi-Z) in power-down mode.
(4) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(5) Mute the analog output externally if click noise (3) adversely affect system performance
The timing example is shown in this figure.
(6) DZFL/R pins are "L" in the power-down mode (PDN pin = "L"). (DZFB bit = "0")

Figure 8. Power-down/up Sequence Example

■ Reset Function

(1) RESET by RSTN bit = "0"

When the RSTN bit = "0", the AK4390's digital section is powered down, but the internal register values are not initialized. The analog outputs settle to AVDD/2 (typ) and the DZF pins for both channels go to "H". Figure 9 shows the example of reset by RSTN bit.



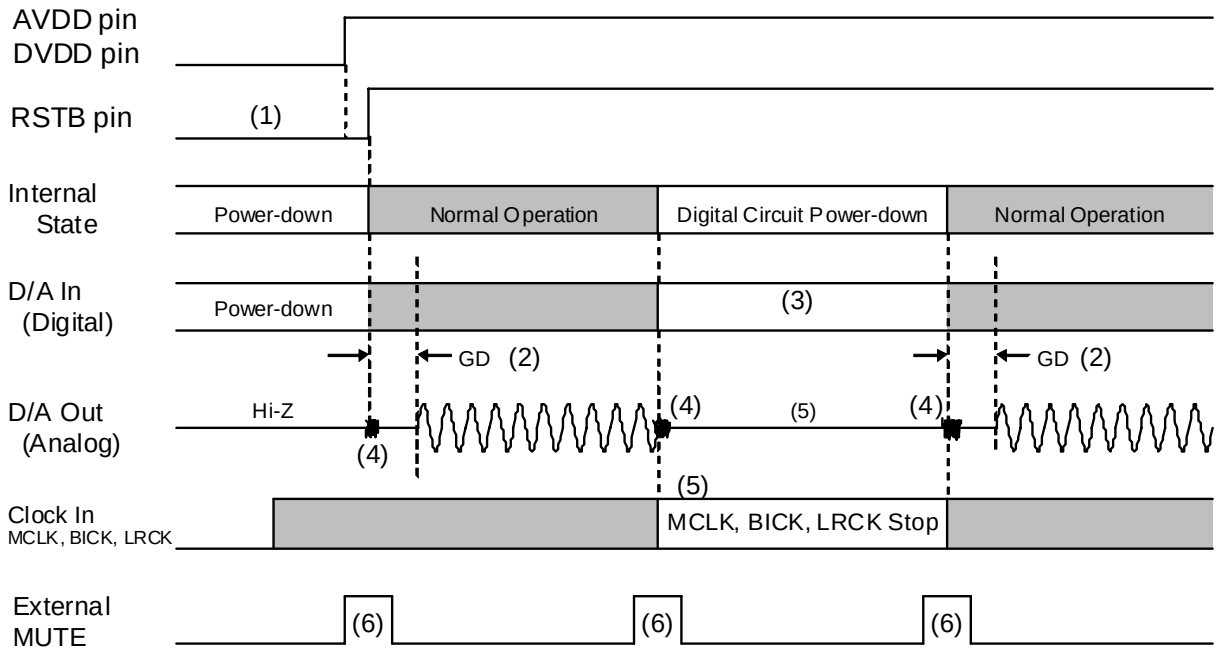
Notes:

(1) The analog output corresponding to digital input has group delay (GD).
(2) Analog outputs settle to AVDD/2 (typ).
(3) Click noise occurs at the edges ("↑ ↓") of the internal timing of RSTN bit.
This noise is output even if "0" data is input.
(4) DZF pins go to "H" when the RSTN bit is set to "0", and return to "L" at 2/fs after the RSTN bit becomes "1".
(5) There is a delay, 3 ~ 4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2 ~ 3/fs from RSTN bit "1" to the internal RSTN bit "1".
(6) Mute the analog output externally if click noise (3) adversely affect system performance

Figure 9. Reset Sequence Example 1

(2) RESET by MCLK or LRCK stop

The AK4390 is automatically placed in reset state when MCLK or LRCK is stopped during normal operation and the analog outputs are floating (Hi-Z). When MCLK and LRCK are input again, the AK4390 exits reset state and starts the operation. Zero detect function is disable when MCLK or LRCK is stopped.



Notes:

(1) After AVDD and DVDD are powered-up, the PDN pin should be held "L" for 150ns.
(2) The analog output corresponding to digital input has the group delay (GD).
(3) Digital data can be stopped. The click noise after MCLK and LRCK are input again can be reduced by inputting the "0" data during this period.
(4) Click noise occurs in 3 ~ 4LRCK cycles ether on a rising edge (↑) of the PDN signal or MCLK inputs. This noise is output even if "0" data is input.
(5) Mute the analog output externally if click noise (4) influences system application. The timing example is shown in this figure.

Figure 10. Reset Sequence Example 2

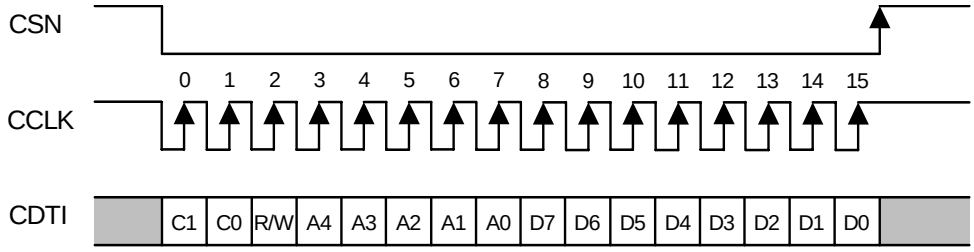
■ Register Control Interface

Pins (parallel control mode) or registers (serial control mode) can control the functions of the AK4390. In parallel control mode, the register setting is ignored, and in serial control mode the pin settings are ignored. When the state of the PSN pin is changed, the AK4390 should be reset by the PDN pin. The serial control interface is enabled by the PSN pin = "L". In this mode, pin settings must be all "L". Internal registers may be written to through3-wire µP interface pins: CSN, CCLK and CDTI. The data on this interface consists of Chip address (2-bits, CAD0/1), Read/Write (1-bit; fixed to "1"), Register address (MSB first, 5-bits) and Control data (MSB first, 8-bits). The AK4390 latches the data on the rising edge of CCLK, so data should be clocked in on the falling edge. The writing of data is valid when CSN "↑". The clock speed of CCLK is 5MHz (max).

Function	Parallel Control Mode	Serial Control Mode
Audio Format	Y	Y
De-emphasis	Y	Y
SMUTE	Y	Y
Minimum delay Filter	-	Y
Digital Attenuator	-	Y

Table 6. Function List (Y: Available, -: Not available)

Setting the PDN pin to "L" resets the registers to their default values. In serial control mode, the internal timing circuit is reset by the RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 11. Control I/F Timing

* The AK4390 does not support the read command.
* When the AK4390 is in power down mode (PDN pin = "L") or the MCLK is not provided, writing into the control register is prohibited.
* The control data can not be written when the CCLK rising edge is 15 times or less or 17 times or more during CSN is "L".

Function List

Function	Default	Address	Bit	PCM
Attenuation Level	0dB	03H 04H	ATT7-0	Y
Audio Data Interface Modes	24bit MSB justified	00H	DIF2-0	Y
Data Zero Detect Enable	Disable	01H	DZFE	Y
Data Zero Detect Mode	Separated	01H	DZFM	Y
Minimum delay Filter Enable	Sharp roll-off filter	01H	SD	Y
De-emphasis Response	OFF	01H	DEM1-0	Y
Soft Mute Enable	Normal Operation	01H	SMUTE	Y
Inverting Enable of DZF	“H” active	02H	DZFB	Y

Table 7. Function List2 (Y: Available, -: Not available)

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	0	0	DIF2	DIF1	DIF0	RSTN
01H	Control 2	DZFE	DZFM	SD	DFS1	DFS0	DEM1	DEM0	SMUTE
02H	Control 3	0	0	0	0	0	DZFB	0	0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0

Notes:

Data must not be written into addresses from 05H to 1FH.

When the PDN pin goes to "L", the registers are initialized to their default values.

When RSTN bit is set to "0", only the internal timing is reset, and the registers are not initialized to their default values.

When the state of the PSN pin is changed, the AK4390 should be reset by the PDN pin.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	0	0	0	0	DIF2	DIF1	DIF0	RSTN
Default		0	0	0	0	0	1	0	1

RSTN: Internal timing reset

0: Reset. All registers are not initialized.

1: Normal Operation (default)

When internal clocks are changed, the AK4390 should be reset by the PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (Table 4)

Initial value is "010" (Mode 2: 24-bit MSB justified).

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	DZFE	DZFM	SD	0	0	DEM1	DEM0	SMUTE
	Default	0	0	0	0	0	0	1	0

SMUTE: Soft Mute Enable
0: Normal Operation (default)
1: DAC outputs soft-muted.

DEM1-0: De-emphasis Response (Table 5)
Initial value is "01" (OFF).

SD: Minimum Delay Filter Enable
0: Sharp roll-off filter (default)
1: Minimum Delay filter

DZFM: Data Zero Detect Mode
0: Channel Separated Mode (default)
1: Channel AND'ed Mode
If the DZFM bit is set to "1", the DZF pins of both channels goes to "H" only when the input data for both channels are continuously zero for 8192 LRCK cycles.

DZFE: Data Zero Detect Enable
0: Disable (default)
1: Enable
The zero detect function can be disabled by DZFE bit "0". In this case, the DZF pins of both channels are always "L".

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Control 3	0	0	0	0	0	DZFB	0	0
	Default	0	0	0	0	0	0	0	0

DZFB: Inverting Enable of DZF
0: DZF pin goes "H" at Zero Detection (default)
1: DZF pin goes "L" at Zero Detection

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	Lch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
04H	Rch ATT	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
	Default	1	1	1	1	1	1	1	1

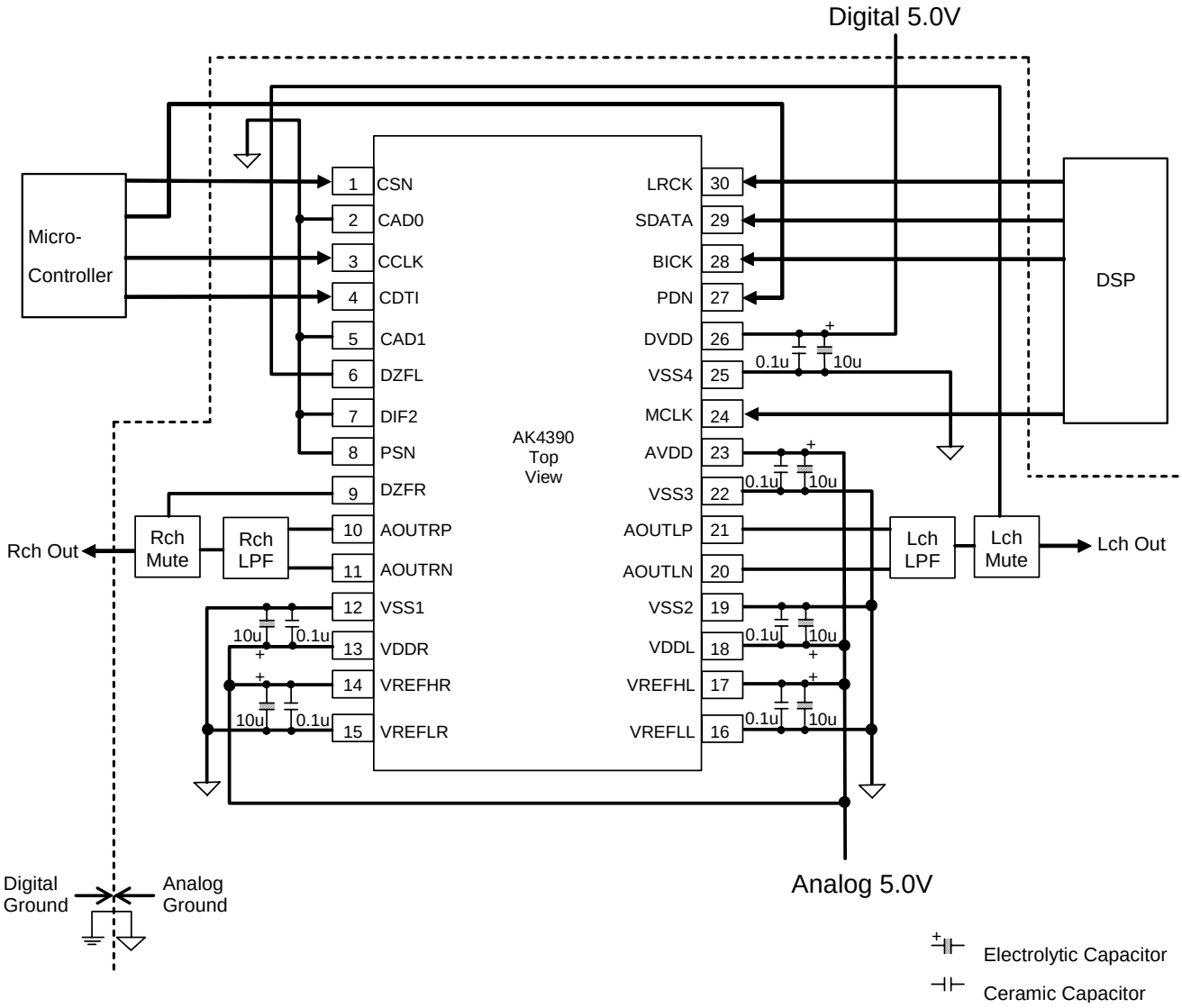
ATT7-0: Attenuation Level
256 levels, 0.5dB step

Data	Attenuation
FFH	0dB
FEH	-0.5dB
FDH	-1.0dB
:	:
:	:
02H	-126.5dB
01H	-127.0dB
00H	MUTE (-∞)

The transition between set values is a soft transition of 7425 levels. It takes 7424/fs (168ms@fs=44.1kHz) from FFH (0dB) to 00H (MUTE). If the PDN pin goes to "L", the ATTs are initialized to FFH. The ATT values are FFH when RSTN = "0". When RSTN return to "1", the ATT values fade to their current value. This digital attenuator is independent of the soft mute function.

SYSTEM DESIGN

Figure 12 shows the system connection diagram. Figure 14 and Figure 15 shows the analog output circuit examples. The evaluation board (AKD4390) demonstrates the optimum layout, power supply arrangements and measurement results.



Notes:

- Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc.
- VSS1/2/3/4 must be connected to the same analog ground plane.
- When AOUT drives a capacitive load, some resistance should be added in series between AOUT and the capacitive load.
- All input pins except pull-down/pull-up pins should not be allowed to float.

Figure 12. Typical Connection Diagram (AVDD=5V, DVDD=5V, Serial Control Mode)

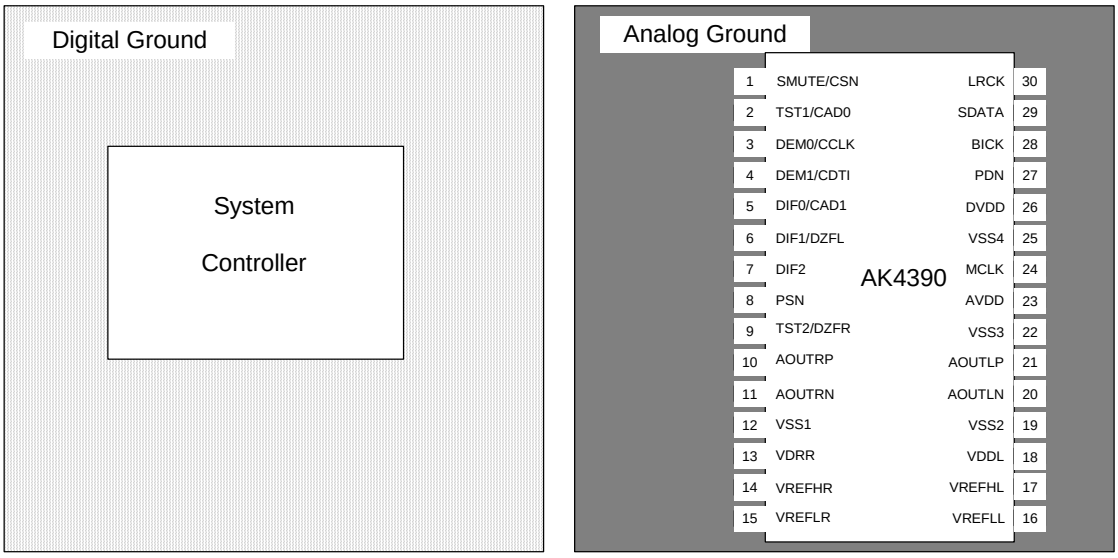


Figure 13. Ground Layout

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from digital supply in system. Power lines of AVDD and DVDD should be distributed separately from the point with low impedance of regulator etc. The power up sequence between AVDD and DVDD is not critical. **VSS1/2/3/4 must be connected to the same analog ground plane.** Decoupling capacitors for high frequency should be placed as near as possible to the supply pin.

2. Voltage Reference

The differential voltage between VREFHL/R and VREFLL/R sets the analog output range. The VREFHL/R pin is normally connected to AVDD, and the VREFLL/R pin is normally connected to VSS1/2/3. VREFHL/R and VREFLL/R should be connected with a 0.1µF ceramic capacitor. All signals, especially clocks, should be kept away from the VREFHL/R and VREFLL/R pins in order to avoid unwanted noise coupling into the AK4390.

3. Analog Outputs

The analog outputs are fully differential outputs at 2.8Vpp (typ, VREFHL/R – VREFLL/R = 5V), centered around AVDD/2 (typ). The differential outputs are summed externally, V_{AOUT} = (AOUT+) – (AOUT–) between AOUT+ and AOUT–. If the summing gain is 1, the output range is 5.6Vpp (typ, VREFHL/R – VREFLL/R = 5V). The bias voltage of the external summing circuit is supplied externally. The input data format is two's complement. The output voltage (V_{AOUT}) is positive full scale for 7FFFFFH (@24-bits) and negative full scale for 800000H (@24-bits). The ideal V_{AOUT} is 0V for 000000H(@24-bits).

The internal switched-capacitor filters attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Figure 14 shows an example of an external LPF circuit summing the differential outputs with an op-amp. Figure 15 shows an example of differential outputs and a LPF circuit example by three op-amps.

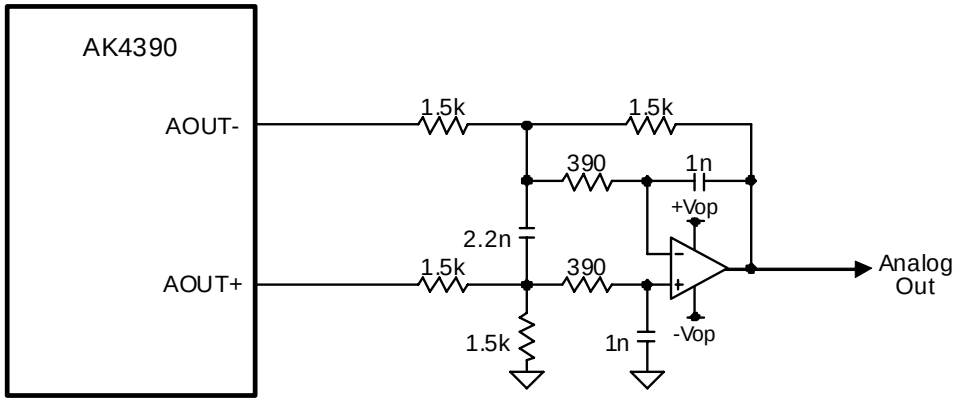


Figure 14. External LPF Circuit Example 1 for PCM (fc = 99.2kHz, Q=0.704)

Frequency Response	Gain
20kHz	–0.011dB
40kHz	–0.127dB
80kHz	–1.571dB

Table 8. Filter Response of External LPF Circuit Example 1 for PCM

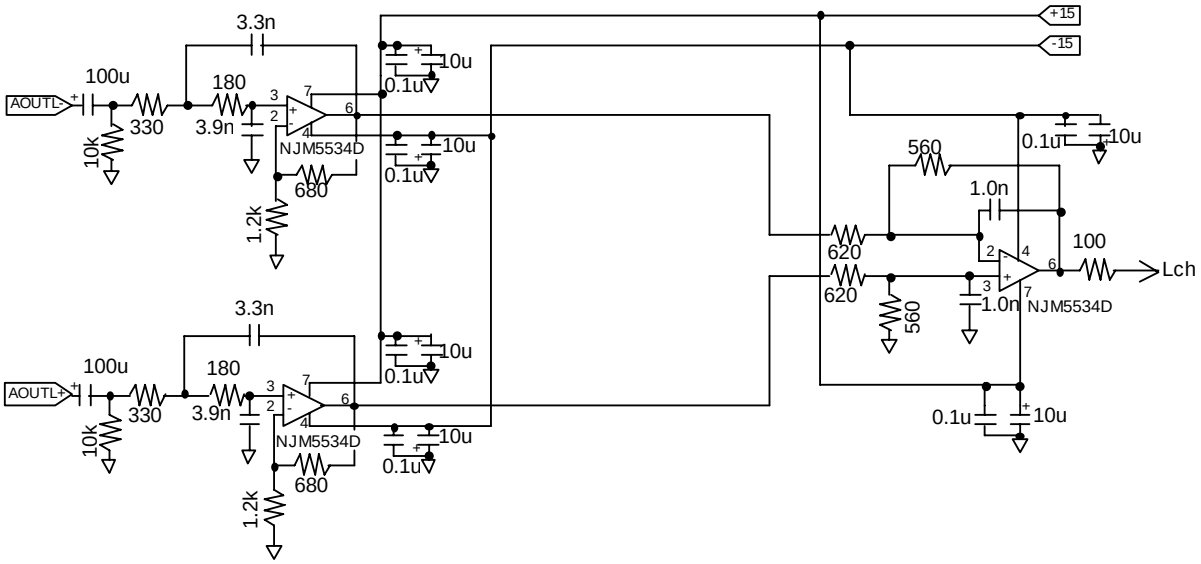


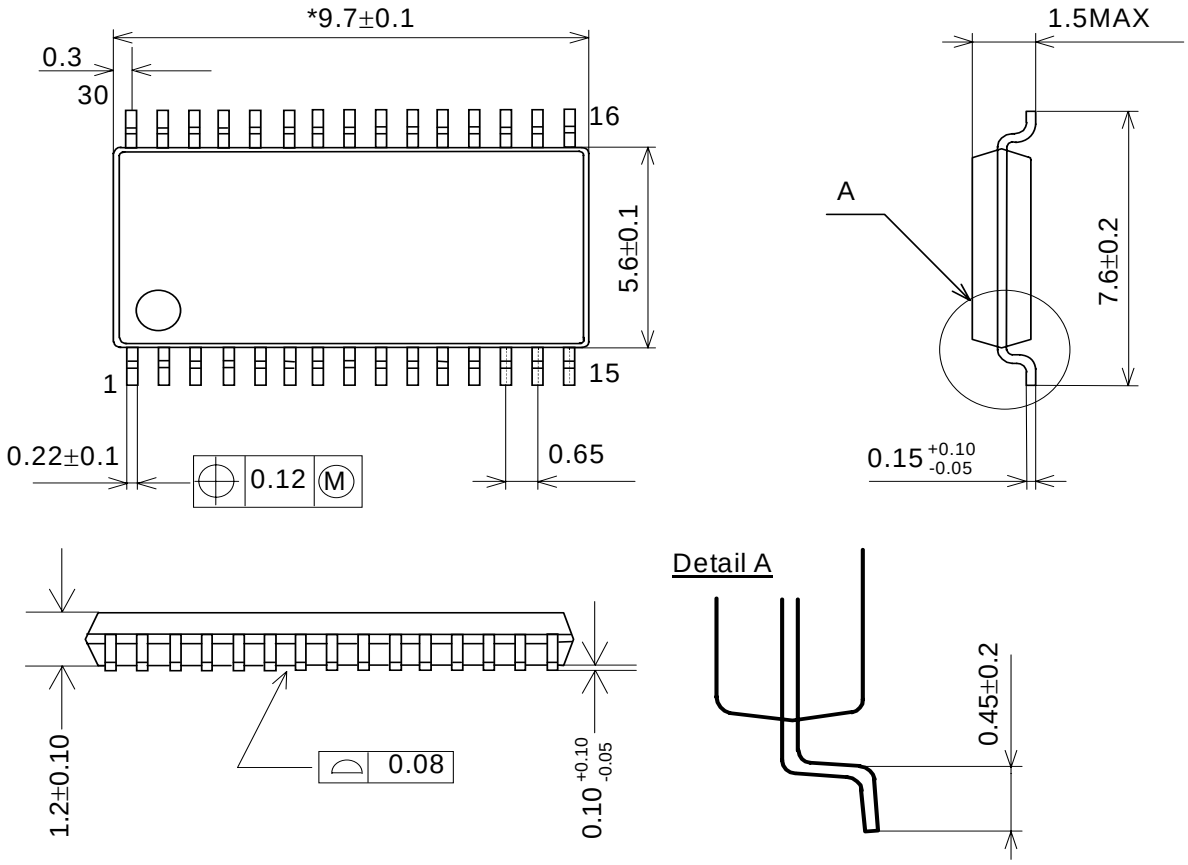
Figure 15. External LPF Circuit Example 2 for PCM

		1st Stage	2nd Stage	Total
Cut-off Frequency		182kHz	284kHz	-
Q		0.637	-	-
Gain		+3.9dB	-0.88dB	+3.02dB
Frequency Response	20kHz	-0.025	-0.021	-0.046dB
	40kHz	-0.106	-0.085	-0.191dB
	80kHz	-0.517	-0.331	-0.848dB

Table 9. Filter Response of External LPF Circuit Example 2 for PCM

PACKAGE

30pin VSOP (Unit: mm)



NOTE: Dimension "*" does not include mold flash.

■ Material & Lead finish

Package molding compound: Epoxy, Halogen (bromine and chlorine) free
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING

XXXXXXXXX Date code identifier

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
09/01/09	00	First Edition		
09/02/05	01	Error Correct	4	PIN/FUNCTION Pin No.5, 6, 7 "PCM Mode" → "Parallel Control Mode" Pin No. 28, 29, 30 "PCM Mode" was deleted.
			17	■ De-emphasis Filter Descriptions about DSD mode were deleted.
			22	■ Register Control Interface Table 6 was changed.
			23	Table 7 was changed.
		Description Addition	30	■ Material & Lead Finish "Halogen (bromine and chlorine) free" was added.
09/02/23	02	Error Correct	29	Figure 14 was changed. Table 8 was changed.
09/04/27	03	Description Change		Short Delay Filter → Minimum Delay Filter

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