**AKM**

**AsahiKASEI**
ASAHI KASEI EMD

**AK5701**

**16-Bit ΔΣ Stereo ADC with PLL & MIC-AMP**

## GENERAL DESCRIPTION

The AK5701 features a 16-bit stereo ADC. Input circuits include a Microphone-Amplifier and an ALC (Auto Level Control) circuit that is suitable for portable application with recording function. On-chip PLL supports base-band clock of mobile phone, therefore it is easy to connect with DSP. The AK5701 is available in a 24pin QFN, utilizing less board space than competitive offerings.

## FEATURES

1. **Resolution: 16bits**
2. **Recording Function**
   - **2 Stereo Input Selector**
   - **Full-differential or Single-ended Input**
   - **MIC Amplifier (+30dB/+15dB or 0dB)**
   - **Input Voltage: 1.8Vpp@VA=3.0V (= 0.6 x AVDD)**
   - **ADC Performance: S/(N+D): 78dB, DR, S/N: 89dB@MGAIN=0dB**
     **S/(N+D): 77dB, DR, S/N: 87dB@MGAIN=+15dB**
     **S/(N+D): 72dB, DR, S/N: 77dB@MGAIN=+30dB**
   - **Digital HPF for DC-offset cancellation (fc=3.4Hz@fs=44.1kHz)**
   - **Digital ALC (Automatic Level Control)**
     **(+36dB ~ −54dB, 0.375dB Step, Mute)**
3. **Sampling Rate:**
   - **PLL Slave Mode (EXLRCK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (EXBCLK pin): 7.35kHz ~ 48kHz**
   - **PLL Slave Mode (MCKI pin):**
     **8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz**
   - **PLL Master Mode:**
     **8kHz, 11.025kHz, 12kHz, 16kHz, 22.05kHz, 24kHz, 32kHz, 44.1kHz, 48kHz**
   - **EXT Slave Mode:**
     **7.35kHz ~ 48kHz (256fs), 7.35kHz ~ 26kHz (512fs), 7.35kHz ~ 13kHz (1024fs)**
4. **PLL Input Clock:**
   - **MCKI pin:**
     **27MHz, 26MHz, 24MHz, 19.2MHz, 13.5MHz, 13MHz, 12.288MHz, 12MHz, 11.2896MHz**
   - **EXLRCK pin: 1fs**
   - **EXBCLK pin: 32fs/64fs**
5. **Master/Slave mode**
6. **Audio Interface Format: MSB First, 2's compliment**
   - **DSP Mode, 16bit MSB justified, I²S**
7. **μP I/F: 3-wire Serial**
8. **Power Supply:**
   - **AVDD: 2.4 ~ 3.6V**
   - **DVDD: 1.6 ~ 3.6V**
9. **Power Supply Current: 8mA**
10. **AK5701VN: Ta = −30 ~ 85°C**
    **AK5701KN: Ta = −40 ~ 85°C**
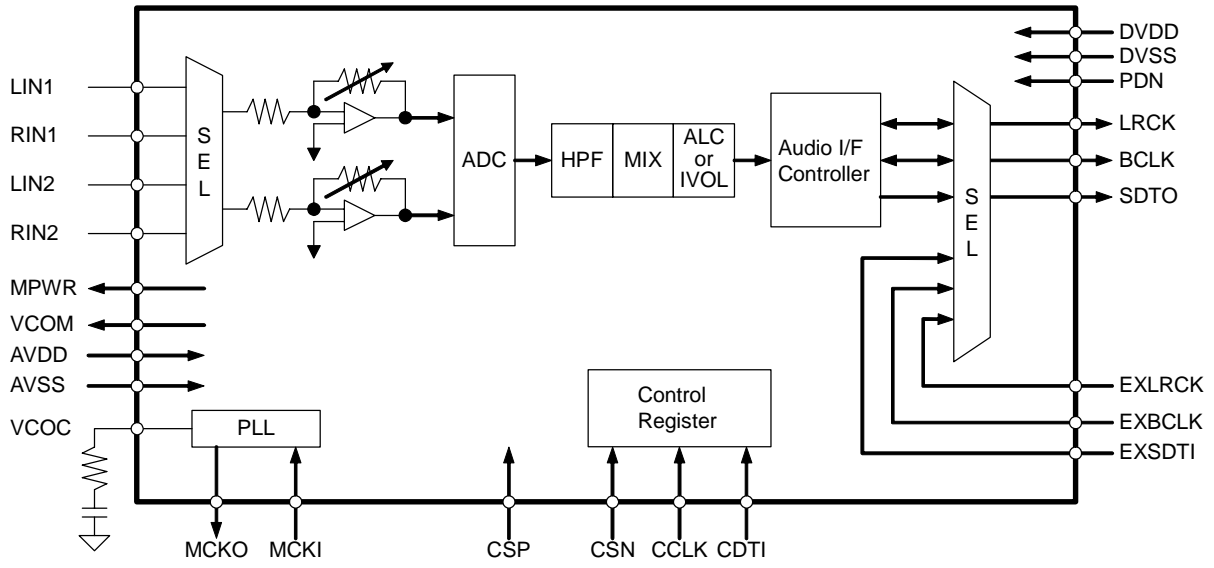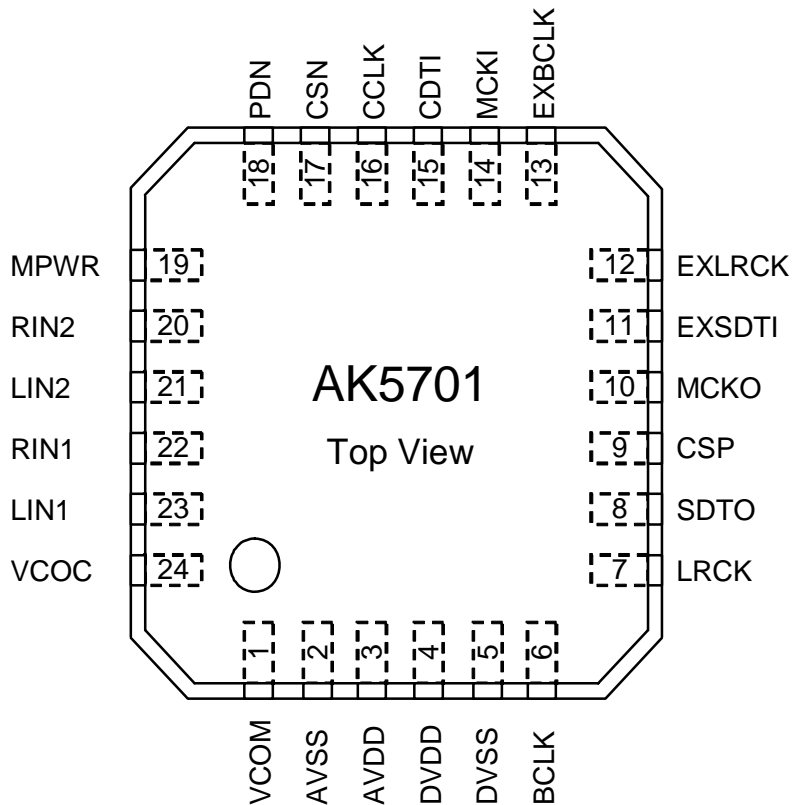11. **Package: 24pin QFN (4mm x 4mm)**

**■ Block Diagram**



Figure 1. Block Diagram

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## ■ Ordering Guide

| | | |
|---|---|---|
| AK5701VN | −30 ~ +85°C | 24pin QFN (0.5mm pitch) |
| AK5701KN | −40 ~ +85°C | 24pin QFN (0.5mm pitch) |
| AKD5701 | Evaluation board for AK5701 | |

## ■ Pin Layout



## ■ Comparison with AK5355VN

| Function | AK5355VN | AK5701 |
|---|---|---|
| Input Selector | No | Yes |
| Input Gain | +15dB/0dB | +30dB/+15dB/0dB |
| Mic Bias | No | Yes |
| ALC | No | Yes |
| Mono Mic Mode | No | Yes |
| Audio I/F Format | Left justified, $I^2$S | DSP Mode, Left justified, $I^2$S |
| PLL | No | Yes |
| Master Mode | No | Yes |
| Output Data Selector | No | Yes |
| Serial Control | No | Yes |
| Power Supply | 2.1 ~ 3.6V | AVDD=2.4 ~ 3.6V<br>DVDD=1.6 ~ 3.6V |
| Package | 20pin QFN (4.2mm x 4.2mm) | 24pin QFN (4mm x 4mm) |
| Ambient Temperature | −40 ~ +85°C | AK5701VN : −30 ~ +85°C<br>AK5701KN : −40 ~ +85°C |

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## PIN/FUNCTION

| No. | Pin Name | I/O | Function |
|---|---|---|---|
| 1 | VCOM | O | Common Voltage Output Pin, 0.5 x AVDD<br>  Bias voltage of ADC inputs. |
| 2 | AVSS | - | Analog Ground Pin |
| 3 | AVDD | - | Analog Power Supply Pin |
| 4 | DVDD | - | Digital Power Supply Pin |
| 5 | DVSS | - | Digital Ground Pin |
| 6 | BCLK | O | Audio Serial Data Clock Pin |
| 7 | LRCK | O | Input / Output Channel Clock Pin |
| 8 | SDTO | O | Audio Serial Data Output Pin |
| 9 | CSP | I | Chip Select Polarity Pin<br>  "H": CSN pin = "H" active, C1-0 = "01"<br>  "L": CSN pin = "L" active, C1-0 = "10" |
| 10 | MCKO | O | Master Clock Output Pin |
| 11 | EXSDTI | I | External Audio Serial Data Input Pin |
| 12 | EXLRCK | I | External Input / Output Channel Clock Pin |
| 13 | EXBCLK | I | External Audio Serial Data Clock Pin |
| 14 | MCKI | I | External Master Clock Input Pin |
| 15 | CDTI | I | Control Data Input Pin |
| 16 | CCLK | I | Control Data Clock Pin (Internal Pull-down at CSP pin = "H") |
| 17 | CSN | I | Chip Select Pin |
| 18 | PDN | I | Power-Down Mode Pin<br>  "H": Power-up, "L": Power-down, reset and initializes the control register. |
| 19 | MPWR | O | MIC Power Supply Pin |
| 20 | RIN2 | I | Rch Analog Input 2 Pin          (MDIF2 bit = "0") |
|    | RIN+ | I | Rch Positive Input Pin          (MDIF2 bit = "1") |
| 21 | LIN2 | I | Lch Analog Input 2 Pin          (MDIF2 bit = "0") |
|    | RIN− | I | Rch Negative Input Pin          (MDIF2 bit = "1") |
| 22 | RIN1 | I | Rch Analog Input 1 Pin          (MDIF1 bit = "0") |
|    | LIN− | I | Lch Negative Input Pin          (MDIF1 bit = "1") |
| 23 | LIN1 | I | Lch Analog Input 1 Pin          (MDIF1 bit = "0") |
|    | LIN+ | I | Lch Positive Input Pin          (MDIF1 bit = "1") |
| 24 | VCOC | O | Output Pin for Loop Filter of PLL Circuit<br>  This pin should be connected to AVSS with one resistor and capacitor in series. |

Note 1. All input pins except analog input pins (LIN1, RIN1, LIN2, RIN2) should not be left floating.


## ■ Handling of Unused Pin

The unused I/O pins should be processed appropriately as below.

| Classification | Pin Name | Setting |
|---|---|---|
| Analog | MPWR, VCOC, LIN1/LIN+, RIN1/LIN−, LIN2/RIN−, RIN2/RIN+ | These pins should be open. |
| Digital | BCLK, LRCK, SDTO, MCKO | These pins should be open. |
|  | MCKI, EXBCLK, EXLRCK, EXSDTI | These pins should be connected to DVSS. |

## ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 2)

| Parameter | | Symbol | min | max | Units |
|---|---|---|---|---|---|
| Power Supplies: | Analog | AVDD | −0.3 | 4.6 | V |
| | Digital | DVDD | −0.3 | 4.6 | V |
| | \|AVSS – DVSS\| (Note 3) | ΔGND | - | 0.3 | V |
| Input Current, Any Pin Except Supplies | | IIN | - | ±10 | mA |
| Analog Input Voltage (Note 4) | | VINA | −0.3 | AVDD+0.3 | V |
| Digital Input Voltage (Note 5) | | VIND | −0.3 | DVDD+0.3 | V |
| Ambient Temperature | AK5701VN | Ta | −30 | 85 | °C |
| (powered applied) | AK5701KN | Ta | −40 | 85 | °C |
| Storage Temperature | | Tstg | −65 | 150 | °C |

Note 2. All voltages with respect to ground.
Note 3. AVSS and DVSS must be connected to the same analog ground plane.
Note 4. LIN1/LIN+, RIN1/LIN−, LIN2/RIN−, RIN2/RIN+ pins
Note 5. PDN, CSN, CCLK, CDTI, CSP, MCKI, EXSDTI, EXLRCK, EXBCLK pins

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 2)

| Parameter | | Symbol | min | typ | Max | Units |
|---|---|---|---|---|---|---|
| Power Supplies | Analog | AVDD | 2.4 | 3.0 | 3.6 | V |
| (Note 6) | Digital | DVDD | 1.6 | 3.0 | AVDD | V |

Note 2. All voltages with respect to ground.
Note 6. The power-up sequence between AVDD and DVDD is not critical. When only AVDD is powered OFF, the power supply current of DVDD at power-down mode may be increased. DVDD should not be powerd OFF while AVDD is powered ON.

* AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=3.0V; AVSS=DVSS=0V; PLL Master Mode; MCKI=12MHz, fs=44.0995kHz, BCLK=64fs; Signal Frequency=1kHz; 16bit Data; Measurement frequency=20Hz ~ 20kHz; unless otherwise specified)

| Parameter | | Min | Typ | max | Units |
|---|---|---|---|---|---|
| **MIC Amplifier:** LIN1, RIN1, LIN2, RIN2 pins; MDIF1 = MDIF2 bits = "0" (Single-ended inputs) | | | | | |
| Input Resistance | MGAIN1-0 bits = "00" | 40 | 60 | 80 | kΩ |
| | MGAIN1-0 bits = "01" or "10" | 20 | 30 | 40 | kΩ |
| Gain | MGAIN1-0 bits = "00" | - | 0 | - | dB |
| | MGAIN1-0 bits = "01" | - | +15 | - | dB |
| | MGAIN1-0 bits = "10" | - | +30 | - | dB |
| **MIC Amplifier:** LIN+, LIN−, RIN+, RIN− pins; MDIF1 = MDIF2 bits = "1" (Full-differential input) | | | | | |
| Input Voltage (Note 7) | | | | | |
| | MGAIN1-0 bits = "01" | - | - | 0.37 | Vpp |
| | MGAIN1-0 bits = "10" | - | - | 0.066 | Vpp |
| **MIC Power Supply:** MPWR pin | | | | | |
| Output Voltage (Note 8) | | 2.02 | 2.25 | 2.48 | V |
| Load Resistance | | 0.5 | - | - | kΩ |
| Load Capacitance | | - | - | 30 | pF |
| **ADC Analog Input Characteristics:** LIN1/RIN1/LIN2/RIN2 pins (Single-ended inputs) → ADC → IVOL, MGAIN=+15dB, IVOL=0dB, ALC=OFF | | | | | |
| Resolution | | - | - | 16 | Bits |
| Input Voltage (Note 9) | MGAIN=+30dB | - | 0.057 | - | Vpp |
| | MGAIN=+15dB | 0.27 | 0.32 | 0.37 | Vpp |
| | MGAIN=0dB | 1.53 | 1.80 | 2.07 | Vpp |
| S/(N+D) (−0.5dBFS) (Note 10) | | 67 | 77 | - | dB |
| D-Range (−60dBFS, A-weighted) (Note 11) | | 79 | 87 | - | dB |
| S/N (A-weighted) (Note 11) | | 79 | 87 | - | dB |
| Interchannel Isolation (Note 12) | | 80 | 90 | - | dB |
| Interchannel Gain Mismatch | MGAIN=+30dB | - | 0.2 | - | dB |
| | MGAIN=+15dB | - | 0.2 | 1.0 | dB |
| | MGAIN=0dB | - | 0.2 | 0.5 | dB |
| **Power Supplies:** | | | | | |
| Power Supply Current: AVDD+DVDD | | | | | |
| Power Up (PDN pin = "H") (Note 13) | | - | 8 | 12 | mA |
| Power Down (PDN pin = "L") (Note 14) | | - | 1 | 20 | μA |

Note 7. The voltage difference between LIN+/RIN+ and LIN−/RIN− pins. AC coupling capacitor should be connected in series at each input pin. Full-differential input is not available at MGAIN1-0 bits = "00". Maximum input voltage of LIN+, LIN−, RIN+ and RIN− pins is proportional to AVDD voltage, respectively.
Vin = |(L/RIN+) − (L/RIN−)| = 0.123 x AVDD (max)@MGAIN1-0 bits = "01", 0.022 x AVDD (max)@MGAIN1-0 bits = "10".
When the signal larger than above value is input to LIN+, LIN−, RIN+ or RIN− pin, ADC does not operate normally.

Note 8. Output voltage is proportional to AVDD voltage. Vout = 0.75 x AVDD (typ).

Note 9. Input voltage is proportional to AVDD voltage. Vin = 0.107 x AVDD (typ)@MGAIN1-0 bits = "01" (+15dB), Vin = 0.6 x AVDD(typ)@MGAIN1-0 bits = "00" (0dB).

Note 10. 80dB(typ)@MGAIN=0dB, 70dB(typ)@MGAIN=+30dB

Note 11. 89dB(typ)@MGAIN=0dB, 77dB(typ)@MGAIN=+30dB

Note 12. 100dB(typ)@MGAIN=0dB, 80dB(typ)@MGAIN=+30dB

Note 13. PLL Master Mode (MCKI=12MHz), PMADL = PMADR = PMVCM = PMPLL = PMMP = M/S bits = "1" and MCKO bit = "0". MPWR pin outputs 0mA. AVDD=6.4mA(typ), DVDD=1.6mA(typ).
EXT Slave Mode (PMPLL = M/S = MCKO bits = "0"): AVDD=5.7mA(typ), DVDD=1.3mA(typ).
Bypass Mode (THR bit = "1", PMADL = PMADR = M/S bits = "0"), fs=8kHz: AVDD=1μA(typ), DVDD=150μA(typ).

Note 14. All digital input pins are fixed to DVDD or DVSS.

**FILTER CHARACTERISTICS**

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V; fs=44.1kHz)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **ADC Digital Filter (Decimation LPF):** | | | | | | |
| Passband (Note 15) | ±0.1dB | PB | 0 | - | 17.4 | kHz |
| | −1.0dB | | - | 20.0 | - | kHz |
| | −3.0dB | | - | 21.1 | - | kHz |
| Stopband (Note 15) | | SB | 25.7 | - | - | kHz |
| Passband Ripple | | PR | - | - | ±0.1 | dB |
| Stopband Attenuation | | SA | 65 | - | - | dB |
| Group Delay (Note 16) | | GD | - | 18 | - | 1/fs |
| Group Delay Distortion | | ΔGD | - | 0 | - | μs |
| **ADC Digital Filter (HPF):** HPF1-0 bits = "00" | | | | | | |
| Frequency Response (Note 15) | −3.0dB | FR | - | 3.4 | - | Hz |
| | −0.5dB | | - | 10 | - | Hz |
| | −0.1dB | | - | 22 | - | Hz |

Note 15. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.454*fs (@−1.0dB). Each response refers to that of 1kHz.
Note 16. The calculated delay time caused by digital filtering. This time is from the input of analog signal to setting of the 16-bit data of both channels from the input register to the output register of the ADC. This time includes the group delay of the HPF.

**DC CHARACTERISTICS**

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| High-Level Input Voltage | | | | | | |
| | Except CSP pin; 2.2V≤ DVDD ≤3.6V | VIH | 70%DVDD | - | - | V |
| | Except CSP pin; 1.6V≤ DVDD <2.2V | VIH | 80%DVDD | - | - | V |
| | CSP pin | VIH | 90%DVDD | - | - | V |
| Low-Level Input Voltage | | | | | | |
| | Except CSP pin; 2.2V≤ DVDD ≤3.6V | VIL | - | - | 30%DVDD | V |
| | Except CSP pin; 1.6V≤ DVDD <2.2V | VIL | - | - | 20%DVDD | V |
| | CSP pin | VIL | - | - | 10%DVDD | V |
| High-Level Output Voltage (Iout= −200μA) | | VOH | DVDD−0.2 | - | - | V |
| Low-Level Output Voltage (Iout= 200μA) | | VOL | - | - | 0.2 | V |
| Input Leakage Current (Note 17) | | Iin | - | - | ±10 | μA |

Note 17. When CSP pin is "H", CCLK pin has internal pull-down device, normally 100kΩ.

**SWITCHING CHARACTERISTICS**

(Ta=25°C; AVDD=2.4 ~ 3.6V; DVDD=1.6 ~ 3.6V; $C_L$=20pF)

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **PLL Master Mode (PLL Reference Clock = MCKI pin)** | | | | | | |
| **MCKI Input Timing** | | | | | | |
| Frequency | | fCLK | 11.2896 | - | 27 | MHz |
| Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
| **MCKO Output Timing** | | | | | | |
| Frequency | | fMCK | 0.2352 | - | 12.288 | MHz |
| Duty Cycle | | | | | | |
| Except 256fs at fs=32kHz, 29.4kHz | | dMCK | 40 | 50 | 60 | % |
| 256fs at fs=32kHz, 29.4kHz | | dMCK | - | 33 | - | % |
| **LRCK Output Timing** | | | | | | |
| Frequency | | | | | | |
| Except DSP Mode 1 | | fs | 7.35 | - | 48 | kHz |
| DSP Mode 1 (Note 18) | | fsd | 14.7 | - | 96 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | - | tBCK | - | ns |
| Except DSP Mode: Duty Cycle | | Duty | - | 50 | - | % |
| **BCLK Output Timing** | | | | | | |
| Period | BCKO1-0 bit = "01" | tBCK | - | 1/(32fs) | - | ns |
| | BCKO1-0 bit = "10" | tBCK | - | 1/(64fs) | - | ns |
| Duty Cycle | | dBCK | - | 50 | - | % |
| **PLL Slave Mode (PLL Reference Clock = MCKI pin)** | | | | | | |
| **MCKI Input Timing** | | | | | | |
| Frequency | | fCLK | 11.2896 | - | 27 | MHz |
| Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
| Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
| **MCKO Output Timing** | | | | | | |
| Frequency | | fMCK | 0.2352 | - | 12.288 | MHz |
| Duty Cycle | | | | | | |
| Except 256fs at fs=32kHz, 29.4kHz | | dMCK | 40 | 50 | 60 | % |
| 256fs at fs=32kHz, 29.4kHz | | dMCK | - | 33 | - | % |
| **EXLRCK Input Timing** | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs − tBCK | ns |
| Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
| **EXBCLK Input Timing** | | | | | | |
| Period | | tBCK | 1/(64fs) | - | 1/(32fs) | ns |
| Pulse Width Low | | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | | tBCKH | 0.4 x tBCK | - | - | ns |
| **PLL Slave Mode (PLL Reference Clock = EXLRCK pin)** | | | | | | |
| **EXLRCK Input Timing** | | | | | | |
| Frequency | | fs | 7.35 | - | 48 | kHz |
| DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs − tBCK | ns |
| Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
| **EXBCLK Input Timing** | | | | | | |
| Period | | tBCK | 1/(64fs) | - | 1/(32fs) | ns |
| Pulse Width Low | | tBCKL | 0.4 x tBCK | - | - | ns |
| Pulse Width High | | tBCKH | 0.4 x tBCK | - | - | ns |

Note 18. Sampling frequency is 7.35kHz ~ 48kHz.

| Parameter | | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|---|
| **PLL Slave Mode (PLL Reference Clock = EXBCLK pin)** | | | | | | |
|   **EXLRCK Input Timing** | | | | | | |
|     Frequency | | fs | 7.35 | - | 48 | kHz |
|     DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs − tBCK | ns |
|     Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
|   **EXBCLK Input Timing** | | | | | | |
|     Period | PLL3-0 bits = "0010" | tBCK | - | 1/(32fs) | - | ns |
| | PLL3-0 bits = "0011" | tBCK | - | 1/(64fs) | - | ns |
|     Pulse Width Low | | tBCKL | 0.4 x tBCK | - | - | ns |
|     Pulse Width High | | tBCKH | 0.4 x tBCK | - | - | ns |
| **External Slave Mode** | | | | | | |
|   **MCKI Input Timing** | | | | | | |
|     Frequency | 256fs | fCLK | 1.8816 | - | 12.288 | MHz |
| | 512fs | fCLK | 3.7632 | - | 13.312 | MHz |
| | 1024fs | fCLK | 7.5264 | - | 13.312 | MHz |
|     Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
|     Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
|   **EXLRCK Input Timing** | | | | | | |
|     Frequency | 256fs | fs | 7.35 | - | 48 | kHz |
| | 512fs | fs | 7.35 | - | 26 | kHz |
| | 1024fs | fs | 7.35 | - | 13 | kHz |
|     DSP Mode: Pulse Width High | | tLRCKH | tBCK−60 | - | 1/fs − tBCK | ns |
|     Except DSP Mode: Duty Cycle | | Duty | 45 | - | 55 | % |
|   **EXBCLK Input Timing** | | | | | | |
|     Period | | tBCK | 312.5 | - | - | ns |
|     Pulse Width Low | | tBCKL | 130 | - | - | ns |
|     Pulse Width High | | tBCKH | 130 | - | - | ns |
| **External Master Mode** | | | | | | |
|   **MCKI Input Timing** | | | | | | |
|     Frequency | 256fs | fCLK | 1.8816 | - | 12.288 | MHz |
| | 512fs | fCLK | 3.7632 | - | 13.312 | MHz |
| | 1024fs | fCLK | 7.5264 | - | 13.312 | MHz |
|     Pulse Width Low | | tCLKL | 0.4/fCLK | - | - | ns |
|     Pulse Width High | | tCLKH | 0.4/fCLK | - | - | ns |
|   **LRCK Output Timing** | | | | | | |
|     Frequency | | fs | 7.35 | - | 48 | kHz |
|     DSP Mode: Pulse Width High | | tLRCKH | - | tBCK | - | ns |
|     Except DSP Mode: Duty Cycle | | Duty | - | 50 | - | % |
|   **BCLK Output Timing** | | | | | | |
|     Period | BCKO1-0 bit = "01" | tBCK | - | 1/(32fs) | - | ns |
| | BCKO1-0 bit = "10" | tBCK | - | 1/(64fs) | - | ns |
|     Duty Cycle | | dBCK | - | 50 | - | % |

| Parameter | Symbol | min | typ | Max | Units |
|---|---|---|---|---|---|
| **Audio Interface Timing (DSP Mode)** | | | | | |
|   **Master Mode** | | | | | |
|     LRCK "↑" to BCLK "↑" (Note 19) | tDBF | 0.5 x tBCK – 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
|     LRCK "↑" to BCLK "↓" (Note 20) | tDBF | 0.5 x tBCK – 40 | 0.5 x tBCK | 0.5 x tBCK + 40 | ns |
|     BCLK "↑" to SDTO (BCKP bit = "0") | tBSD | −70 | - | 70 | ns |
|     BCLK "↓" to SDTO (BCKP bit = "1") | tBSD | −70 | - | 70 | ns |
|   **Slave Mode** | | | | | |
|     EXLRCK "↑" to EXBCLK "↑" (Note 19) | tLRB | 0.4 x tBCK | - | - | ns |
|     EXLRCK "↑" to EXBCLK "↓" (Note 20) | tLRB | 0.4 x tBCK | - | - | ns |
|     EXBCLK "↑" to EXLRCK "↑" (Note 19) | tBLR | 0.4 x tBCK | - | - | ns |
|     EXBCLK "↓" to EXLRCK "↑" (Note 20) | tBLR | 0.4 x tBCK | - | - | ns |
|     EXBCLK "↑" to SDTO (BCKP bit = "0") | tBSD | - | - | 80 | ns |
|     EXBCLK "↓" to SDTO (BCKP bit = "1") | tBSD | - | - | 80 | ns |
| **Audio Interface Timing (Left justified & I²S)** | | | | | |
|   **Master Mode** | | | | | |
|     BCLK "↓" to LRCK Edge (Note 21) | tMBLR | −40 | - | 40 | ns |
|     LRCK Edge to SDTO (MSB)<br>       (Except I²S mode) | tLRD | −70 | - | 70 | ns |
|     BCLK "↓" to SDTO | tBSD | −70 | - | 70 | ns |
|   **Slave Mode** | | | | | |
|     EXLRCK Edge to EXBCLK "↑" (Note 21) | tLRB | 50 | - | - | ns |
|     EXBCLK "↑" to EXLRCK Edge (Note 21) | tBLR | 50 | - | - | ns |
|     EXLRCK Edge to SDTO (MSB)<br>       (Except I²S mode) | tLRD | - | - | 80 | ns |
|     EXBCLK "↓" to SDTO | tBSD | - | - | 80 | ns |

Note 19. MSBS, BCKP bits = "00" or "11"
Note 20. MSBS, BCKP bits = "01" or "10"
Note 21. EXBCLK rising edge must not occur at the same time as EXLRCK edge.

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| **Control Interface Timing (CSP pin = "L")** | | | | | |
| CCLK Period | tCCK | 142 | - | - | ns |
| CCLK Pulse Width Low | tCCKL | 56 | - | - | ns |
| Pulse Width High | tCCKH | 56 | - | - | ns |
| CDTI Setup Time | tCDS | 28 | - | - | ns |
| CDTI Hold Time | tCDH | 28 | - | - | ns |
| CSN "H" Time | tCSW | 150 | - | - | ns |
| CSN Edge to CCLK "↑" (Note 22) | tCSS | 50 | - | - | ns |
| CCLK "↑" to CSN Edge (Note 22) | tCSH | 50 | - | - | ns |
| **Control Interface Timing (CSP pin = "H")** | | | | | |
| CCLK Period | tCCK | 142 | - | - | ns |
| CCLK Pulse Width Low | tCCKL | 56 | - | - | ns |
| Pulse Width High | tCCKH | 56 | - | - | ns |
| CDTI Setup Time | tCDS | 28 | - | - | ns |
| CDTI Hold Time | tCDH | 28 | - | - | ns |
| CSN "L" Time | tCSW | 150 | - | - | ns |
| CSN Edge to CCLK "↑" (Note 22) | tCSS | 50 | - | - | ns |
| CCLK "↑" to CSN Edge (Note 22) | tCSH | 50 | - | - | ns |
| **Power-down & Reset Timing** | | | | | |
| PDN Pulse Width (Note 23) | tPD | 150 | - | - | ns |
| PMADL or PMADR "↑" to SDTO valid (Note 24) | | | | | |
| HPF1-0 bits = "00" | tPDV | - | 3088 | - | 1/fs |
| HPF1-0 bits = "01" | tPDV | - | 1552 | - | 1/fs |
| HPF1-0 bits = "10" | tPDV | - | 784 | - | 1/fs |

Note 22. CCLK rising edge must not occur at the same time as CSN edge.
Note 23. The AK5701 can be reset by the PDN pin = "L".
Note 24. This is the count of LRCK "↑" from the PMADL or PMADR bit = "1".

## ■ Timing Diagram
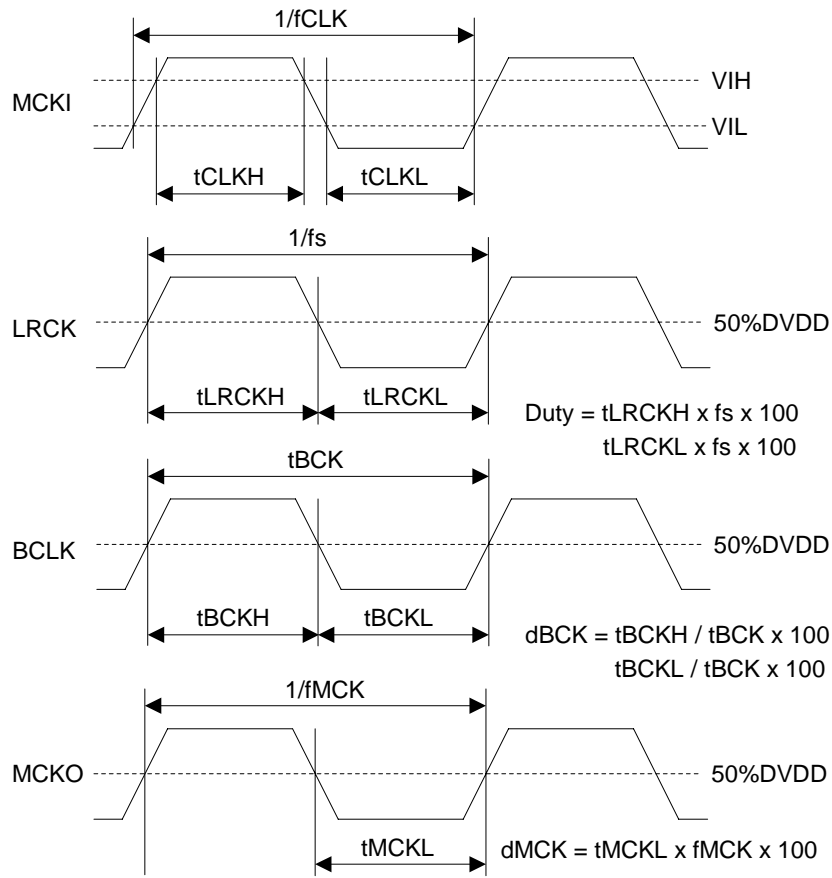


Figure 2. Clock Timing (PLL/EXT Master mode)

Duty = tLRCKH x fs x 100
       tLRCKL x fs x 100

dBCK = tBCKH / tBCK x 100
       tBCKL / tBCK x 100

dMCK = tMCKL x fMCK x 100
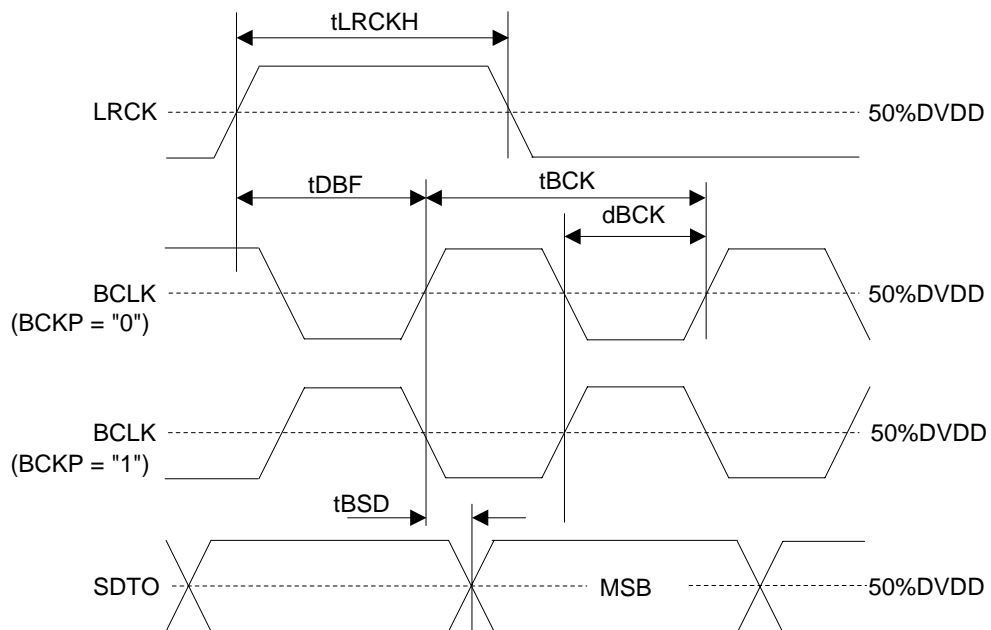


Figure 3. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = "0")
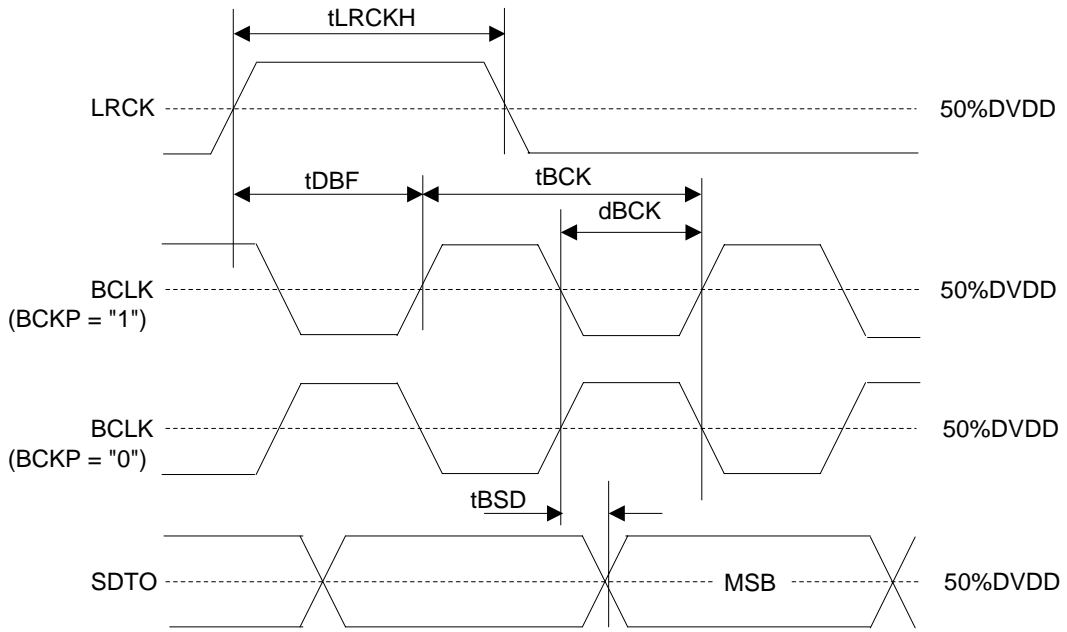
Figure 4. Audio Interface Timing (PLL/EXT Master mode & DSP mode: MSBS = "1")
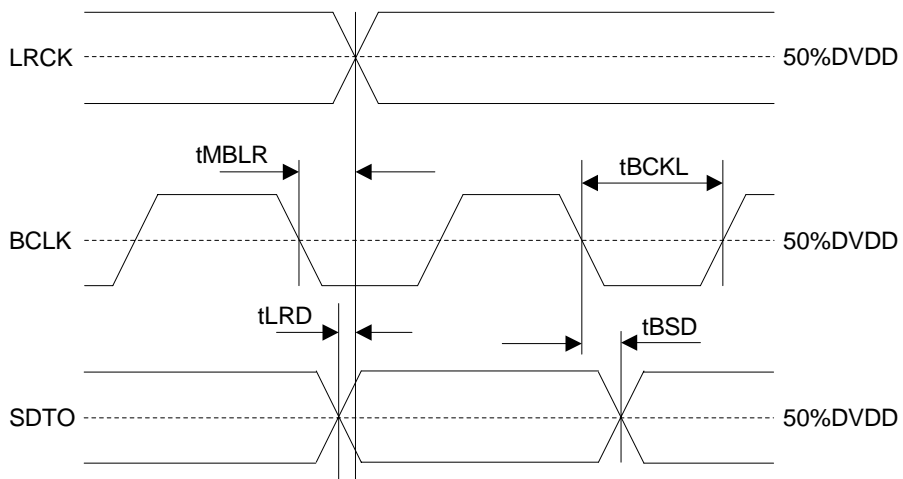


Figure 5. Audio Interface Timing (PLL/EXT Master mode & Except DSP mode)
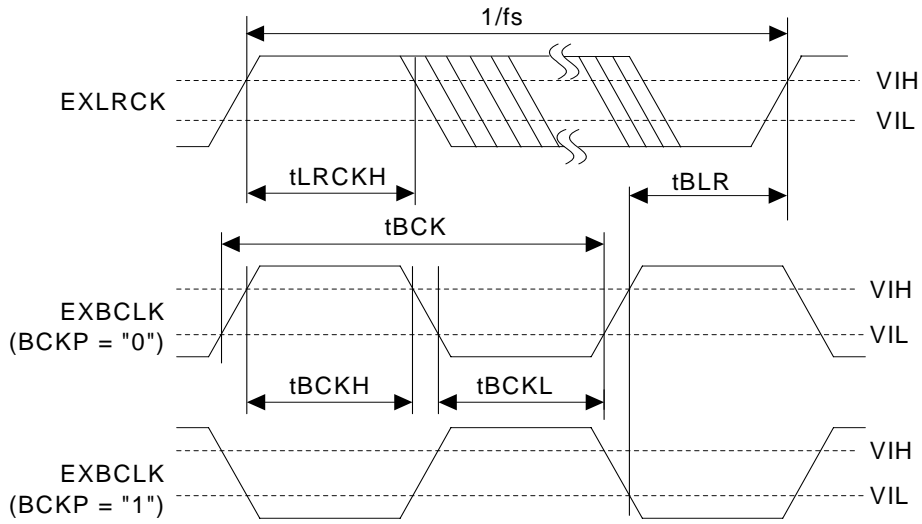
Figure 6. Clock Timing (PLL Slave mode; PLL Reference Clock = EXLRCK or EXBCLK pin & DSP mode; MSBS = 0)
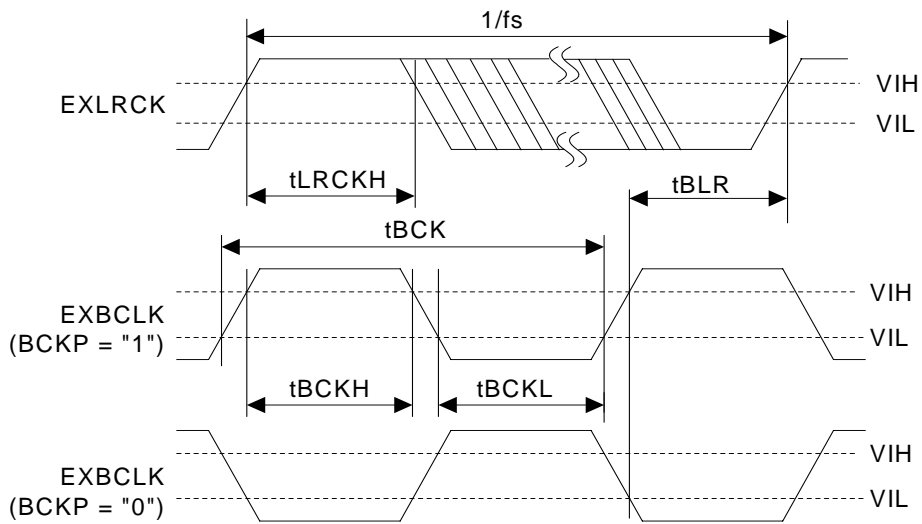


Figure 7. Clock Timing (PLL Slave mode; PLL Reference Clock = EXLRCK or EXBCLK pin & DSP mode; MSBS = 1)
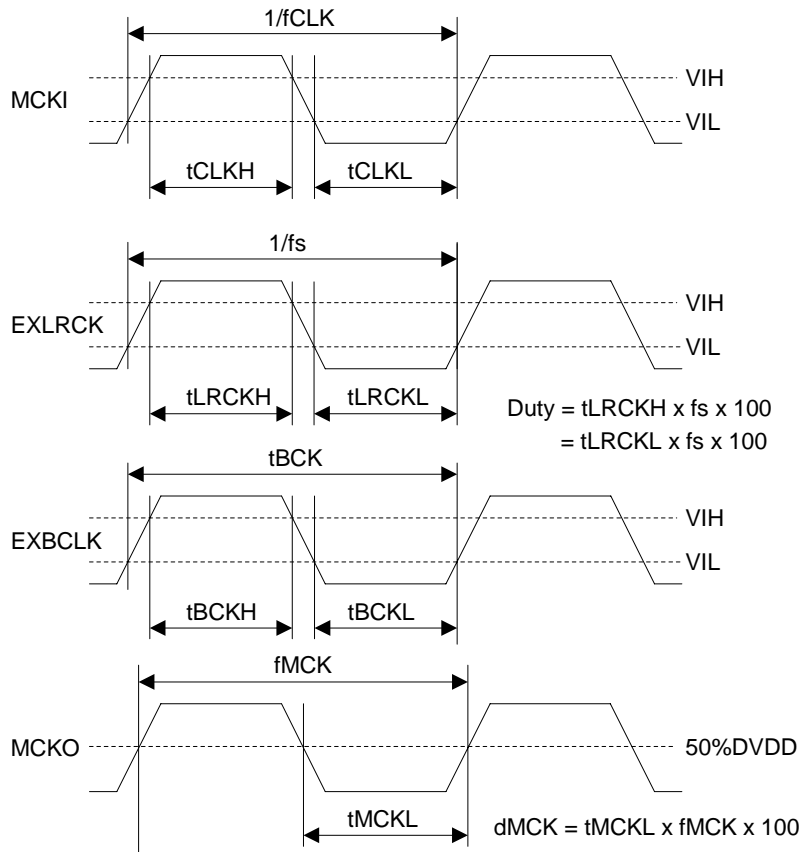
Figure 8. Clock Timing (PLL Slave mode; PLL Reference Clock = MCKI pin & Except DSP mode)

In Figure 8:

$$\text{Duty} = tLRCKH \times fs \times 100$$
$$= tLRCKL \times fs \times 100$$

$$dMCK = tMCKL \times fMCK \times 100$$
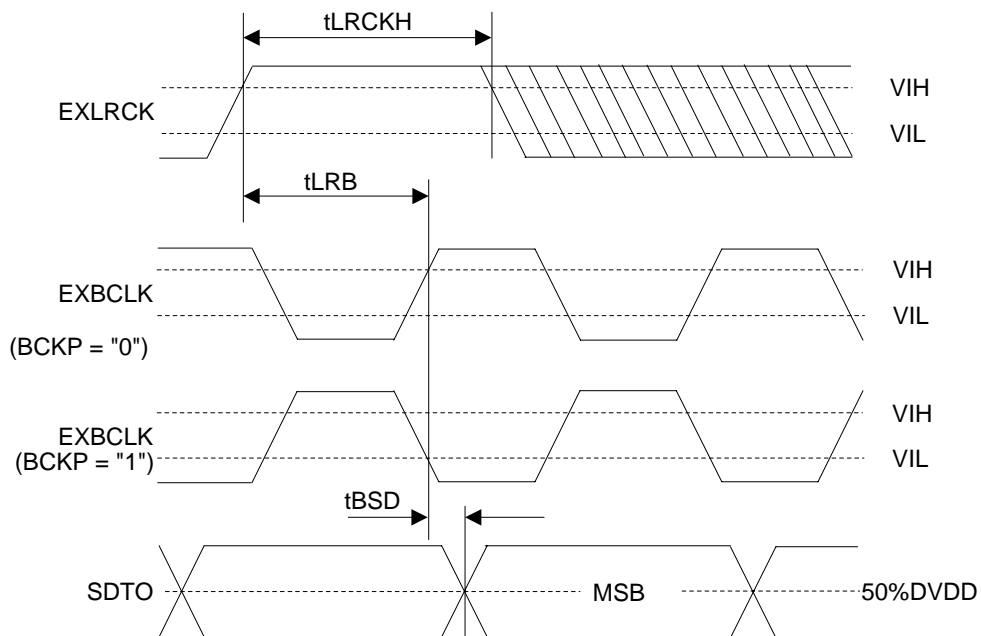


Figure 9. Audio Interface Timing (PLL Slave mode & DSP mode; MSBS = 0)
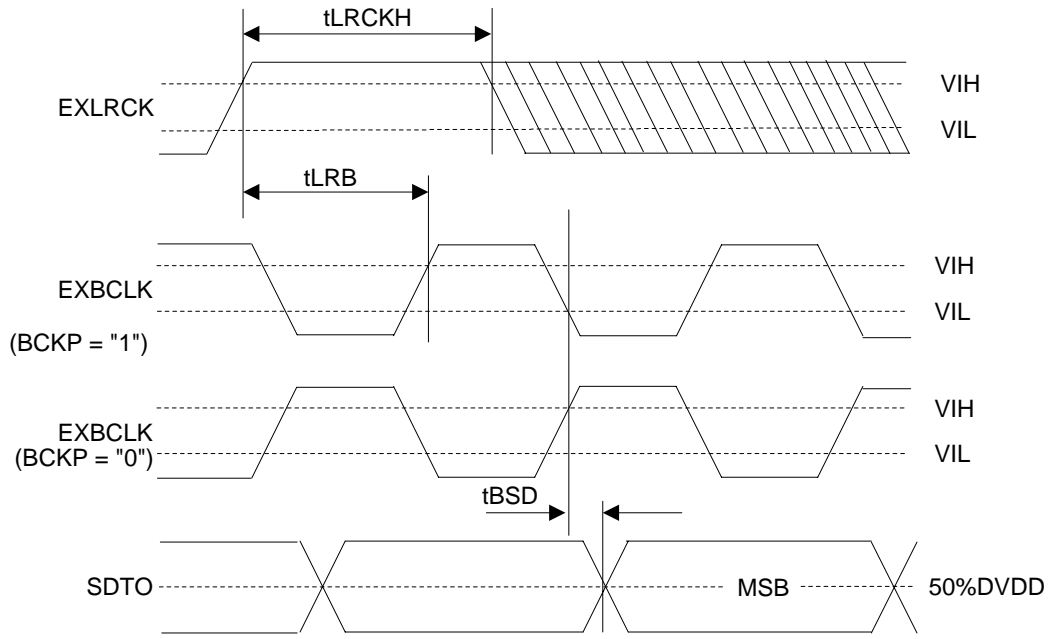
Figure 10. Audio Interface Timing (PLL Slave mode, DSP mode; MSBS = 1)
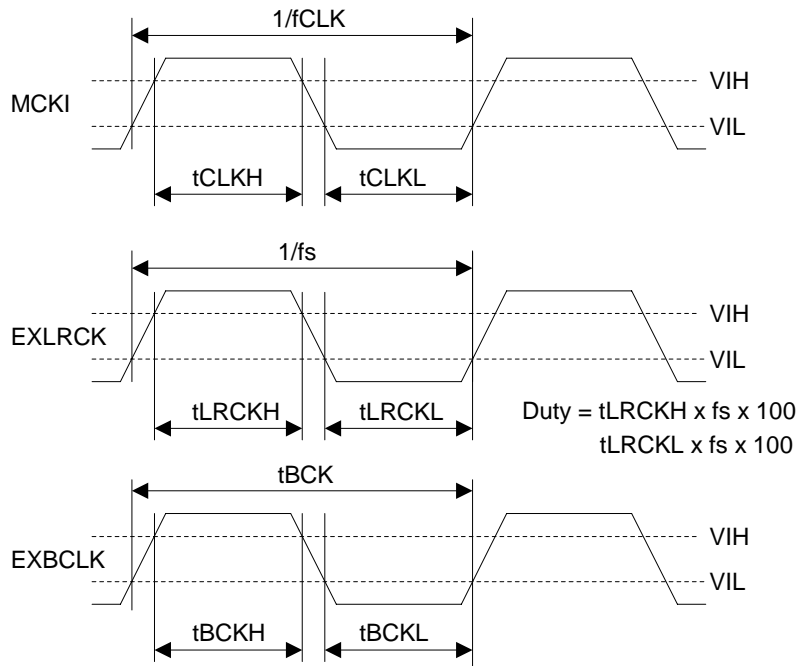


Figure 11. Clock Timing (EXT Slave mode)
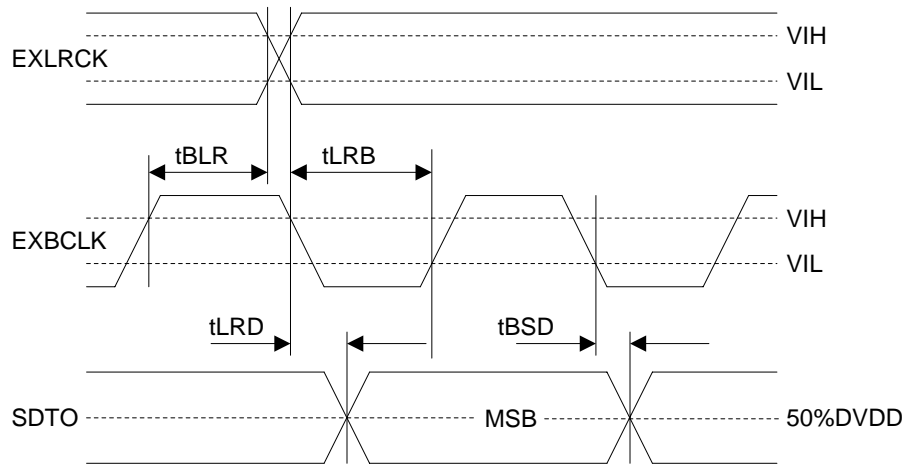
Figure 12. Audio Interface Timing (PLL/EXT Slave mode)
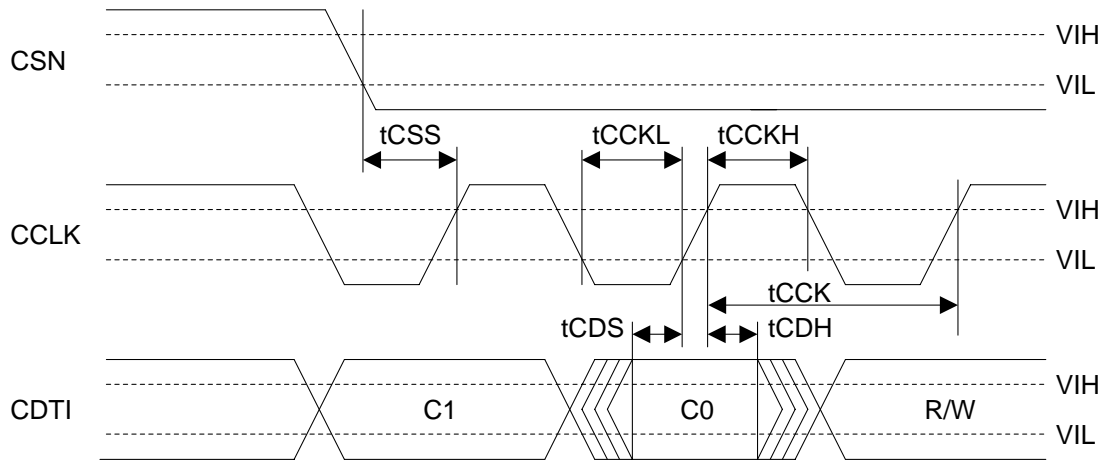
Figure 13. WRITE Command Input Timing (CSP pin = "L")
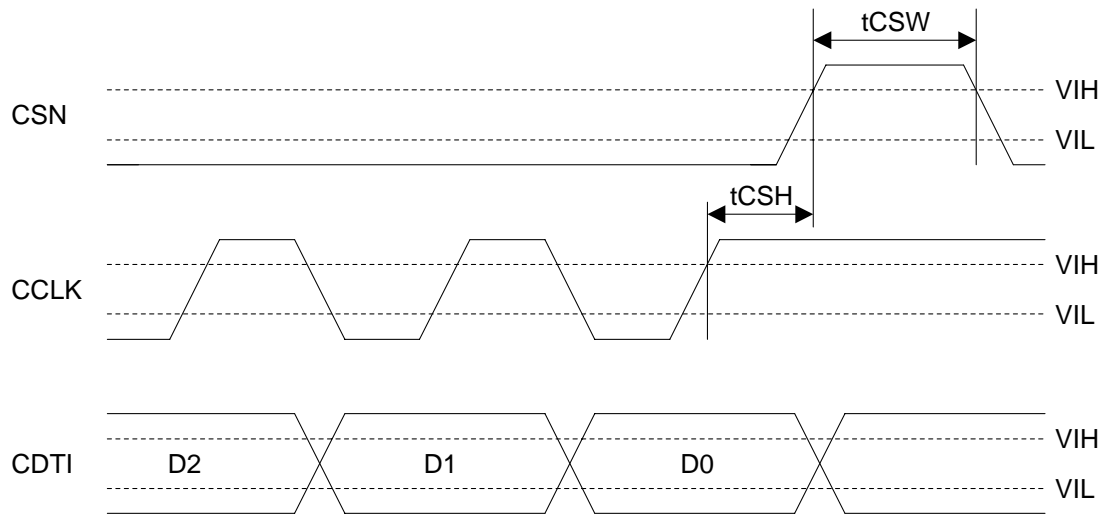


Figure 14. WRITE Data Input Timing (CSP pin = "L")
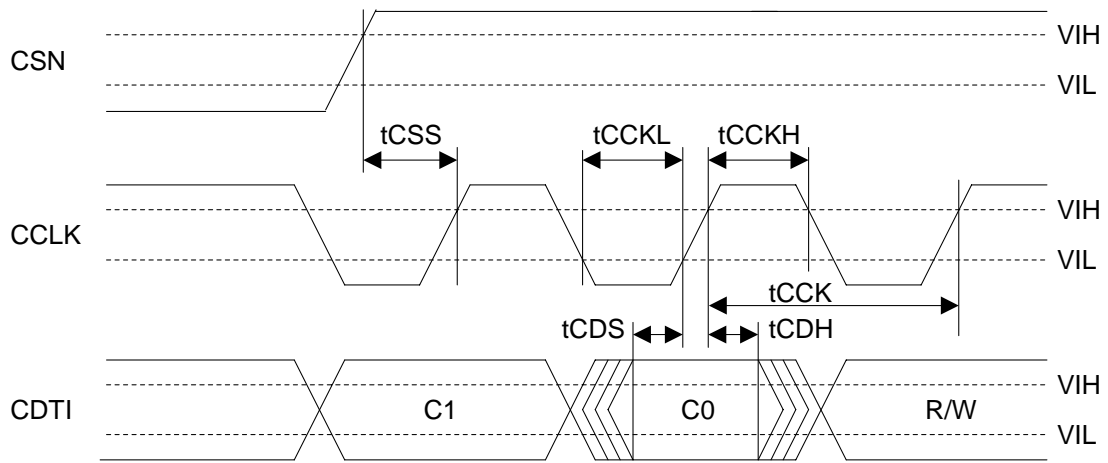
Figure 15. WRITE Command Input Timing (CSP pin = "H")
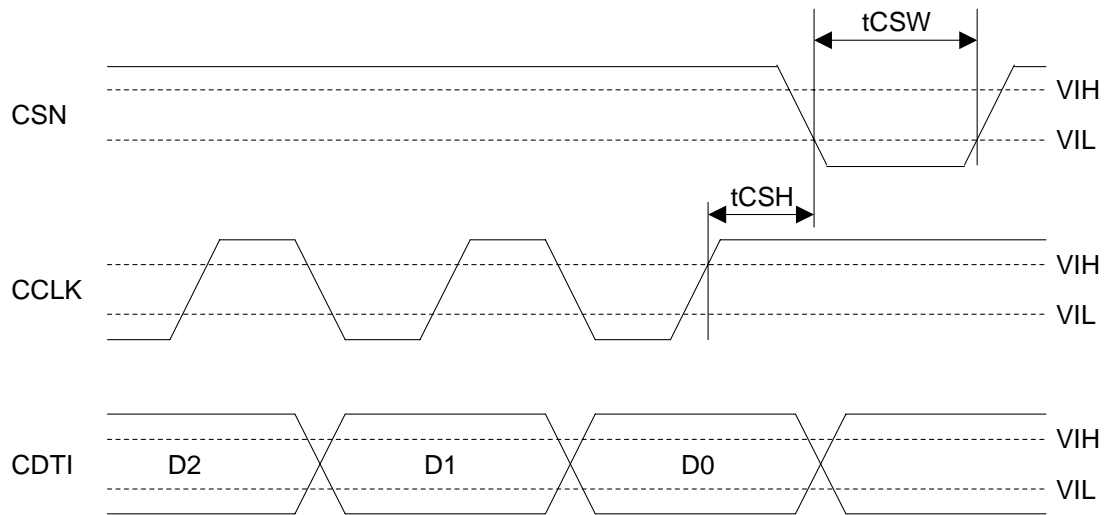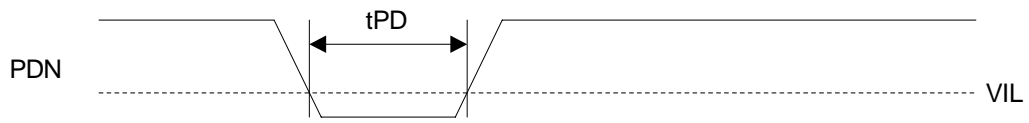


Figure 16. WRITE Data Input Timing (CSP pin = "H")

PMADL bit
or
PMADR bit

tPDV

SDTO                                                                              50%DVDD
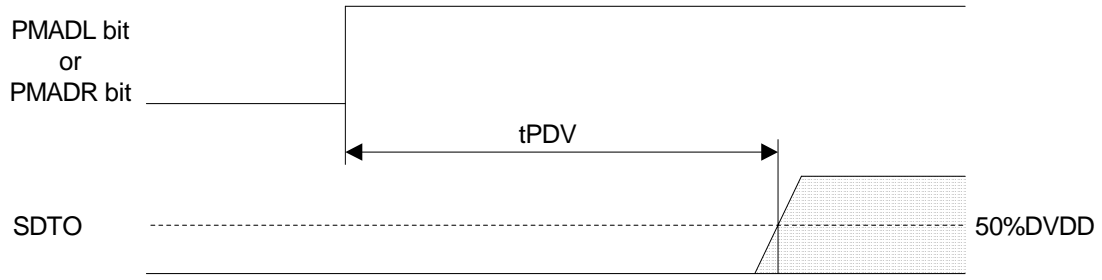
Figure 17. Power Down & Reset Timing 1

tPD

PDN

VIL

Figure 18. Power Down & Reset Timing 2

**AKM**

## OPERATION OVERVIEW

### ■ System Clock

There are the following five clock modes to interface with external devices (Table 1 and Table 2)

| Mode | PMPLL bit | M/S bit | PLL3-0 bits | Figure |
|---|---|---|---|---|
| PLL Master Mode (Note 25) | 1 | 1 | See Table 4 | Figure 19 |
| PLL Slave Mode 1 (PLL Reference Clock: MCKI pin) | 1 | 0 | See Table 4 | Figure 20 |
| PLL Slave Mode 2 (PLL Reference Clock: EXLRCK or EXBCLK pin) | 1 | 0 | See Table 4 | Figure 21 |
| EXT Slave Mode | 0 | 0 | x | Figure 22 |
| EXT Master Mode (Note 26) | 0 | 0 | x | Figure 23 |

Note 25. If M/S bit = "1", PMPLL bit = "0" and MCKO bit = "1" during the setting of PLL Master Mode, the invalid clocks are output from the MCKO pin when MCKO bit is "1".
Note 26. In case of EXT Master Mode, the register should be set as Figure 49.

Table 1. Clock Mode Setting (x: Don't care)

| Mode | MCKO bit | MCKO pin | MCKI pin | BCLK pin, EXBCLK pin | LRCK pin, EXLRCK pin |
|---|---|---|---|---|---|
| PLL Master Mode | 0 | L | Selected by PLL3-0 bits | BCLK pin (Selected by BCKO1-0 bits) | LRCK pin (1fs) (Note 27) |
| | 1 | Selected by PS1-0 bits | | | |
| PLL Slave Mode (PLL Reference Clock: MCKI pin) | 0 | L | Selected by PLL3-0 bits | EXBCLK pin (≥ 32fs) | EXLRCK pin (1fs) |
| | 1 | Selected by PS1-0 bits | | | |
| PLL Slave Mode (PLL Reference Clock: EXLRCK or EXBCLK pin) | 0 | L | GND | EXBCLK pin (Selected by PLL3-0 bits) | EXLRCK pin (1fs) |
| EXT Slave Mode | 0 | L | Selected by FS1-0 bits | EXBCLK pin (≥ 32fs) | EXLRCK pin (1fs) |
| EXT Master Mode | 0 | L | Selected by FS1-0 bits | BCLK pin (Selected by BCKO1-0 bits) | LRCK pin (1fs) |

Note 27. LRCK becomes 2fs at PLL Master Mode & DSP Mode 1.

Table 2. Clock pins state in Clock Mode

### ■ Master Mode/Slave Mode

The M/S bit selects either master or slave mode. M/S bit = "1" selects master mode and "0" selects slave mode. When the AK5701 is power-down mode (PDN pin = "L") and exits reset state, the AK5701 is slave mode. After exiting reset state, the AK5701 goes to master mode by changing M/S bit = "1".

| M/S bit | Mode | Used pins | |
|---|---|---|---|
| 0 | Slave Mode | EXBCLK, EXLRCK | (default) |
| 1 | Master Mode | BCLK, LRCK | |

Table 3. Select Master/Salve Mode

**AKM**

## ■ PLL Mode

When PMPLL bit is "1", a fully integrated analog phase locked loop (PLL) generates a clock that is selected by the PLL3-0 and FS3-0 bits. The PLL lock time is shown in Table 4, whenever the AK5701 is supplied to a stable clocks after PLL is powered-up (PMPLL bit = "0" → "1") or sampling frequency changes.

1) Setting of PLL Mode

| Mode | PLL3 bit | PLL2 Bit | PLL1 bit | PLL0 bit | PLL Reference Clock Input Pin | Input Frequency | R and C of VCOC pin | | PLL Lock Time (max) | |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | R[Ω] | C[F] | | |
| 0 | 0 | 0 | 0 | 0 | EXLRCK pin | 1fs | 6.8k | 220n | 80ms | |
| 2 | 0 | 0 | 1 | 0 | EXBCLK pin | 32fs | 10k | 4.7n | 2ms | |
| | | | | | | | 10k | 10n | 4ms | |
| 3 | 0 | 0 | 1 | 1 | EXBCLK pin | 64fs | 10k | 4.7n | 2ms | |
| | | | | | | | 10k | 10n | 4ms | |
| 4 | 0 | 1 | 0 | 0 | MCKI pin | 11.2896MHz | 10k | 4.7n | 40ms | |
| 5 | 0 | 1 | 0 | 1 | MCKI pin | 12.288MHz | 10k | 4.7n | 40ms | |
| 6 | 0 | 1 | 1 | 0 | MCKI pin | 12MHz | 10k | 4.7n | 40ms | |
| 7 | 0 | 1 | 1 | 1 | MCKI pin | 24MHz | 10k | 4.7n | 40ms | |
| 8 | 1 | 0 | 0 | 0 | MCKI pin | 19.2MHz | 10k | 4.7n | 40ms | |
| 9 | 1 | 0 | 0 | 1 | MCKI pin | 12MHz (Note 28) | 10k | 4.7n | 40ms | (default) |
| 12 | 1 | 1 | 0 | 0 | MCKI pin | 13.5MHz | 10k | 10n | 40ms | |
| 13 | 1 | 1 | 0 | 1 | MCKI pin | 27MHz | 10k | 10n | 40ms | |
| 14 | 1 | 1 | 1 | 0 | MCKI pin | 13MHz | 10k | 220n | 60ms | |
| 15 | 1 | 1 | 1 | 1 | MCKI pin | 26MHz | 10k | 220n | 60ms | |
| Others | Others | | | | | N/A | | | | |

Note 28. Please see Table 5 regarding the difference between PLL3-0 bits = "0110"(Mode 6) and "1001"(Mode 9).
Table 4. Setting of PLL Mode (*fs: Sampling Frequency)

2) Setting of sampling frequency in PLL Mode
When PLL reference clock input is MCKI pin, the sampling frequency is selected by FS3-0 bits as defined in Table 5.

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 8kHz | |
| 1 | 0 | 0 | 0 | 1 | 12kHz | |
| 2 | 0 | 0 | 1 | 0 | 16kHz | |
| 3 | 0 | 0 | 1 | 1 | 24kHz | |
| 4 | 0 | 1 | 0 | 0 | 7.35kHz<br>7.349918kHz (Note 29) | |
| 5 | 0 | 1 | 0 | 1 | 11.025kHz<br>11.024877kHz (Note 29) | |
| 6 | 0 | 1 | 1 | 0 | 14.7kHz<br>14.69984kHz (Note 29) | |
| 7 | 0 | 1 | 1 | 1 | 22.05kHz<br>22.04975kHz (Note 29) | |
| 10 | 1 | 0 | 1 | 0 | 32kHz | |
| 11 | 1 | 0 | 1 | 1 | 48kHz | |
| 14 | 1 | 1 | 1 | 0 | 29.4kHz<br>29.39967kHz (Note 29) | |
| 15 | 1 | 1 | 1 | 1 | 44.1kHz<br>44.0995kHz (Note 29) | (default) |
| Others | Others | | | | N/A | |

Note 29. In case of PLL3-0 bits = "1001"
Table 5. Setting of Sampling Frequency at PMPLL bit = "1" and Reference Clock=MCKI pin

When PLL reference clock input is EXLRCK or EXBCLK pin, the sampling frequency is selected by FS3 and FS2 bits (Table 6).

| Mode | FS3 bit | FS2 bit | FS1 bit | FS0 bit | Sampling Frequency Range | |
|------|---------|---------|---------|---------|--------------------------|---|
| 0 | 0 | 0 | x | x | 7.35kHz ≤ fs ≤ 12kHz | |
| 1 | 0 | 1 | x | x | 12kHz < fs ≤ 24kHz | |
| 2 | 1 | x | x | x | 24kHz < fs ≤ 48kHz | (default) |
| Others | Others | | | | N/A | |

(x: Don't acre, N/A: Not available)

Table 6. Setting of Sampling Frequency at PMPLL bit = "1" and Reference=EXLRCK/EXBCLK

## ■ PLL Unlock State

1) PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

In this mode, LRCK and BCLK pins go to "L" and irregular frequency clock is output from the MCKO pin at MCKO bit is "1" before the PLL goes to lock state after PMPLL bit = "0" → "1". If MCKO bit is "0", the MCKO pin changes to "L" (Table 7).

In DSP Mode 0 and 1, BCLK and LRCK start to output corresponding to Lch data after PLL goes to lock state by setting PMPLL bit = "0" → "1". When MSBS and BCKP bits are "01" or "10" in DSP Mode 0 and 1, BCLK "H" time of the first pulse becomes 1/(256fs) shorter than "H" time except for the first pulse.

When sampling frequency is changed, BCLK and LRCK pins do not output irregular frequency clocks but go to "L" by setting PMPLL bit to "0".

| PLL State | MCKO pin | | BCLK pin | LRCK pin |
|-----------|----------|---|----------|----------|
| | MCKO bit = "0" | MCKO bit = "1" | | |
| After that PMPLL bit "0" → "1" | "L" Output | Invalid | "L" Output | "L" Output |
| PLL Unlock (except above case) | "L" Output | Invalid | Invalid | Invalid |
| PLL Lock | "L" Output | See Table 9 | See Table 10 | 1fs Output (Note 30) |

Note 30. LRCK becomes 2fs at DSP Mode 1.

Table 7. Clock Operation at PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

2) PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

In this mode, an invalid clock is output from the MCKO pin before the PLL goes to lock state after PMPLL bit = "0" → "1". After that, the clock selected by Table 9 is output from the MCKO pin when PLL is locked. ADC and DAC output invalid data when the PLL is unlocked. For DAC, the output signal should be muted by writing "0" to DACL, DACH and DACS bits.

| PLL State | MCKO pin | |
|-----------|----------|---|
| | MCKO bit = "0" | MCKO bit = "1" |
| After that PMPLL bit "0" → "1" | "L" Output | Invalid |
| PLL Unlock (except above case) | "L" Output | Invalid |
| PLL Lock | "L" Output | See Table 9 |

Table 8. Clock Operation at PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

## ■ PLL Master Mode (PMPLL bit = "1", M/S bit = "1")

When an external clock (11.2896MHz, 12MHz, 12.288MHz, 13MHz, 13.5MHz, 19.2MHz, 24MHz, 26MHz or 27MHz) is input to MCKI pin, the MCKO, BCLK and LRCK clocks are generated by an internal PLL circuit. The MCKO output frequency is selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. The BCLK output frequency is selected among 32fs or 64fs, by BCKO1-0 bits (Table 10).
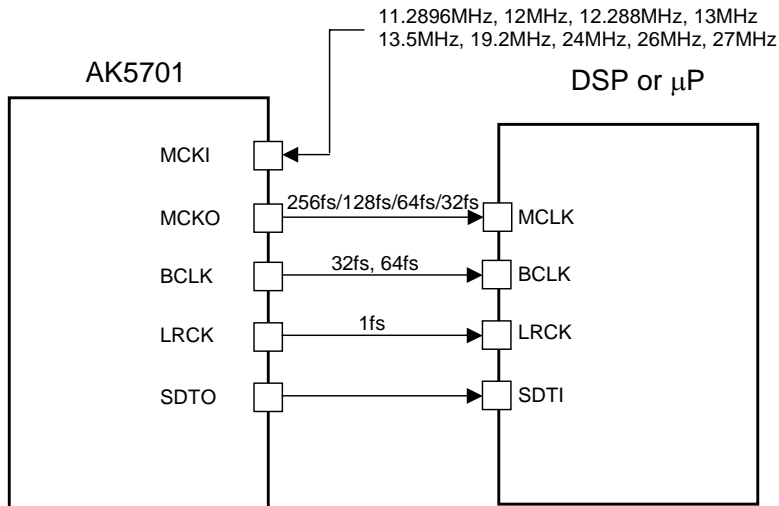


Figure 19. PLL Master Mode

| Mode | PS1 bit | PS0 bit | MCKO pin | |
|------|---------|---------|----------|-----------|
| 0 | 0 | 0 | 256fs | (default) |
| 1 | 0 | 1 | 128fs | |
| 2 | 1 | 0 | 64fs | |
| 3 | 1 | 1 | 32fs | |

Table 9. MCKO Output Frequency (PLL Mode, MCKO bit = "1")

| BCKO1 bit | BCKO0 bit | BCLK Output Frequency | |
|-----------|-----------|-----------------------|-----------|
| 0 | 0 | N/A | |
| 0 | 1 | 32fs | (default) |
| 1 | 0 | 64fs | |
| 1 | 1 | N/A | |

Table 10. BCLK Output Frequency at Master Mode (N/A: Not available)

**AKM**

## ■ PLL Slave Mode (PMPLL bit = "1", M/S bit = "0")

A reference clock of PLL is selected among the input clocks to the MCKI, EXBCLK or EXLRCK pin. The required clock to the AK5701 is generated by an internal PLL circuit. Input frequency is selected by PLL3-0 bits (Table 4).

### a) PLL reference clock: MCKI pin

EXBCLK and EXLRCK inputs should be synchronized with MCKO output. The phase between MCKO and EXLRCK is not important. The MCKO pin outputs the frequency selected by PS1-0 bits (Table 9) and the output is enabled by MCKO bit. Sampling frequency can be selected by FS3-0 bits (Table 5).



11.2896MHz, 12MHz, 12.288MHz, 13MHz
13.5MHz, 19.2MHz, 24MHz, 26MHz, 27MHz

AK5701 ... DSP or μP

| AK5701 | | DSP or μP |
|---|---|---|
| MCKI | | |
| MCKO | 256fs/128fs/64fs/32fs | MCLK |
| EXBCLK | ≥ 32fs | BCLK |
| EXLRCK | 1fs | LRCK |
| SDTO | | SDTI |
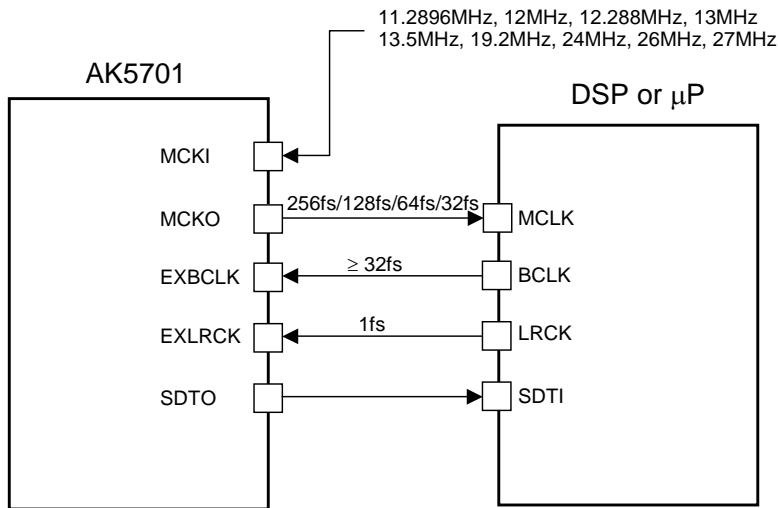
Figure 20. PLL Slave Mode 1 (PLL Reference Clock: MCKI pin)

The external clocks (MCKI, EXBCLK and EXLRCK) should always be present whenever the ADC is in operation (PMADL bit = "1" or PMADR bit = "1"). If these clocks are not provided, the AK5701 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC should be in the power-down mode (PMADL=PMADR bits = "0").

### b) PLL reference clock: EXBCLK or EXLRCK pin

Sampling frequency corresponds to 7.35kHz to 48kHz by changing FS3-0 bits (Table 6).



| AK5701 | | DSP or μP |
|---|---|---|
| MCKI | | |
| EXBCLK | 32fs, 64fs | BCLK |
| EXLRCK | 1fs | LRCK |
| SDTO | | SDTI |
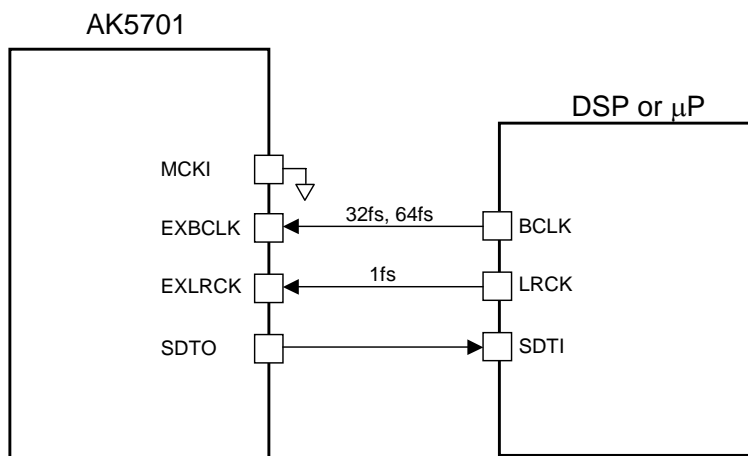
Figure 21. PLL Slave Mode 2 (PLL Reference Clock: EXLRCK or EXBCLK pin)

## ■ EXT Slave Mode (PMPLL bit = "0", M/S bit = "0")

When PMPLL bit is "0", the AK5701 becomes EXT mode. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. This mode is compatible with I/F of the normal audio CODEC. The clocks required to operate are MCKI (256fs, 512fs or 1024fs), EXLRCK (fs) and EXBCLK (≥32fs). The master clock (MCKI) should be synchronized with EXLRCK. The phase between these clocks is not important. The input frequency of MCKI is selected by FS1-0 bits (Table 11).

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range | |
|------|-----------|---------|---------|----------------------|--------------------------|---|
| 0 | x | 0 | 0 | 256fs | 7.35kHz ~ 48kHz | |
| 1 | x | 0 | 1 | 1024fs | 7.35kHz ~ 13kHz | |
| 2 | x | 1 | 0 | 512fs | 7.35kHz ~ 26kHz | |
| 3 | x | 1 | 1 | 256fs | 7.35kHz ~ 48kHz | (default) |

Table 11. MCKI Frequency at EXT Slave Mode (PMPLL bit = "0", M/S bit = "0") (x: Don't care)

The external clocks (MCKI, EXBCLK and EXLRCK) should always be present whenever the ADC is in operation (PMADL bit = "1" or PMADR bit = "1"). If these clocks are not provided, the AK5701 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If the external clocks are not present, the ADC should be in the power-down mode (PMADL=PMADR bits = "0").
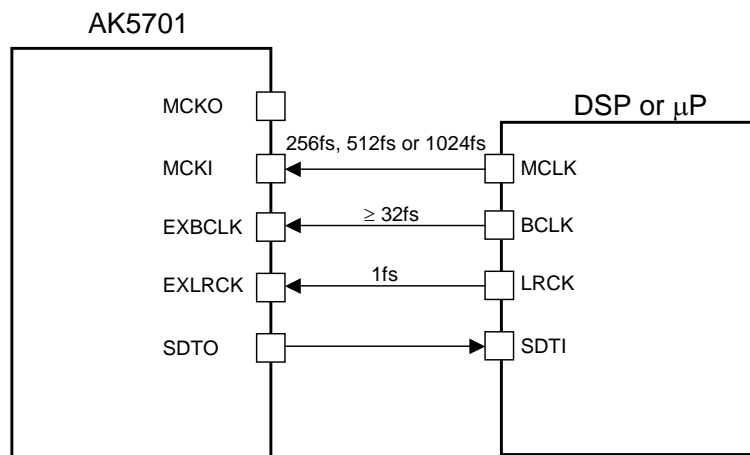


Figure 22. EXT Slave Mode

### ■ EXT Master Mode (PMPLL bit = "0", M/S bit = "1", TE3-0 bits = "0101", TMASTER bit = "1")

The AK5701 becomes EXT Master Mode by setting as Figure 49. Master clock is input from the MCKI pin, the internal PLL circuit is not operated. The clock required to operate is MCKI (256fs, 512fs or 1024fs). The input frequency of MCKI is selected by FS1-0 bits (Table 12).

| Mode | FS3-2 bits | FS1 bit | FS0 bit | MCKI Input Frequency | Sampling Frequency Range | |
|---|---|---|---|---|---|---|
| 0 | x | 0 | 0 | 256fs | 7.35kHz ~ 48kHz | |
| 1 | x | 0 | 1 | 1024fs | 7.35kHz ~ 13kHz | |
| 2 | x | 1 | 0 | 512fs | 7.35kHz ~ 26kHz | |
| 3 | x | 1 | 1 | 256fs | 7.35kHz ~ 48kHz | (default) |

Table 12. MCKI Frequency at EXT Master Mode (x: Don't care)

MCKI should always be present whenever the ADC is in operation (PMADL bit = "1" or PMADR bit = "1"). If MCKI is not provided, the AK5701 may draw excess current and it is not possible to operate properly because utilizes dynamic refreshed logic internally. If MCKI is not present, the ADC should be in the power-down mode (PMADL=PMADR bits = "0").
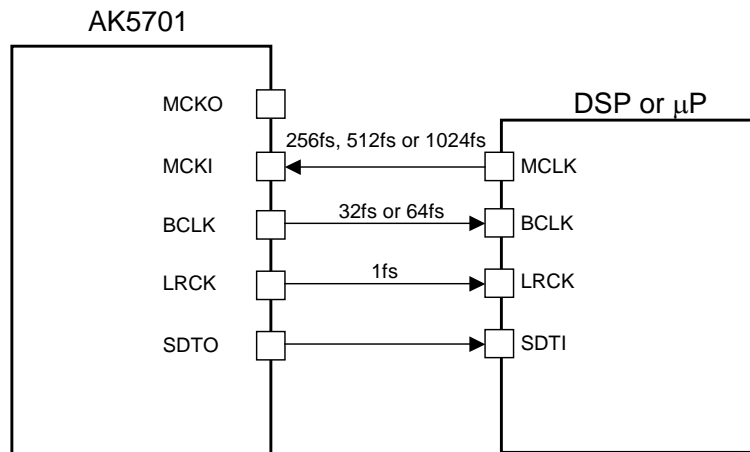


Figure 23. EXT Master Mode

| BCKO1 bit | BCKO0 bit | BCLK Output Frequency | |
|---|---|---|---|
| 0 | 0 | N/A | |
| 0 | 1 | 32fs | (default) |
| 1 | 0 | 64fs | |
| 1 | 1 | N/A | |

Table 13. BCLK Output Frequency at Master Mode (N/A: Not available)

## ■ Bypass Mode

When THR bit = "1", M/S bit = "0", PMADL bit = "0" and PMADR bit = "0", input clocks and data of EXLRCK, EXBCLK and EXSDTI pins are bypassed to LRCK, BCLK and SDTO pins, respectively.

When THR bit = "1", M/S bit = "0" and PMADL bit = "1" or PMADR bit = "1", input clocks of EXLRCK and EXBCLK pins are bypassed to LRCK and BCLK pins, and ADC data is output from the SDTO pin.

| THR bit | M/S bit | PMADL bit PMADR bit | BCLK/LRCK | SDTO | Mode | Figure | |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 00 | L | L | Power down | | (default) |
| | | 01/10/11 | L | ADC data | Slave mode | | |
| | 1 | 00 | Output | L | Power down | | |
| | | 01/10/11 | Output | ADC data | Master mode | | |
| 1 | 0 | 00 | EXBCLK/EXLRCK | EXSDTI | Bypass mode | Figure 24 | |
| | | 01/10/11 | EXBCLK/EXLRCK | ADC data | Slave & Bypass | Figure 25 | |
| | 1 | 00 | N/A | N/A | N/A | | |
| | | 01/10/11 | Output | ADC data | Master mode | | |

Table 14. Bypass Mode Select (N/A: Not available)
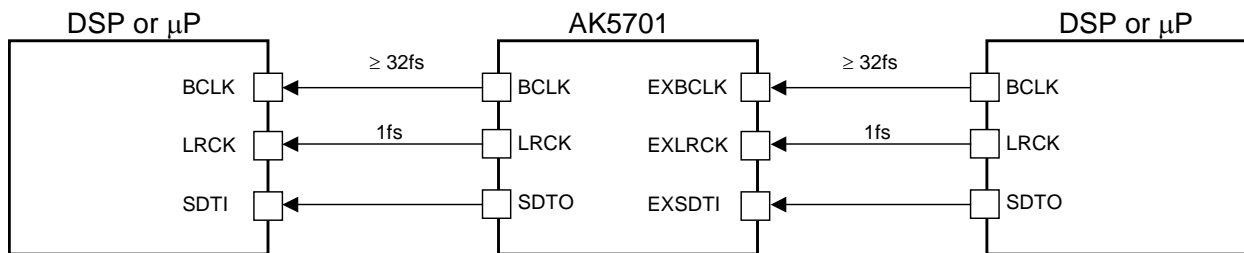


Figure 24. Bypass Mode
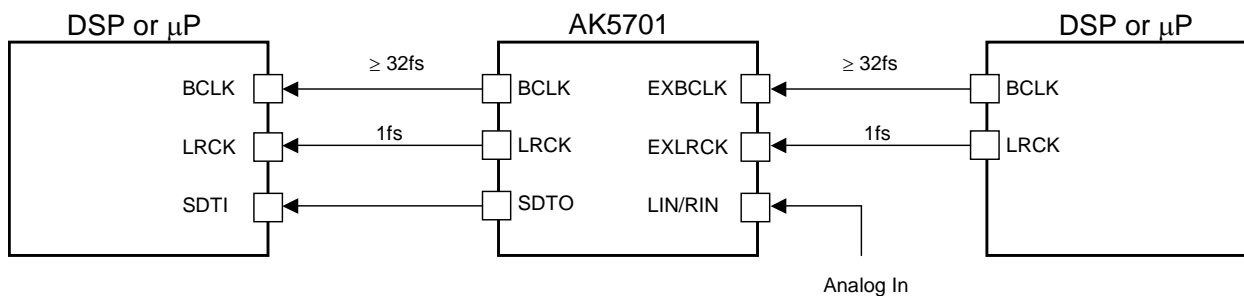


Figure 25. Slave & Bypass Mode

**■ Audio Interface Format**

Fore types of data format are available and are selected by setting the DIF1-0 bits (Table 15). In all modes, the serial data is MSB first, 2's complement format. Audio interface formats can be used in both master and slave modes, but DSP Mode 1 supports PLL Master Mode only. LRCK, BCLK and SDTO pins are used in master mode. EXLRCK, EXBCLK and SDTO pins are used in slave mode. In modes 2 and 3, the SDTO is clocked out on the falling edge ("↓") of BCLK/EXBCLK.

| Mode | DIF1 bit | DIF0 bit | SDTO | BCLK, EXBCLK | Figure | |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | DSP Mode 0 | 32fs | See Table 16 | |
| 1 | 0 | 1 | DSP Mode 1 | ≥ 32fs | | |
| 2 | 1 | 0 | MSB justified | ≥ 32fs | Figure 34 | |
| 3 | 1 | 1 | I²S compatible | ≥ 32fs | Figure 35 | (default) |

Table 15. Audio Interface Format

In Modes 0 and 1 (DSP mode 0 and 1), the audio I/F timing is changed by BCKP and MSBS bits.

When BCKP bit is "0", SDTO data is output by rising edge ("↑") of BCLK/EXBCLK.
When BCKP bit is "1", SDTO data is output by falling edge ("↓") of BCLK/EXBCLK.

MSB data position of SDTO can be shifted by MSBS bit. The shifted period is a half of BCLK/EXBCLK.

| DIF1 | DIF0 | MSBS | BCKP | Audio Interface Format | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | MSB of SDTO is output by the rising edge ("↑") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 26). | |
| | | 0 | 1 | MSB of SDTO is output by the falling edge ("↓") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 27). | |
| | | 1 | 0 | MSB of SDTO is output by next rising edge ("↑") of the falling edge ("↓") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 28). | |
| | | 1 | 1 | MSB of SDTO is output by next falling edge ("↓") of the rising edge ("↑") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 29). | |
| 0 | 1 | 0 | 0 | MSB of SDTO is output by the rising edge ("↑") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 30). | |
| | | 0 | 1 | MSB of SDTO is output by the falling edge ("↓") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 31). | |
| | | 1 | 0 | MSB of SDTO is output by next rising edge ("↑") of the falling edge ("↓") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 32). | |
| | | 1 | 1 | MSB of SDTO is output by next falling edge ("↓") of the rising edge ("↑") of the first BCLK/EXBCLK after the rising edge ("↑") of LRCK/EXLRCK (Figure 33). | (default) |

Table 16. Audio Interface Format in Mode 0, 1

If 16-bit data that ADC outputs is converted to 8-bit data by removing LSB 8-bit, "−1" at 16bit data is converted to "−1" at 8-bit data. And when the DAC playbacks this 8-bit data, "−1" at 8-bit data will be converted to "−256" at 16-bit data and this is a large offset. This offset can be removed by adding the offset of "128" to 16-bit data before converting to 8-bit data.
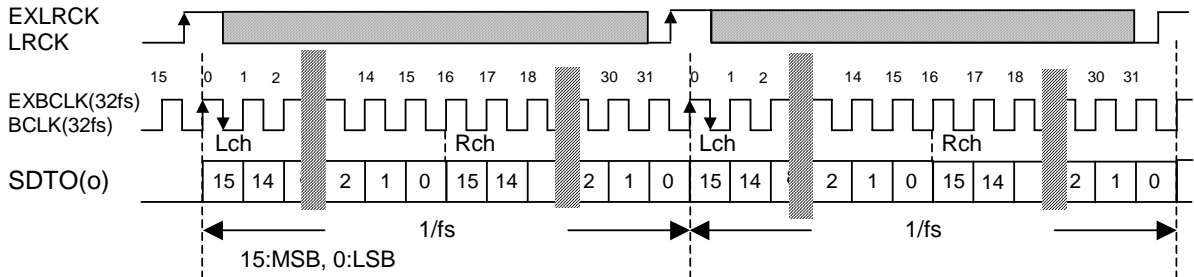
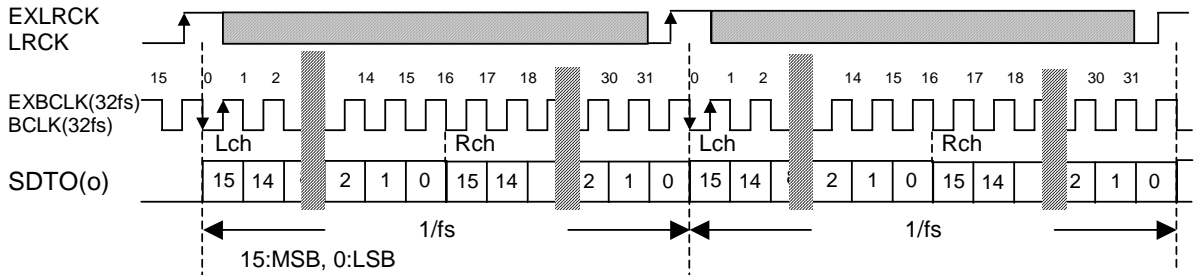Figure 26. Mode 0 Timing (BCKP = "0", MSBS = "0", M/S = "0" or "1")



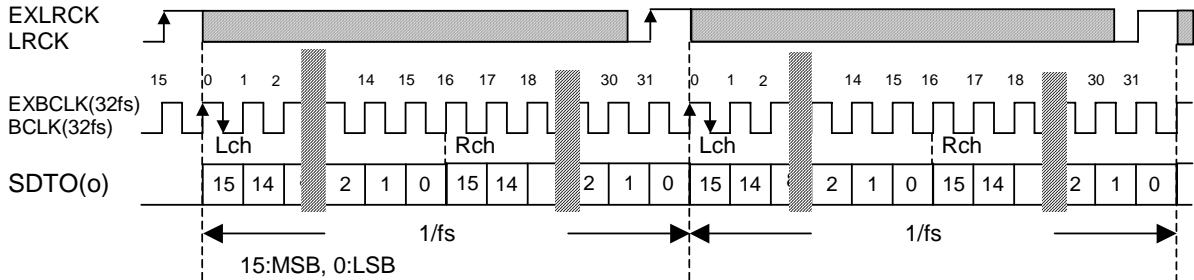Figure 27. Mode 0 Timing (BCKP = "1", MSBS = "0", M/S = "0" or "1")



Figure 28. Mode 0 Timing (BCKP = "0", MSBS = "1", M/S = "0" or "1")
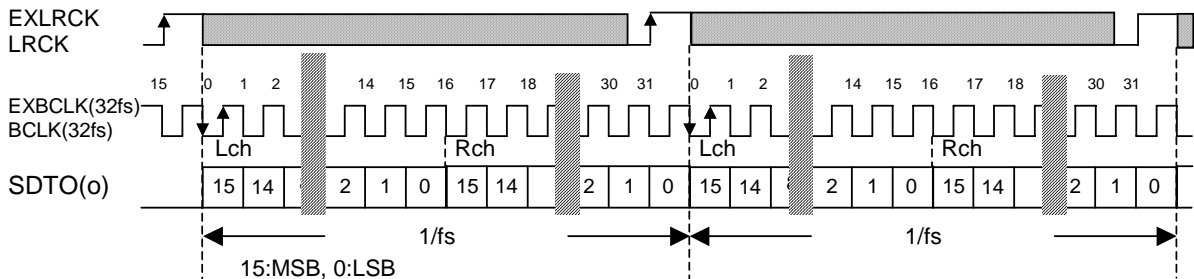


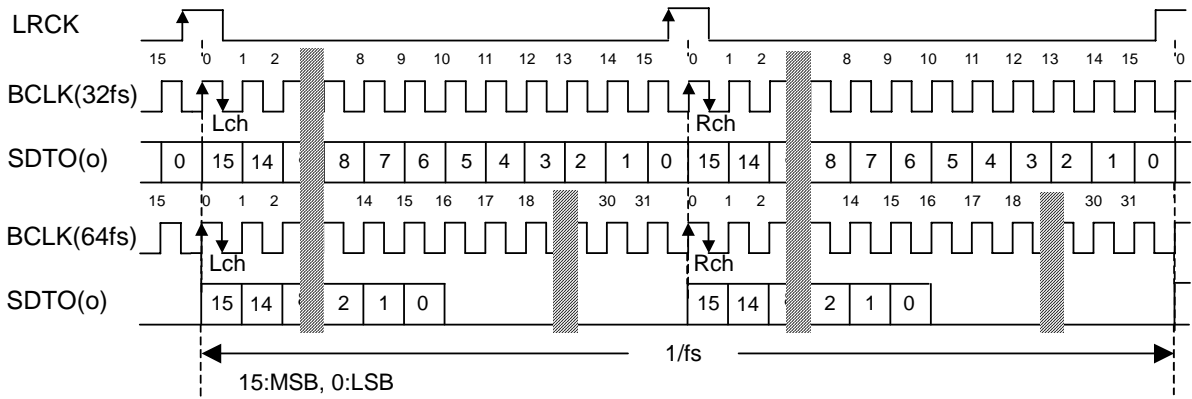Figure 29. Mode 0 Timing (BCKP = "1", MSBS = "1", M/S = "0" or "1")

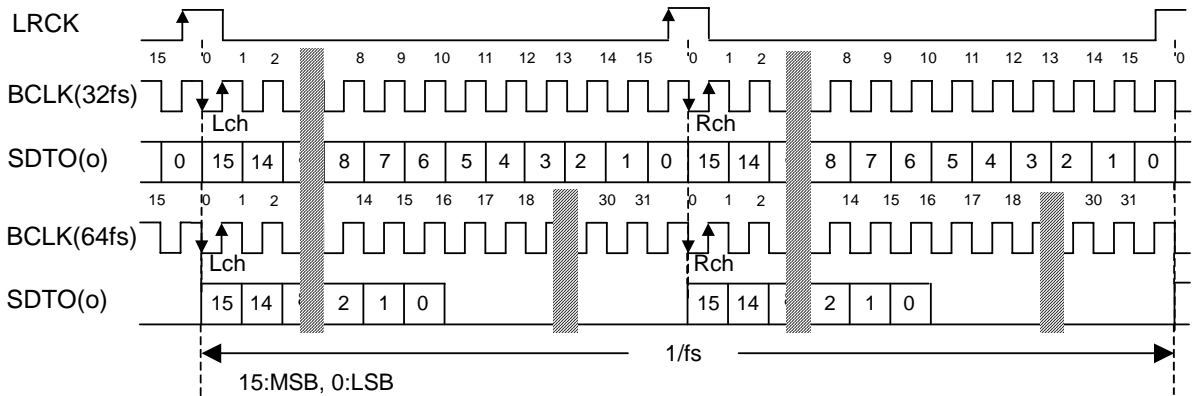Figure 30. Mode 1 Timing (BCKP = "0", MSBS = "0", M/S = "1")

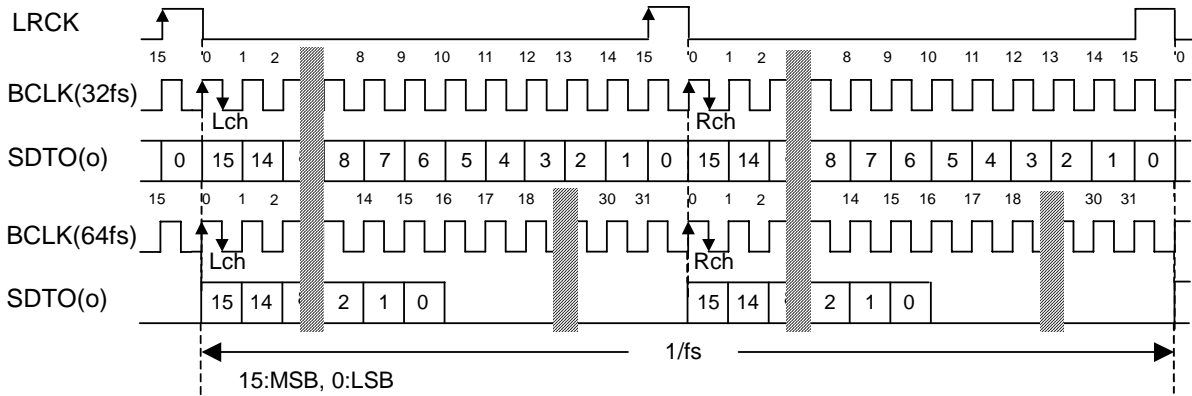Figure 31. Mode 1 Timing (BCKP = "1", MSBS = "0", M/S = "1")

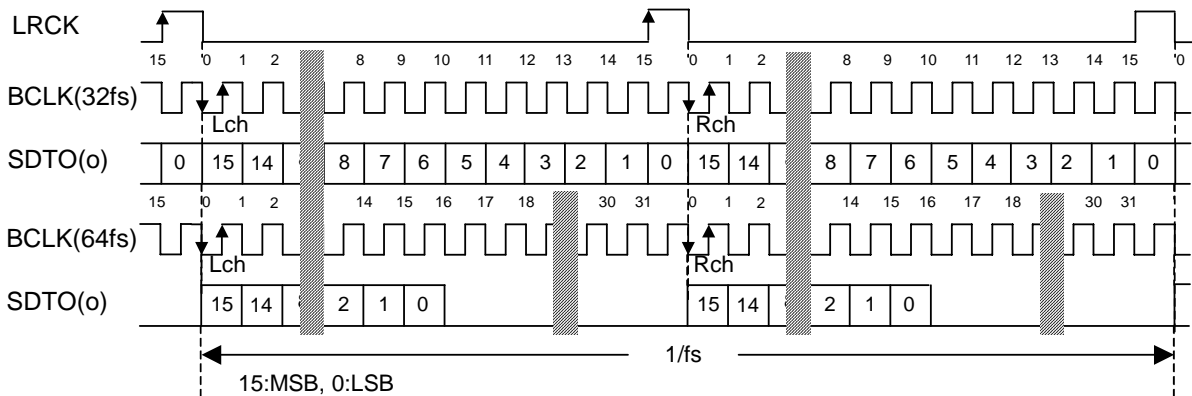Figure 32. Mode 1 Timing (BCKP = "0", MSBS = "1", M/S = "1")

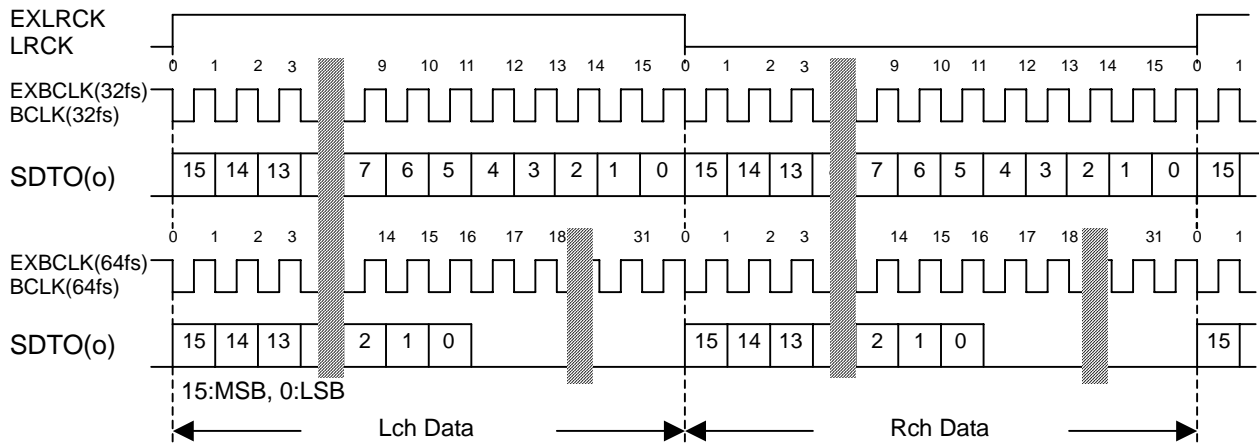Figure 33. Mode 1 Timing (BCKP = "1", MSBS = "1", M/S = "1")

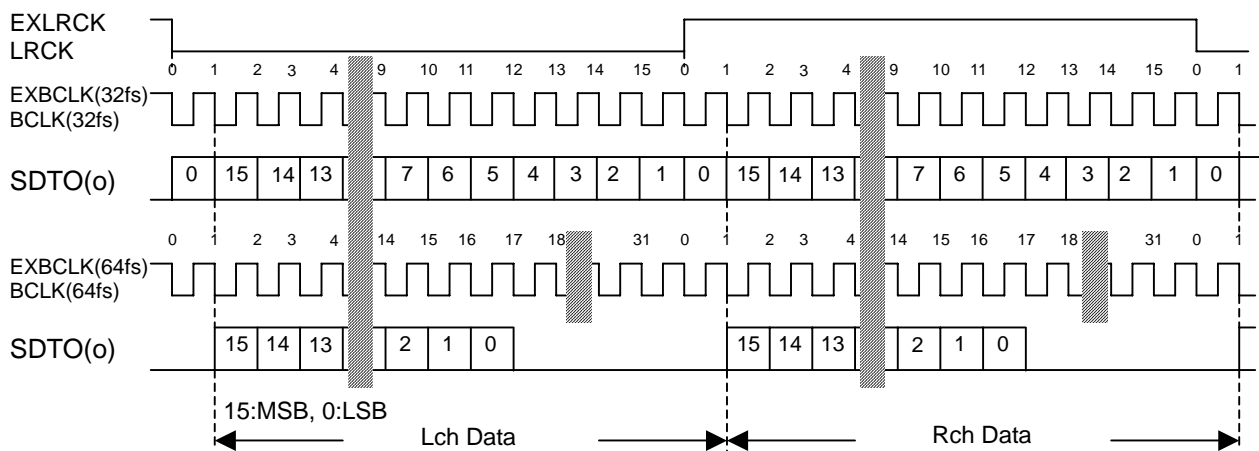Figure 34. Mode 2 Timing (MSB justified, M/S = "0" or "1")



Figure 35. Mode 3 Timing (I²S, M/S = "0" or "1")

■ **Mono/Stereo Selection**

PMADL, PMADR and MIX bits select mono or stereo mode of ADC output data. ALC operation (ALC bit = "1") or digital volume operation (ALC bit = "0") is applied to the data in Table 17.

| PMADL bit | PMADR bit | MIX bit | ADC Lch data | ADC Rch data | |
|-----------|-----------|---------|--------------|--------------|---|
| 0 | 0 | x | All "0" | All "0" | (default) |
| 0 | 1 | x | Rch Input Signal | Rch Input Signal | |
| 1 | 0 | x | Lch Input Signal | Lch Input Signal | |
| 1 | 1 | 0 | Lch Input Signal | Rch Input Signal | |
| | | 1 | (L+R)/2 | (L+R)/2 | |

Table 17. Mono/Stereo Selection (x: Don't care)

## ■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is selected by HPF1-0 bits (Table 18) and scales with sampling rate (fs). The default value is 3.4Hz (@fs=44.1kHz).

| HPF1 bit | HPF0 bit | fc | | | |
|----------|----------|------------|-------------|---------------|------------|
| | | fs=44.1kHz | fs=22.05kHz | fs=11.025kHz | |
| 0 | 0 | 3.4Hz | 1.7Hz | 0.85Hz | (default) |
| 0 | 1 | 6.8Hz | 3.4Hz | 1.7Hz | |
| 1 | 0 | 13.6Hz | 6.8Hz | 3.4Hz | |
| 1 | 1 | N/A | N/A | N/A | |

Table 18. Digital HPF Cut-off Frequency (N/A: Not available)

## ■ MIC/LINE Input Selector

The AK5701 has input selector. When MDIF1 and MDIF2 bits are "0", INL and INR bits select LIN1/LIN2 and RIN1/RIN2, respectively. When MDIF1 and MDIF2 bits are "1", LIN1, RIN1, LIN2 and RIN2 pins become LIN+, LIN−, RIN− and RIN+ pins respectively. In this case, full-differential input is available (Figure 37).

| MDIF1 bit | MDIF2 bit | INL bit | INR bit | Lch | Rch | |
|-----------|-----------|---------|---------|--------|--------|-----------|
| 0 | 0 | 0 | 0 | LIN1 | RIN1 | (default) |
| | | | 1 | LIN1 | RIN2 | |
| | | 1 | 0 | LIN2 | RIN1 | |
| | | | 1 | LIN2 | RIN2 | |
| | 1 | 0 | x | LIN1 | RIN+/− | |
| | | 1 | x | N/A | N/A | |
| 1 | 0 | x | 0 | N/A | N/A | |
| | | | 1 | LIN+/− | RIN2 | |
| | 1 | x | x | LIN+/− | RIN+/− | |

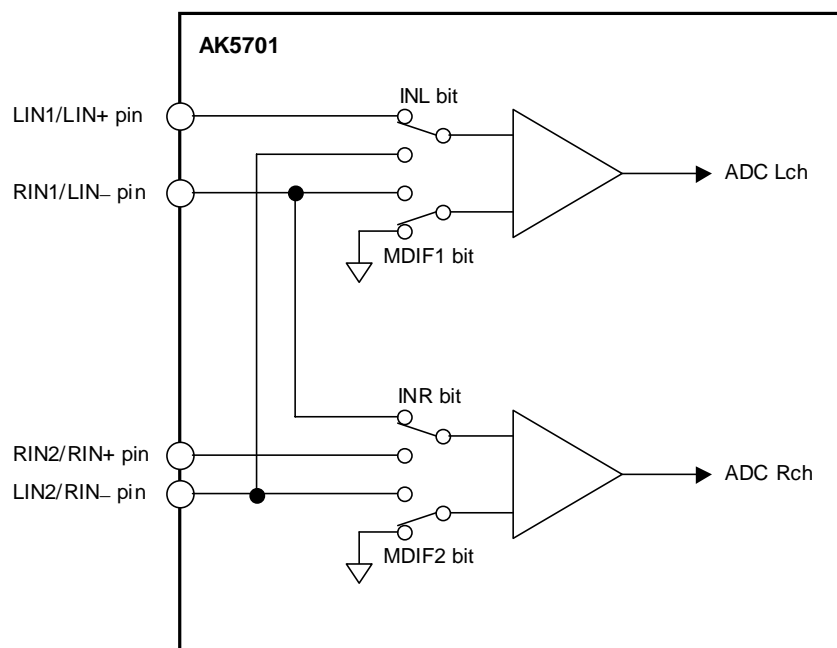Table 19. MIC/Line In Path Select (N/A: Not available)
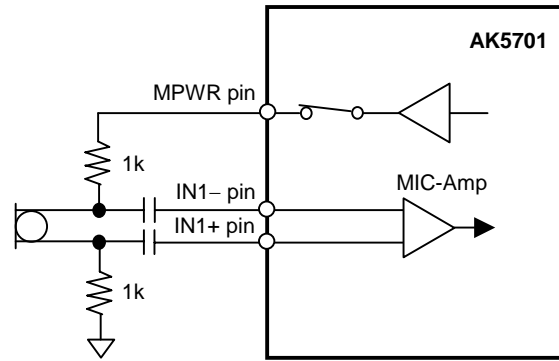


Figure 36. Mic/Line Input Selector

Figure 37. Connection Example for Full-differential Mic Input (MDIF1/2 bits = "1")

## ■ MIC Gain Amplifier

The AK5701 has a gain amplifier for microphone input. The gain of MIC-Amp is selected by the MGAIN1-0 bits (Table 20). The typical input impedance is 60kΩ(typ)@MGAIN1-0 bits = "00" or 30kΩ(typ)@MGAIN1-0 bits = "01" or "10".

| MGAIN1 bit | MGAIN0 bit | Input Gain | |
|------------|------------|------------|-----------|
| 0 | 0 | 0dB | |
| 0 | 1 | +15dB | (default) |
| 1 | 0 | +30dB | |
| 1 | 1 | N/A | |

Table 20. Mic Input Gain (N/A: Not available)

## ■ MIC Power

When PMMP bit = "1", the MPWR pin supplies power for the microphone. This output voltage is typically 0.75 x AVDD and the load resistance is minimum 0.5kΩ. In case of using two sets of stereo mic, the load resistance is minimum 2kΩ for each channel. Any capacitor must not be connected directly to the MPWR pin (Figure 38).

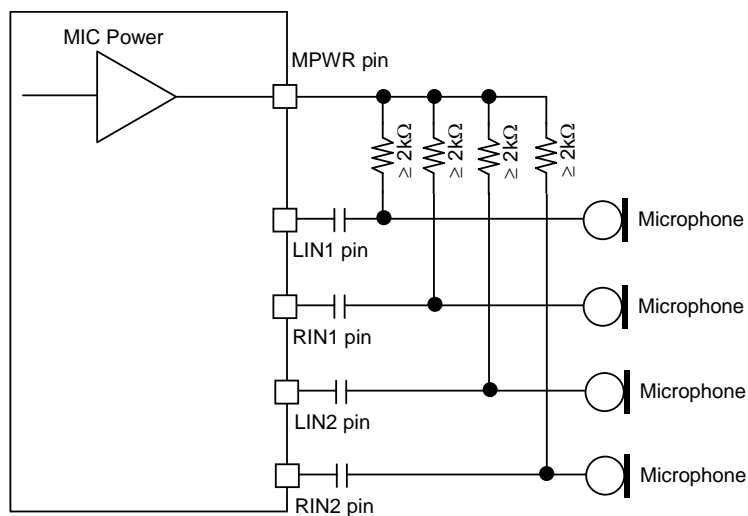| PMMP bit | MPWR pin | |
|----------|----------|-----------|
| 0 | Hi-Z | (default) |
| 1 | Output | |

Table 21. MIC Power



Figure 38. MIC Block Circuit

**■ ALC Operation**

The ALC (Automatic Level Control) is done by ALC block when ALC bit is "1".

1.  ALC Limiter Operation

During the ALC limiter operation, when either Lch or Rch exceeds the ALC limiter detection level (Table 22), the IVL and IVR values (same value) are attenuated automatically by the amount defined by the ALC limiter ATT step (Table 23).

When ZELMN bit = "0" (zero cross detection is enabled), the IVL and IVR values are changed by ALC limiter operation at the individual zero crossing points of Lch and Rch or at the zero crossing timeout. ZTM1-0 bits set the zero crossing timeout period of both ALC limiter and recovery operation (Table 24).

When ZELMN bit = "1" (zero cross detection is disabled), IVL and IVR values are immediately (period: 1/fs) changed by ALC limiter operation. Attenuation step is fixed to 1 step regardless of the setting of LMAT1-0 bits.

The attenuation operation is executed continuously until the input signal level becomes ALC limiter detection level (Table 22) or less. After completing the attenuation operation, unless ALC bit is changed to "0", the operation repeats when the input signal level exceeds LMTH1-0 bits.

| LMTH1 | LMTH0 | ALC Limier Detection Level | ALC Recovery Waiting Counter Reset Level | |
|---|---|---|---|---|
| 0 | 0 | ALC Output ≥ −2.5dBFS | −2.5dBFS > ALC Output ≥ −4.1dBFS | (default) |
| 0 | 1 | ALC Output ≥ −4.1dBFS | −4.1dBFS > ALC Output ≥ −6.0dBFS | |
| 1 | 0 | ALC Output ≥ −6.0dBFS | −6.0dBFS > ALC Output ≥ −8.5dBFS | |
| 1 | 1 | ALC Output ≥ −8.5dBFS | −8.5dBFS > ALC Output ≥ −12dBFS | |

Table 22. ALC Limiter Detection Level / Recovery Counter Reset Level

| ZELMN | LMAT1 | LMAT0 | ALC Limiter ATT Step | | |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 step | 0.375dB | (default) |
| | 0 | 1 | 2 step | 0.750dB | |
| | 1 | 0 | 4 step | 1.500dB | |
| | 1 | 1 | 8 step | 3.000dB | |
| 1 | x | x | 1step | 0.375dB | |

Table 23. ALC Limiter ATT Step

| ZTM1 | ZTM0 | | Zero Crossing Timeout Period | | | |
|---|---|---|---|---|---|---|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | (default) |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |

Table 24. ALC Zero Crossing Timeout Period

2. ALC Recovery Operation

The ALC recovery operation waits for the WTM1-0 bits (Table 25) to be set after completing the ALC limiter operation. If the input signal does not exceed "ALC recovery waiting counter reset level" (Table 22) during the wait time, the ALC recovery operation is executed. The IVL and IVR values are automatically incremented by RGAIN1-0 bits (Table 26) up to the set reference level (Table 27) with zero crossing detection which is timeout period set by ZTM1-0 bits (Table 24). Then the IVL and IVR are set to the same value for both channels. The ALC recovery operation is executed at a period set by WTM1-0 bits. If ZTM1-0 is longer than WTM1-0 and no zero crossing occurs, the ALC recovery operation is executed at a period set by ZTM1-0 bits.

For example, when the current IVOL value is 30H and RGAIN1-0 bits are set to "01", IVOL is changed to 32H by the auto limiter operation and then the input signal level is gained by 0.75dB (=0.375dB x 2). When the IVOL value exceeds the reference level (REF7-0), the IVOL values are not increased.

When
  "ALC recovery waiting counter reset level (LMTH1-0) ≤ Output Signal < ALC limiter detection level (LMTH1-0)" during the ALC recovery operation, the waiting timer of ALC recovery operation is reset. When
  "ALC recovery waiting counter reset level (LMTH1-0) > Output Signal",
the waiting timer of ALC recovery operation starts.

The ALC operation corresponds to the impulse noise. When the impulse noise is input, the ALC recovery operation becomes faster than a normal recovery operation. When large noise is input to microphone instantaneously, the quality of small level in the large noise can be improved by this fast recovery operation.

| WTM1 | WTM0 | | ALC Recovery Operation Waiting Period | | | |
|---|---|---|---|---|---|---|
| | | | 8kHz | 16kHz | 44.1kHz | |
| 0 | 0 | 128/fs | 16ms | 8ms | 2.9ms | (default) |
| 0 | 1 | 256/fs | 32ms | 16ms | 5.8ms | |
| 1 | 0 | 512/fs | 64ms | 32ms | 11.6ms | |
| 1 | 1 | 1024/fs | 128ms | 64ms | 23.2ms | |

Table 25. ALC Recovery Operation Waiting Period

| RGAIN1 | RGAIN0 | GAIN STEP | | |
|---|---|---|---|---|
| 0 | 0 | 1 step | 0.375dB | (default) |
| 0 | 1 | 2 step | 0.750dB | |
| 1 | 0 | 3 step | 1.125dB | |
| 1 | 1 | 4 step | 1.500dB | |

Table 26. ALC Recovery GAIN Step

| REF7-0 | GAIN(dB) | Step | |
|---|---|---|---|
| F1H | +36.0 | | |
| F0H | +35.625 | | |
| EFH | +35.25 | | |
| : | : | | |
| E2H | +30.375 | | |
| E1H | +30.0 | 0.375dB | (default) |
| E0H | +29.625 | | |
| : | : | | |
| 03H | −53.25 | | |
| 02H | −53.625 | | |
| 01H | −54.0 | | |
| 00H | MUTE | | |

Table 27. Reference Level at ALC Recovery operation

3. Example of ALC Operation

Table 28 shows the examples of the ALC setting for mic recording.

| Register Name | Comment | fs=8kHz | | fs=44.1kHz | |
|---|---|---|---|---|---|
| | | Data | Operation | Data | Operation |
| LMTH | Limiter detection Level | 01 | –4.1dBFS | 01 | –4.1dBFS |
| ZELMN | Limiter zero crossing detection | 0 | Enable | 0 | Enable |
| ZTM1-0 | Zero crossing timeout period | 00 | 16ms | 10 | 11.6ms |
| WTM1-0 | Recovery waiting period *WTM1-0 bits should be the same data as ZTM1-0 bits | 00 | 16ms | 10 | 11.6ms |
| REF7-0 | Maximum gain at recovery operation | E1H | +30dB | E1H | +30dB |
| IVL7-0, IVR7-0 | Gain of IVOL | 91H | 0dB | 91H | 0dB |
| LMAT1-0 | Limiter ATT step | 00 | 1 step | 00 | 1 step |
| RGAIN1-0 | Recovery GAIN step | 00 | 1 step | 00 | 1 step |
| ALC | ALC enable | 1 | Enable | 1 | Enable |

Table 28. Example of the ALC setting

The following registers should not be changed during the ALC operation. These bits should be changed after the ALC operation is finished by ALC bit = "0" or PMADL=PMADR bits = "0".

- **LMTH, LMAT1-0, WTM1-0, ZTM1-0, RGAIN1-0, REF7-0, ZELMN**



Example:
  Limiter = Zero crossing Enable
  Recovery Cycle = 16ms@8kHz
  Limiter and Recovery Step = 1
  Maximum Gain = +30.0dB
  Limiter Detection Level = –4.1dBFS
  ALC bit = "1"

Manual Mode

WR (IVL/R7-0)   * The value of IVOL should be the same or smaller than REF's

WR (ZTM1-0, WTM1-0)

WR (REF7-0)

WR (LMAT1-0, RGAIN1-0, ZELMN, LMTH1-0; ALC= "1")

ALC Operation

(1) Addr=18H&19H, Data=91H

(2) Addr=1AH, Data=00H

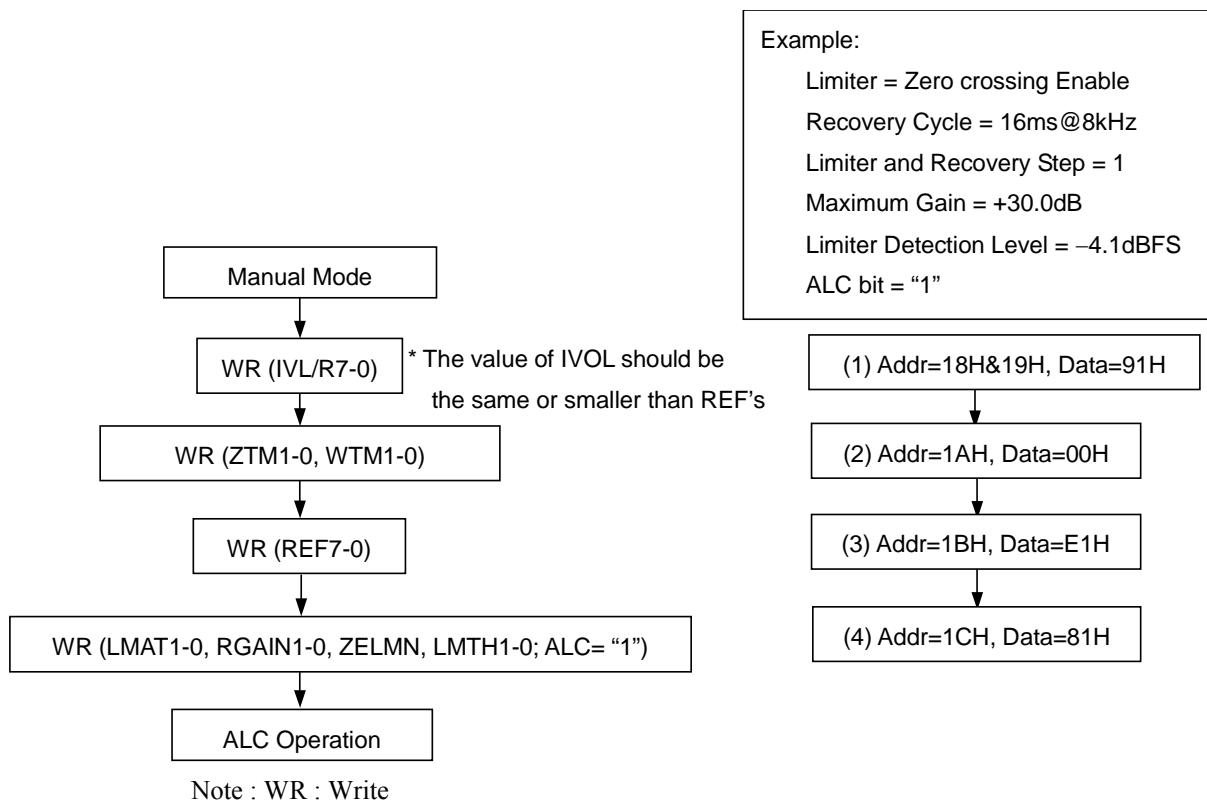(3) Addr=1BH, Data=E1H

(4) Addr=1CH, Data=81H

Note : WR : Write

Figure 39. Registers set-up sequence at ALC operation

## ■ Input Digital Volume (Manual Mode)

The input digital volume becomes a manual mode when ALC bit is "0". This mode is used in the case shown below.

1. After exiting reset state, set-up the registers for the ALC operation (ZTM1-0, LMTH and etc)
2. When the registers for the ALC operation (Limiter period, Recovery period and etc) are changed.
   For example; when the change of the sampling frequency.
3. When IVOL is used as a manual volume.

IVL7-0 and IVR7-0 bits set the gain of the volume control (Table 29). The IVOL value is changed at zero crossing or timeout. Zero crossing timeout period is set by ZTM1-0 bits.

If IVL7-0 or IVR7-0 bits are written during PMADL=PMADR bits = "0", IVOL operation starts with the written values at the end of the ADC initialization cycle after PMADL or PMADR bit is changed to "1".

| IVL7-0<br>IVR7-0 | GAIN (dB) | Step | |
|---|---|---|---|
| F1H | +36.0 | | |
| F0H | +35.625 | | |
| EFH | +35.25 | | |
| : | : | | |
| 92H | +0.375 | | |
| 91H | 0.0 | 0.375dB | (default) |
| 90H | −0.375 | | |
| : | : | | |
| 03H | −53.25 | | |
| 02H | −53.625 | | |
| 01H | −54 | | |
| 00H | MUTE | | |

Table 29. Input Digital Volume Setting

When writing to the IVL7-0 and IVR7-0 bits continuouslly, the control register should be written in an interval more than zero crossing timeout. If not, IVL and IVR are not changed since zero crossing counter is reset at every write operation. If the same register value as the previous write operation is written to IVL and IVR, this write operation is ignored and zero crossing counter is not reset. Therefore, IVL and IVR can be written in an interval less than zero crossing timeout.

| | | | | |
|---|---|---|---|---|
| ALC bit | | | | |
| ALC Status | Disable | Enable | | Disable |
| IVL7-0 bits | | E1H(+30dB) | | |
| IVR7-0 bits | | C6H(+20dB) | | |
| Internal IVL | E1H(+30dB) | E1(+30dB) --> F1(+36dB) | | E1(+30dB) |
| | | (1) | | (2) |
| Internal IVR | C6H(+20dB) | E1(+30dB) --> F1(+36dB) | | C6H(+20dB) |

Figure 40. IVOL value during ALC operation

(1) The IVL value becomes the start value if the IVL and IVR are different when the ALC starts. The wait time from ALC bit = "1" to ALC operation start by IVL7-0 bits is at most recovery time (WTM1-0 bits) plus zerocross timeout period (ZTM1-0 bits).

(2) Writing to IVL and IVR registers (18H and 19H) is ignored during ALC operation. After ALC is disabled, the IVOL changes to the last written data by zero crossing or timeout. When ALC is enabled again, ALC bit should be set to "1" by an interval more than zero crossing timeout period after ALC bit = "0".

## ■ System Reset

When power-up, the AK5701 should be reset by bringing the PDN pin = "L". This ensures that all internal registers reset to their initial values.

The ADC enters an initialization cycle that starts when the PMADL or PMADR bit is changed from "0" to "1". The initialization cycle time is 3088/fs=70.0ms@fs=44.1kHz when HPF1-0 bits are "00" (Table 30). During the initialization cycle, the ADC digital data outputs of both channels are forced to a 2's compliment, "0". The ADC output reflects the analog input signal after the initialization cycle is complete.

| HPF1 bit | HPF0 bit | Init Cycle | | | | |
|---|---|---|---|---|---|---|
| | | Cycle | fs=44.1kHz | fs=22.05kHz | fs=11.025kHz | |
| 0 | 0 | 3088/fs | 70.0ms (Recommendation) | 140.0ms | 280.1ms | (default) |
| 0 | 1 | 1552/fs | 35.2ms | 70.4ms (Recommendation) | 140.8ms | |
| 1 | 0 | 784/fs | 17.8ms | 35.6ms | 71.1ms (Recommendation) | |
| 1 | 1 | N/A | N/A | N/A | N/A | |

Table 30. ADC Initialization Cycle (N/A: Not available)

**AKM**

## ■ Serial Control Interface

Internal registers may be written by using the 3-wire µP interface pins (CSN, CCLK and CDTI). The CSP pin selects the polarity of the CSN pin and chip address.

1)   CSP pin = "L"
The data on this interface consists of a 2-bit Chip address (Fixed to "10"), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Address and data are latched on the 16th CCLK rising edge ("↑") after CSN falling edge("↓"). CSN should be set to "H" once after 16 CCLKs for each address. Clock speed of CCLK is 7MHz (max). The value of internal registers are initialized by the PDN pin = "L".
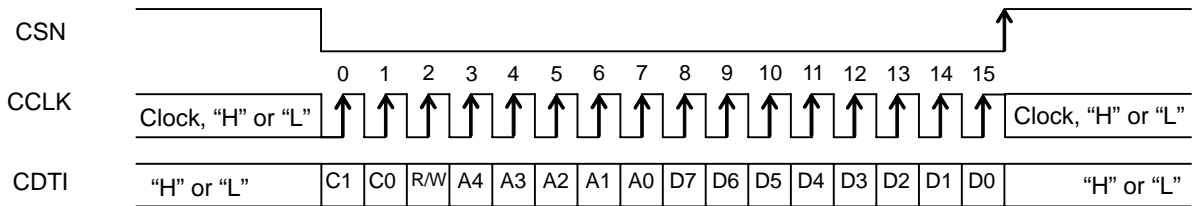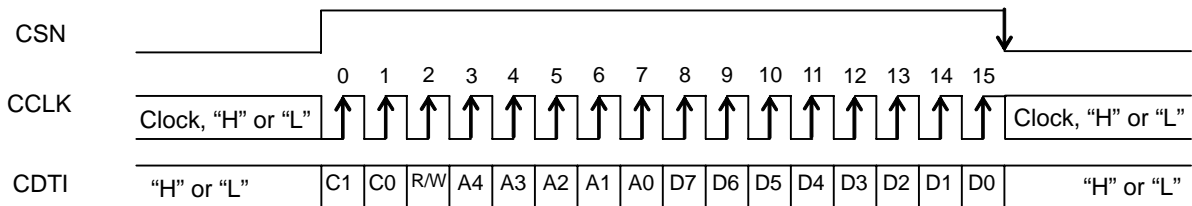


C1-C0:    Chip Address (C1 = "1", C0 = CAD0) ; Fixed to "10"
R/W:       READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A4-A0:    Register Address
D7-D0:    Control data

Figure 41. Serial Control I/F Timing (CSP pin = "L")

2)   CSP pin = "H"
The data on this interface consists of a 2-bit Chip address (Fixed to "01"), Read/Write (Fixed to "1"), Register address (MSB first, 5bits) and Control data (MSB first, 8bits). Each bit is clocked in on the rising edge ("↑") of CCLK. Address and data are latched on the 16th CCLK rising edge ("↑") after CSN rising edge("↑"). CSN should be set to "L" once after 16 CCLKs for each address. Clock speed of CCLK is 7MHz (max). The value of internal registers are initialized by the PDN pin = "L".



C1-C0:    Chip Address (C1 = "0", C0 = CAD1) ; Fixed to "01"
R/W:       READ/WRITE ("1": WRITE, "0": READ); Fixed to "1"
A4-A0:    Register Address
D7-D0:    Control data

Figure 42. Serial Control I/F Timing (CSP pin = "H")

**AKM**

## ■ Register Map

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-----|-----|------|------|------|--------|---------|--------|
| 10H | Power Management | 0 | 0 | 0 | 0 | 0 | PMVCM | PMADR | PMADL |
| 11H | PLL Control | 0 | 0 | PLL3 | PLL2 | PLL1 | PLL0 | M/S | PMPLL |
| 12H | Signal Select | 0 | 0 | 0 | PMMP | MDIF2 | MDIF1 | INR | INL |
| 13H | Mic Gain Control | 0 | 0 | 0 | 0 | 0 | 0 | MGAIN1 | MGAIN0 |
| 14H | Audio Format Select | 0 | 0 | 1 | MIX | MSBS | BCKP | DIF1 | DIF0 |
| 15H | fs Select | HPF1 | HPF0 | BCKO1 | BCKO0 | FS3 | FS2 | FS1 | FS0 |
| 16H | Clock Output Select | 0 | 0 | 0 | 0 | THR | MCKO | PS1 | PS0 |
| 17H | Volume Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IVOLC |
| 18H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 19H | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| 1AH | Timer Select | 0 | 0 | 0 | 0 | ZTM1 | ZTM0 | WTM1 | WTM0 |
| 1BH | ALC Mode Control 1 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| 1CH | ALC Mode Control 2 | ALC | ZELMN | LMAT1 | LMAT0 | RGAIN1 | RGAIN0 | LMTH1 | LMTH0 |
| 1DH | Mode Control 1 | TE3 | TE2 | TE1 | TE0 | 0 | 0 | 0 | 0 |
| 1EH | Mode Control 2 | 0 | 0 | 0 | 0 | 0 | 0 | TMASTER | 0 |

Note 31. PDN pin = "L" resets the registers to their default values.
Note 32. "0" must be sent to the register written as "0" and "1" must be sent to the register written as "1". For addresses
except for 10H to 1EH, data must not be written.

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## ■ Register Definitions

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|-------|-------|-------|
| 10H | Power Management | 0 | 0 | 0 | 0 | 0 | PMVCM | PMADR | PMADL |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PMADL: MIC-Amp Lch and ADC Lch Power Management
   0: Power down (default)
   1: Power up

PMADR: MIC-Amp Rch and ADC Rch Power Management
   0: Power down (default)
   1: Power up
      When the PMADL or PMADR bit is changed from "0" to "1", the initialization cycle (3088/fs=70.0ms@fs= 44.1kHz, HPF1-0 bits = "00") starts. After initializing, digital data of the ADC is output.

PMVCM: VCOM Power Management
   0: Power down (default)
   1: Power up
      When any blocks are powered-up, the PMVCM bit must be set to "1". PMVCM bit can be set to "0" only when PMADL=PMADR=PMPLL=PMMP=MCKO bits = "0".

Each block can be powered-down respectively by writing "0" in each bit of this address. When the PDN pin is "L", all blocks are powered-down regardless as setting of this address. In this case, register is initialized to the default value.

When PMVCM, PMADL, PMADR, PMPLL and MCKO bits are "0", all blocks are powered-down. The register values remain unchanged. Power supply current is 20µA(typ) in this case. For fully shut down (typ. 1µA), the PDN pin should be "L".

When the ADC is not used, external clocks may not be present. When ADC is used, external clocks must always be present.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|------|------|------|------|-----|-------|
| 11H | PLL Control | 0 | 0 | PLL3 | PLL2 | PLL1 | PLL0 | M/S | PMPLL |
| | Default | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |

PMPLL: PLL Power Management
   0: EXT Mode and Power Down (default)
   1: PLL Mode and Power up

M/S: Master / Slave Mode Select
   0: Slave Mode (default)
   1: Master Mode

PLL3-0: PLL Reference Clock Select (Table 4)
   Default: "1001"(MCKI pin=12MHz)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|------|------|------|-----|-----|
| 12H | Signal Select | 0 | 0 | 0 | PMMP | MDIF2 | MDIF1 | INR | INL |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

INL: ADC Lch Input Source Select
    0: LIN1 pin (default)
    1: LIN2 pin

INR: ADC Rch Input Source Select
    0: RIN1 pin (default)
    1: RIN2 pin

MDIF1: ADC Lch Input Type Select
    0: Single-ended input (LIN1/LIN2 pin: default)
    1: Full-differential input (LIN+/LIN− pin)

MDIF2: ADC Rch Input Type Select
    0: Single-ended input (RIN1/RIN2 pin: default)
    1: Full-differential input (RIN+/RIN− pin)

PMMP: MPWR pin Power Management
    0: Power down: Hi-Z (default)
    1: Power up

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|--------|--------|
| 13H | Mic Gain Control | 0 | 0 | 0 | 0 | 0 | 0 | MGAIN1 | MGAIN0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

MGAIN1-0: MIC-Amp Gain Control (Table 20)
    Default: "01"(+15dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|-----|------|------|------|------|
| 14H | Audio Format Select | 0 | 0 | 1 | MIX | MSBS | BCKP | DIF1 | DIF0 |
| | Default | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |

DIF1-0: Audio Interface Format (Table 15)
    Default: "11" (I²S)

BCKP: BCLK/EXBCLK Polarity at DSP Mode (Table 16)
    "0": SDTO is output by the rising edge ("↑") of BCLK/EXBCLK. (default)
    "1": SDTO is output by the falling edge ("↓") of BCLK/EXBCLK.

MSBS: LRCK/EXLRCK Polarity at DSP Mode (Table 16)
    "0": The rising edge ("↑") of LRCK/EXLRCK is half clock of BCLK/EXBCLK before the channel change. (default)
    "1": The rising edge ("↑") of LRCK/EXLRCK is one clock of BCLK/EXBCLK before the channel change.

MIX: ADC Output Data Select (Table 17)
    "0": Normal operation (default)
    "1": (L+R)/2

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-----|------|-------|-------|-----|-----|-----|-----|
| 15H | fs Select | HPF1 | HPF0 | BCKO1 | BCKO0 | FS3 | FS2 | FS1 | FS0 |
| | Default | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |

FS3-0: Sampling Frequency Select (Table 5 and Table 6) and MCKI Frequency Select (Table 11)
    Default: "1111" (44.1kHz)
        FS3-0 bits select sampling frequency at PLL mode and MCKI frequency at EXT mode.

BCKO1-0: BCLK Output Frequency Select at Master Mode (Table 10)
    Default: "01" (32fs)

HPF1-0: Offset Cancel HPF Cut-off Frequency and ADC Initialization Cycle (Table 18, Table 30)
    Default: "00" (fc=3.4Hz@fs=44.1kHz, Init Cycle=3088/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-----|------|-------|-------|-----|-----|-----|-----|
| 16H | Clock Output Select | 0 | 0 | 0 | 0 | THR | MCKO | PS1 | PS0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

PS1-0: MCKO Output Frequency Select (Table 9)
    Default: "00"(256fs)

MCKO: Master Clock Output Enable
    0: Disable: MCKO pin = "L" (default)
    1: Enable: Output frequency is selected by PS1-0 bits.

THR: Bypass Mode (Table 14)
    0: OFF (default)
    1: ON

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|-----|------|------|------|-----|-----|-----|-------|
| 17H | Volume Control | 0 | 0 | 0 | 0 | 0 | 0 | 0 | IVOLC |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

IVOLC: Input Digital Volume Control Mode Select
    0: Independent
    1: Dependent (default)
        When IVOLC bit = "1", IVL7-0 bits control both Lch and Rch volume level, while register values of IVL7-0 bits are not written to IVR7-0 bits. When IVOLC bit = "0", IVL7-0 bits control Lch level and IVR7-0 bits control Rch level, respectively.

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|------|------|------|------|------|------|------|------|
| 18H | Lch Input Volume Control | IVL7 | IVL6 | IVL5 | IVL4 | IVL3 | IVL2 | IVL1 | IVL0 |
| 19H | Rch Input Volume Control | IVR7 | IVR6 | IVR5 | IVR4 | IVR3 | IVR2 | IVR1 | IVR0 |
| | Default | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |

IVL7-0, IVR7-0: Input Digital Volume; 0.375dB step, 242 Level (Table 29)
    Default: "91H" (0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1AH | Timer Select | 0 | 0 | 0 | 0 | ZTM1 | ZTM0 | WTM1 | WTM0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

WTM1-0: ALC Recovery Waiting Period (Table 25)
   Default: "00" (128/fs)

ZTM1-0: ALC Limiter/Recovery Operation Zero Crossing Timeout Period (Table 24)
   Default: "00" (128/fs)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1BH | ALC Mode Control 1 | REF7 | REF6 | REF5 | REF4 | REF3 | REF2 | REF1 | REF0 |
| | Default | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

REF7-0: Reference Value at ALC Recovery Operation. 0.375dB step, 242 Level (Table 27)
   Default: "E1H" (+30.0dB)

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| 1CH | ALC Mode Control 2 | ALC | ZELMN | LMAT1 | LMAT0 | RGAIN1 | RGAIN0 | LMTH1 | LMTH0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

LMTH1-0: ALC Limiter Detection Level / Recovery Counter Reset Level (Table 22)
   Default: "00"

RGAIN1-0: ALC Recovery GAIN Step (Table 26)
   Default: "00"

LMAT1-0: ALC Limiter ATT Step (Table 23)
   Default: "00"

ZELMN: Zero Crossing Detection Enable at ALC Limiter Operation
   0: Enable (default)
   1: Disable

ALC: ALC Enable
   0: ALC Disable (default)
   1: ALC Enable

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|----|----|
| 1DH | Mode Control 1 | TE3 | TE2 | TE1 | TE0 | 0 | 0 | 0 | 0 |
| | Default | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |

TE3-0: EXT Master Mode Enable

When TE3-0 bits is set to "0101", the write operation to addr=1EH is enabled.

TE3-0 bits should be set to "1010" except for EXT Master Mode.

TE3-0 bits must not be set to the value except for "1010" and "0101".

Default: "1010"

| Addr | Register Name | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|---------------|----|----|----|----|----|----|---------|----|
| 1EH | Mode Control 2 | 0 | 0 | 0 | 0 | 0 | 0 | TMASTER | 0 |
| | Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

TMASTER: EXT Master Mode

The write operation to TMASTER bit is enabled when TE3-0 bits = "0101".

0: Except EXT Master Mode (default)

1: EXT Master Mode

**SYSTEM DESIGN**

Figure 43 and Figure 44 shows the system connection diagram for the AK5701. The evaluation board [AKD5701] demonstrates the optimum layout, power supply arrangements and measurement results.
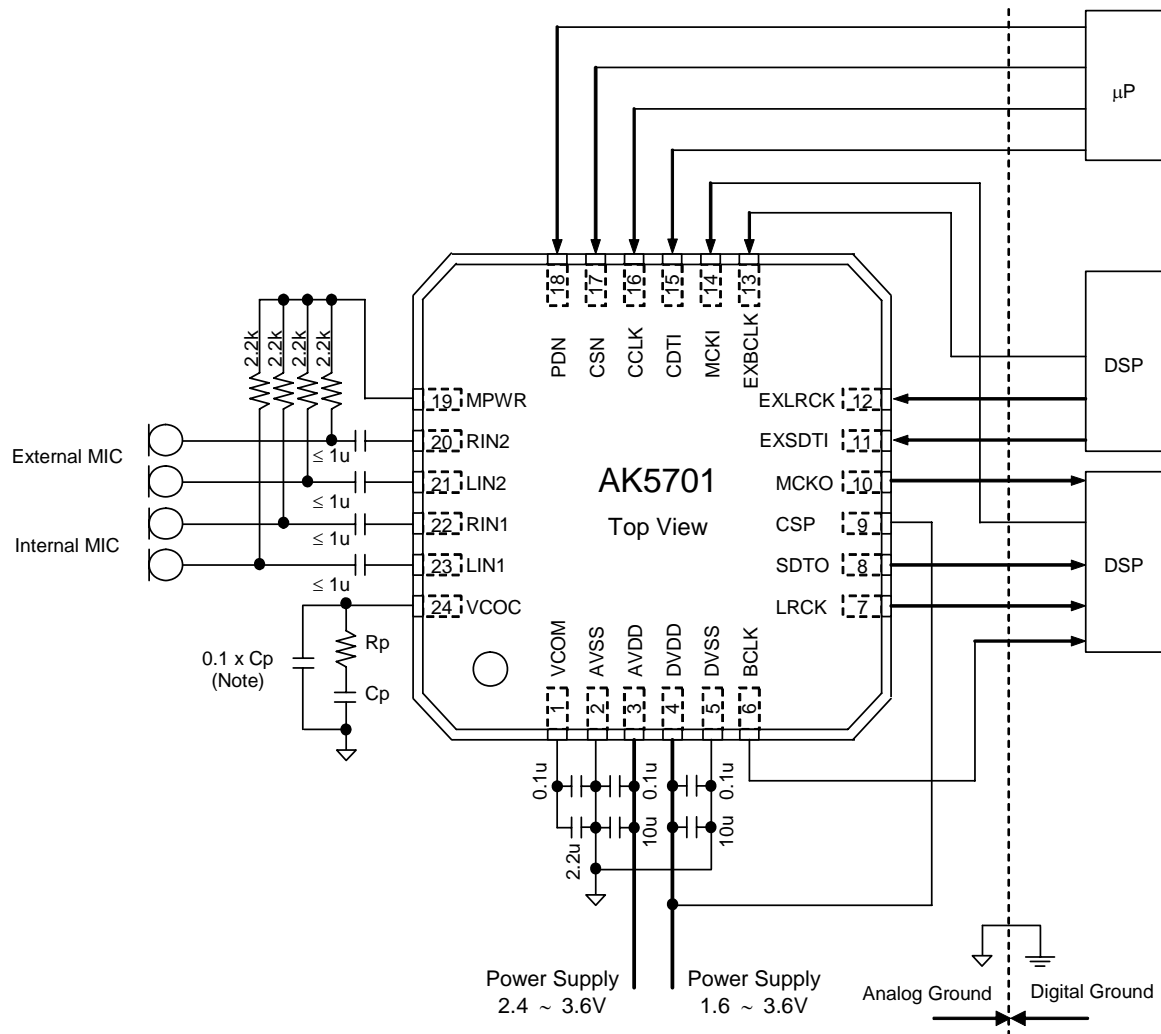


Notes:
  - AVSS and DVSS of the AK5701 should be distributed separately from the ground of external controllers.
  - All digital input pins should not be left floating.
  - When the AK5701 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of the VCOC pin is not needed.
  - When the AK5701 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of the VCOC pin is shown in Table 4. 0.1 x Cp in parallel with Cp+Rp improves PLL jitter characteristics.
  - Mic input AC coupling capacitor should be 1μF or less to start the recording within 100ms.

Figure 43. Typical Connection Diagram (MIC Input)
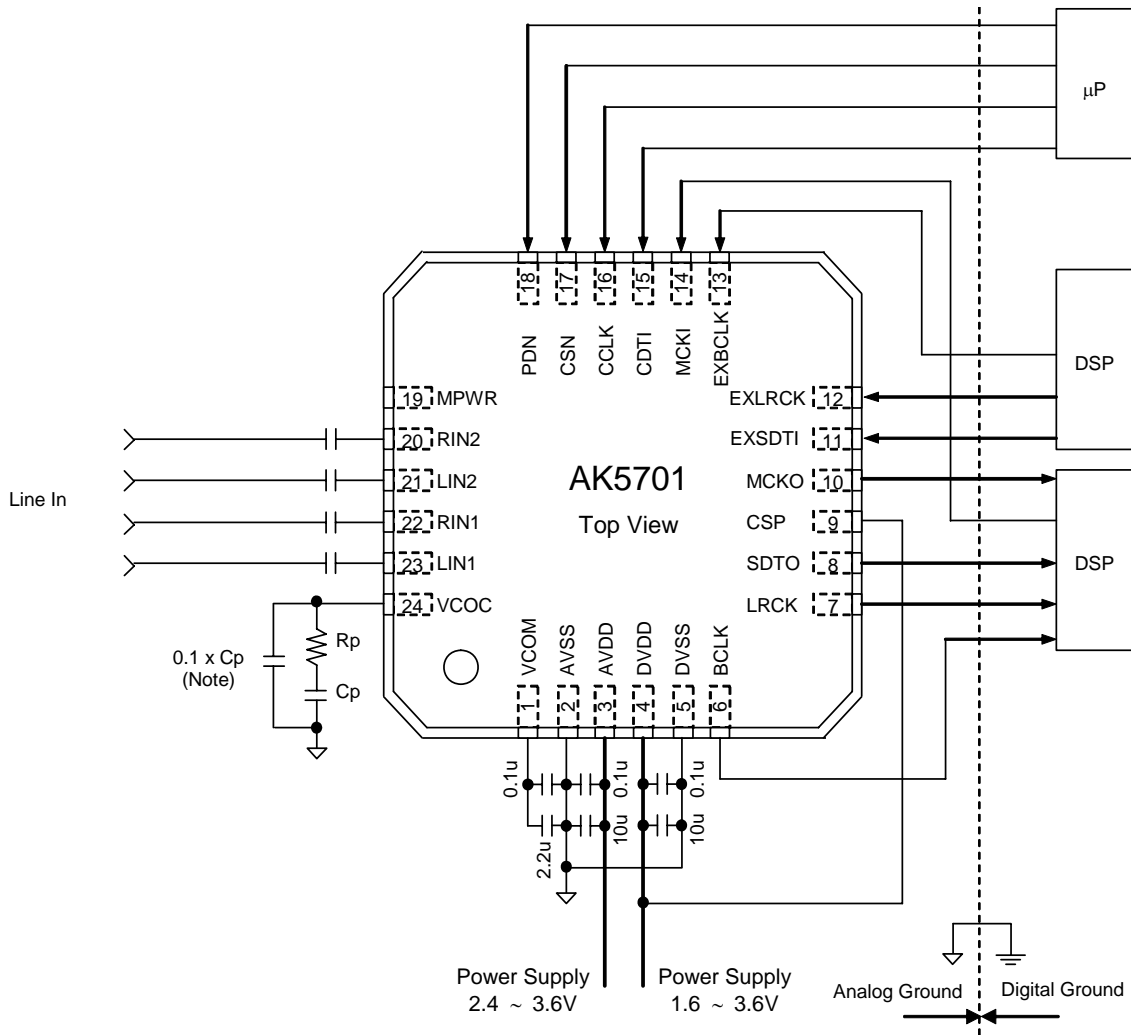
Notes:
- AVSS and DVSS of the AK5701 should be distributed separately from the ground of external controllers.
- All digital input pins should not be left floating.
- When the AK5701 is EXT mode (PMPLL bit = "0"), a resistor and capacitor of the VCOC pin is not needed.
- When the AK5701 is PLL mode (PMPLL bit = "1"), a resistor and capacitor of the VCOC pin is shown in Table 4. 0.1 x Cp in parallel with Cp+Rp improves PLL jitter characteristics.

Figure 44. Typical Connection Diagram (Line Input)

## 1. Grounding and Power Supply Decoupling

The AK5701 requires careful attention to power supply and grounding arrangements. AVDD and DVDD are usually supplied from the system's analog supply. If AVDD and DVDD are supplied separately, the power-up sequence is not critical. AVSS and DVSS of the AK5701 should be connected to the analog ground plane. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK5701 as possible, with the small value ceramic capacitor being the nearest.

## 2. Voltage Reference

VCOM is a signal ground of this chip. A 2.2μF electrolytic capacitor in parallel with a 0.1μF ceramic capacitor attached to the VCOM pin eliminates the effects of high frequency noise. No load current may be drawn from the VCOM pin. All signals, especially clocks, should be kept away from the VCOM pin in order to avoid unwanted coupling into the AK5701.

## 3. Analog Inputs

The analog inputs are single-ended or full-differential and input resistance is 60kΩ (typ)@MGAIN1-0 bits = "00", 30kΩ (typ)@MGAIN1-0 bits = "01" or "10". The input signal range scales with 0.6 x AVDD Vpp(typ)@MGAIN 1-0 bits = "00" centered around the internal common voltage (0.5 x AVDD). Usually the input signal is AC coupled using a capacitor. The cut-off frequency is fc = $1/(2\pi RC)$. The ADC output data format is 2's complement. The DC offset including the ADC's own DC offset is removed by the internal HPF (fc=3.4Hz@ HPF1-0 bits = "00", fs=44.1kHz). The AK5701 can accept input voltages from AVSS to AVDD at single-ended.

**CONTROL SEQUENCE**

## ■ Clock Set up

When ADC is powered-up, the clocks must be supplied.

   1. PLL Master Mode.



Example:

    Audio I/F Format: I2S
    BCLK frequency at Master Mode: 64fs
    Input Master Clock Select at PLL Mode: 11.2896MHz
    MCKO: Enable
    Sampling Frequency: 44.1kHz

(1) Power Supply & PDN pin = "L" → "H"

(2) Addr:11H, Data:12H
    Addr:14H, Data:23H
    Addr:15H, Data:2FH

(3) Addr:10H, Data:04H

(4) Addr:16H, Data:04H
    Addr:11H, Data:13H

MCKO, BCLK and LRCK output
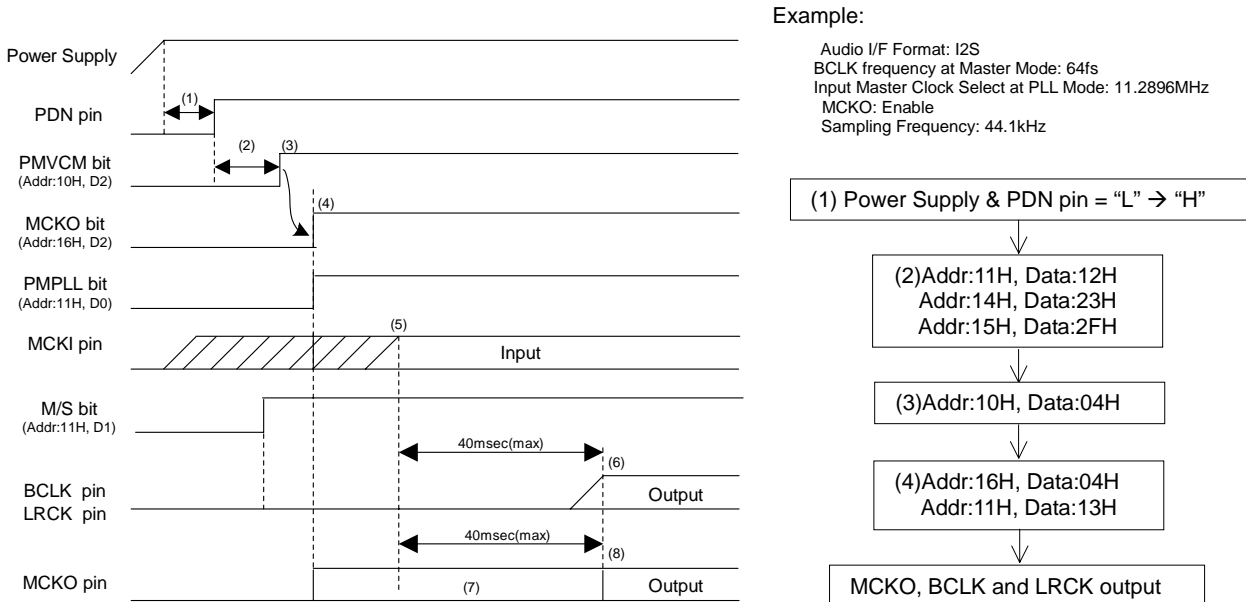
Figure 45. Clock Set Up Sequence (1)

<Example>
   (1) After Power Up, PDN pin "L" → "H"
       "L" time of 150ns or more is needed to reset the AK5701.
   (2) DIF1-0, PLL3-0, FS3-0, BCKO1-0 and M/S bits should be set during this period as follows.
       (2a) M/S bit = "1" and setting of PLL3-0, FS3-0, BCKO1-0 bits.
       (2b) Setting of DIF1-0 bits.
   (3) Power UpVCOM: PMVCM bit = "0" → "1"
       VCOM should first be powered-up before the other block operates.
   (4) In case of using MCKO output: MCKO bit = "1"
       In case of not using MCKO output: MCKO bit = "0"
   (5) PLL operation starts after PMPLL bit changes from "0" to "1" and MCKI is supplied from an external source.
       PLL lock time is 40ms(max) at MCKI=12MHz (Table 4).
   (6) The AK5701 starts to output the LRCK and BCLK clocks after the PLL becomes stable. Then normal operation
       starts.
   (7) The invalid frequency is output from the MCKO pin during this period if MCKO bit = "1".
   (8) The normal clock is output from the MCKO pin after the PLL is locked if MCKO bit = "1".

2. PLL Slave Mode (EXLRCK or EXBCLK pin)



Example:
Audio I/F Format : I2S
PLL Reference clock: EXBCLK
EXBCLK frequency: 64fs
Sampling Frequency: 44.1kHz

(1) Power Supply & PDN pin = "L" → "H"

(2) Addr:11H, Data:0CH
Addr:14H, Data:23H
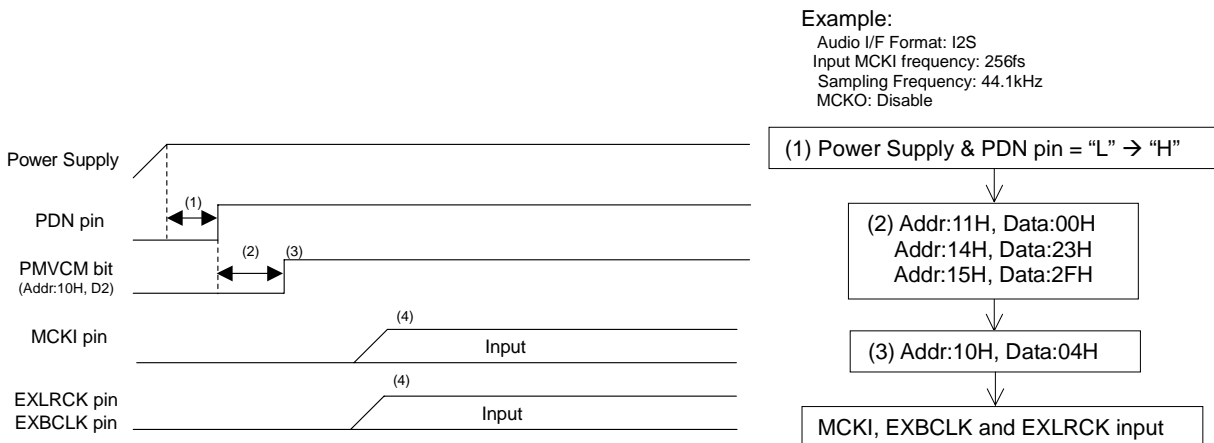Addr:15H, Data:2FH

(3) Addr:10H, Data:04H

(4) Addr:11H, Data:0DH
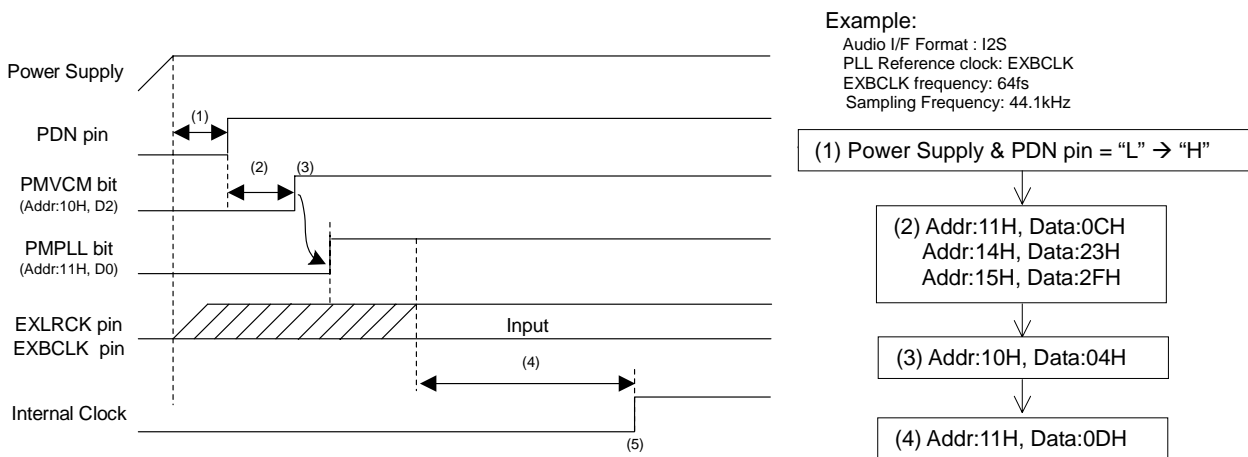
Figure 46. Clock Set Up Sequence (2)

<Example>
(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5701.
(2) DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (EXLRCK or EXBCLK pin) is supplied. PLL lock time is 160ms(max) when EXLRCK is a PLL reference clock. PLL lock time is 2ms(max) when EXBCLK is a PLL reference clock and the external circuit at the VCOC pin is 10k+4.7nF (Table 4).
(5) Normal operation stats after that the PLL is locked.

3. PLL Slave Mode (MCKI pin)

Example:

Audio I/F Format: I2S
BCLK frequency at Master Mode: 64fs
Input Master Clock Select at PLL Mode: 11.2896MHz
MCKO: Enable
Sampling Frequency: 44.1kHz
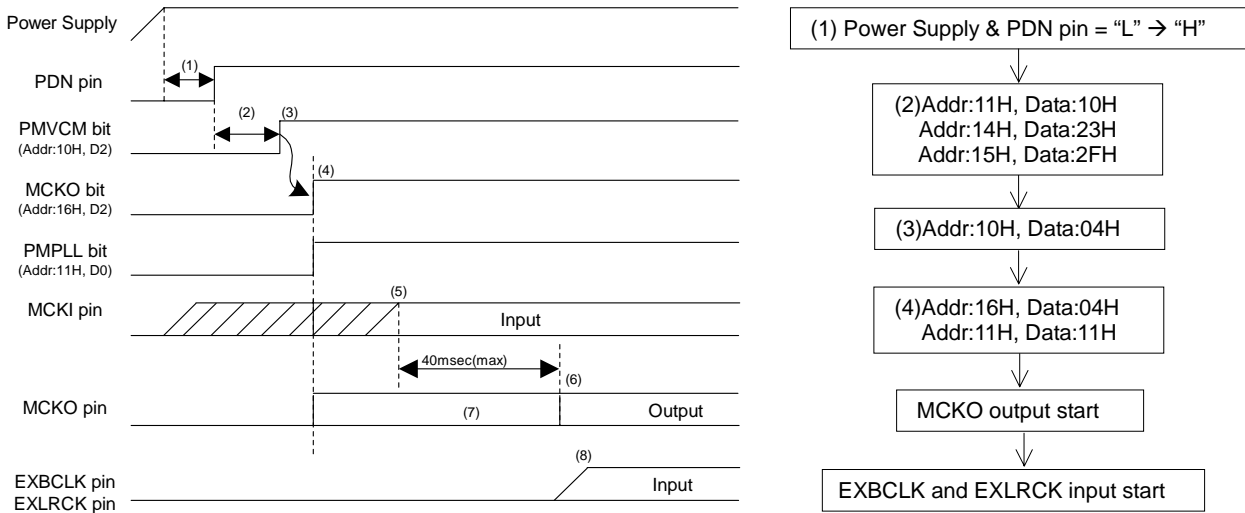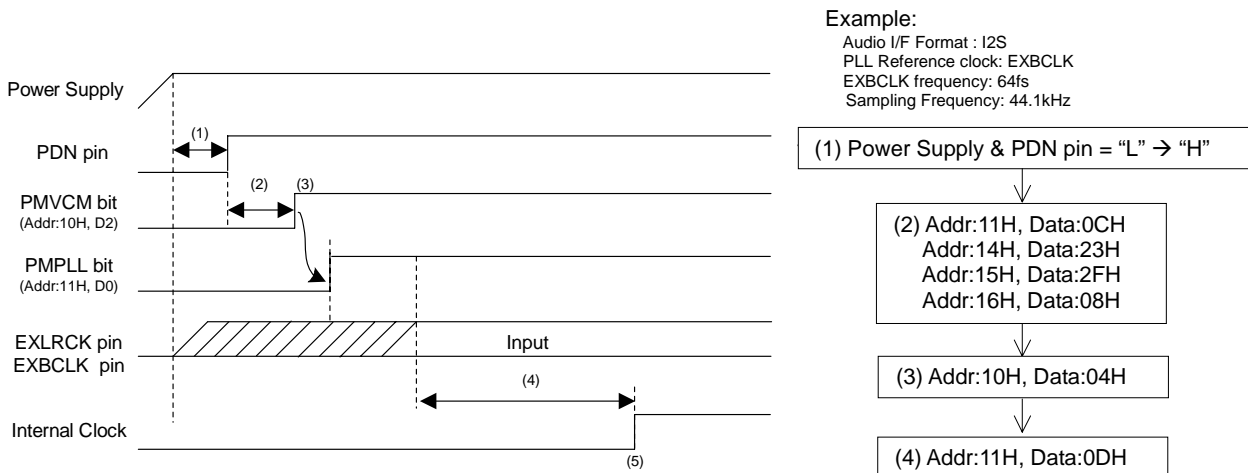


Figure 47. Clock Set Up Sequence (3)

<Example>
  (1) After Power Up: PDN pin "L" → "H"
     "L" time of 150ns or more is needed to reset the AK5701.
  (2) DIF1-0, PLL3-0, FS3-0, BCKO1-0 and M/S bits should be set during this period.
  (3) Power Up VCOM: PMVCM bit = "0" → "1"
     VCOM should first be powered up before the other block operates.
  (4) Enable MCKO output: MCKO bit = "1"
  (5) PLL starts after that the PMPLL bit changes from "0" to "1" and PLL reference clock (MCKI pin) is supplied.
     PLL lock time is 40ms(max) at MCKI=12MHz (Table 4).
  (6) The normal clock is output from MCKO after PLL is locked.
  (7) The invalid frequency is output from MCKO during this period.
  (8) EXBCLK and EXLRCK clocks should be synchronized with MCKO clock.

4. EXT Slave Mode

Example:
Audio I/F Format: I2S
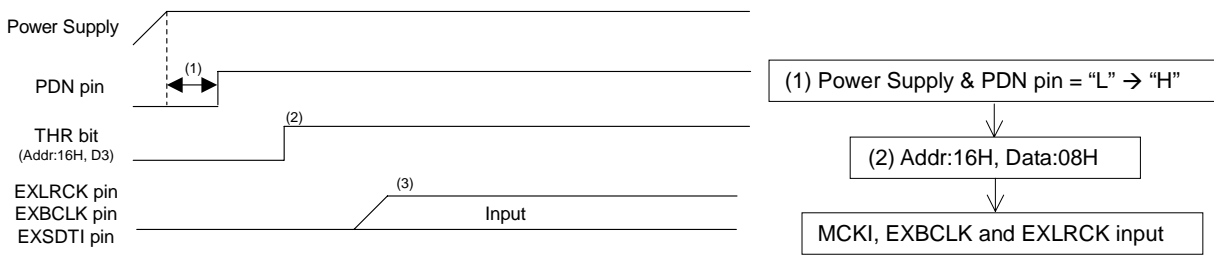Input MCKI frequency: 256fs
Sampling Frequency: 44.1kHz
MCKO: Disable



Figure 48. Clock Set Up Sequence (4)

<Example>
(1) After Power Up: PDN pin "L" → "H"
"L" time of 150ns or more is needed to reset the AK5701.
(2) DIF1-0 and FS1-0 bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
VCOM should first be powered up before the other block operates.
(4) Normal operation starts after the MCKI, EXLRCK and EXBCLK are supplied.

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5. EXT Master Mode
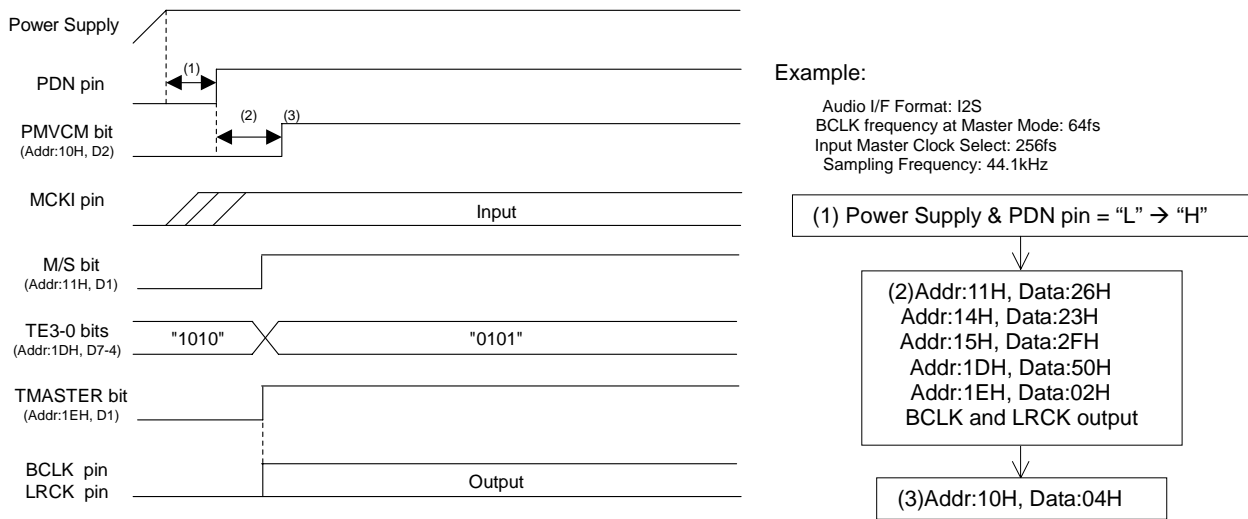


Figure 49. Clock Set Up Sequence (5)

<Example>
    (1) After Power Up: PDN pin "L" → "H"
      "L" time of 150ns or more is needed to reset the AK5701.
    (2) DIF1-0, FS1-0, BCKO1-0, M/S, TE3-0 and TMASTER bits should be set during this period as follows.
      (2a) M/S bit = "1", setting of FS3-0 and BCKO1-0 bits.
      (2b) Setting of DIF1-0 bits.
      (2c) TE3-0 bits = "0101"
      (2d) TMASTER bit = "1": BCLK and LRCK start to output.
    (3) Power Up VCOM: PMVCM bit = "0" → "1"
      VCOM should first be powered up before the other block operates.

When the clock mode is changed from EXT Master Mode to other modes, the register should be set as Table 1 after PDN pin = "L" to "H" or TE3-0 bits = "1010".

## 6. Slave & Bypass Mode



Example:
    Audio I/F Format : I2S
    PLL Reference clock: EXBCLK
    EXBCLK frequency: 64fs
    Sampling Frequency: 44.1kHz

(1) Power Supply & PDN pin = "L" → "H"

(2) Addr:11H, Data:0CH
    Addr:14H, Data:23H
    Addr:15H, Data:2FH
    Addr:16H, Data:08H

(3) Addr:10H, Data:04H

(4) Addr:11H, Data:0DH

Figure 50. Clock Set Up Sequence (6)

<Example>
(1) After Power Up: PDN pin "L" → "H"
    "L" time of 150ns or more is needed to reset the AK5701.
(2) THR bit should be set to "1" and DIF1-0, FS3-0 and PLL3-0 bits should be set during this period.
(3) Power Up VCOM: PMVCM bit = "0" → "1"
    VCOM should first be powered up before the other block operates.
(4) PLL starts after the PMPLL bit changes from "0" to "1" and PLL reference clock (EXLRCK or EXBCLK pin)
    is supplied. PLL lock time is 160ms(max) when EXLRCK is a PLL reference clock. PLL lock time is 2ms(max)
    when EXBCLK is a PLL reference clock and the external circuit at VCOC pin is 10k+4.7nF (Table 4).
(5) Normal operation stats after that the PLL is locked.

## 7. Bypass Mode



Figure 51. Clock Set Up Sequence (7)

<Example>
  (1) After Power Up: PDN pin "L" → "H"
      "L" time of 150ns or more is needed to reset the AK5701.
  (2) THR bit should be set to "1".
  (3) After EXLRCK, EXBCLK and EXSDTI are input, LRCK, BCLK and SDTO start to output.

**AKM**

## ■ MIC Input Recording (Stereo)
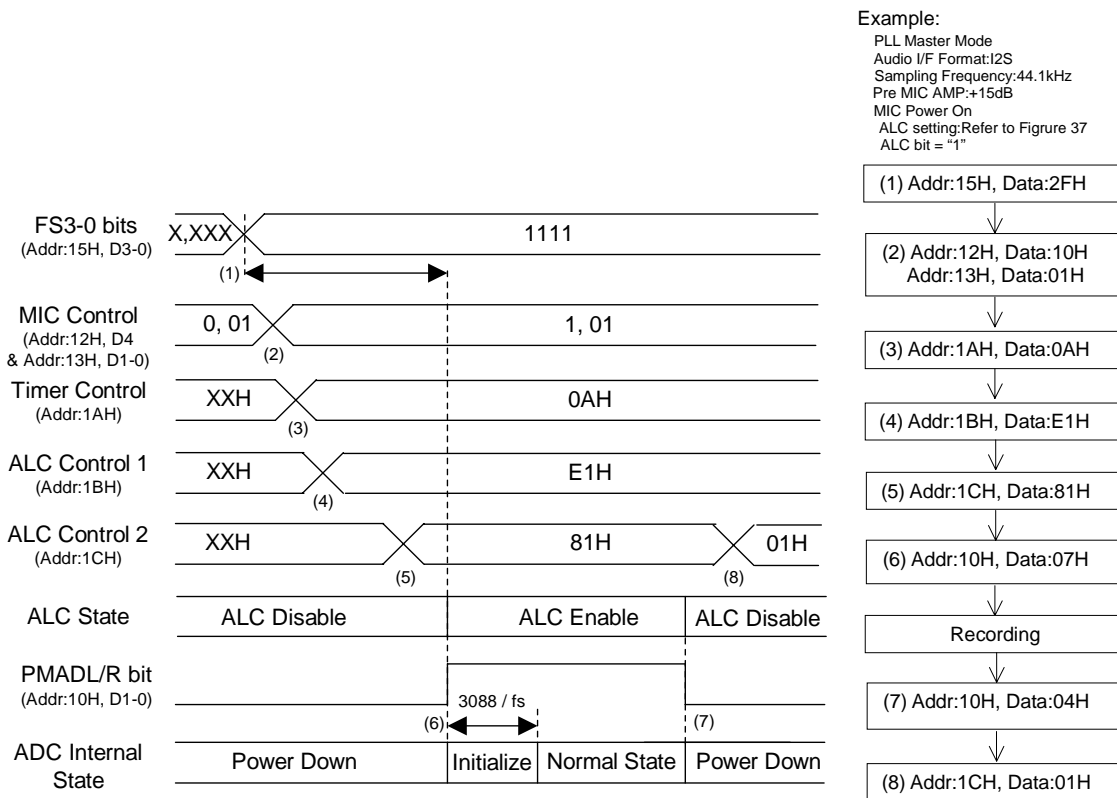


Figure 52. MIC Input Recording Sequence

<Example>
This sequence is an example of ALC setting at fs=44.1kHz. If the parameter of the ALC is changed, please refer to "Figure 39".

At first, clocks should be supplied according to "Clock Set Up" sequence.

(1) Set up a sampling frequency (FS3-0 bit). When the AK5701 is PLL mode, MIC and ADC should be powered-up in consideration of PLL lock time after a sampling frequency is changed.

(2) Set up MIC input (Addr: 12H&13H)

(3) Set up Timer Select for ALC (Addr: 1AH)

(4) Set up REF value for ALC (Addr: 1BH)

(5) Set up LMTH1-0, RGAIN1-0, LMAT1-0 and ALC bits (Addr: 1CH)

(6) Power Up MIC and ADC: PMADL = PMADR bits = "0" → "1"

The initialization cycle time of ADC is 3088/fs=70.0ms@fs=44.1kHz, HPF1-0 bits = "00".

After the ALC bit is set to "1" and MIC&ADC block is powered-up, the ALC operation starts from IVOL default value (0dB).

To start the recording within 100ms, the following sequence is required.

(6a) PMVCM=PMMP bits = "1".

(6b) Wait for 2ms, then PMPLL bit = "1".

(6c) Wait for 6ms, then PMADL=PMADR bits = "1".

(7) Power Down MIC and ADC: PMADL = PMADR bits = "1" → "0"

When the registers for the ALC operation are not changed, ALC bit may be kept as "1". The ALC operation is disabled because the MIC&ADC block is powered-down. If the registers for the ALC operation are also changed when the sampling frequency is changed, it should be executed after the AK5701 goes to the manual mode (ALC bit = "0") or MIC&ADC block is powered-down (PMADL=PMADR bits = "0"). IVOL gain is not reset when PMADL=PMADR bits = "0", and then IVOL operation starts from the setting value when PMADC or PMADR bit is changed to "1".

(8) ALC Disable: ALC bit = "1" → "0"

## ■ Stop of Clock

Master clock can be stopped when ADC is not used.

### 1. PLL Master Mode
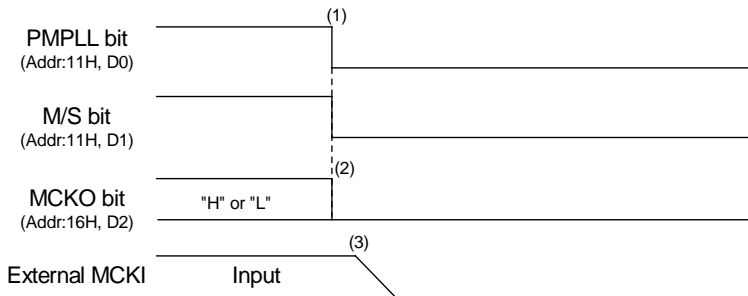


Example:

Audio I/F Format: I2S
BCLK frequency at Master Mode: 64fs
Input Master Clock Select at PLL Mode: 11.2896MHz
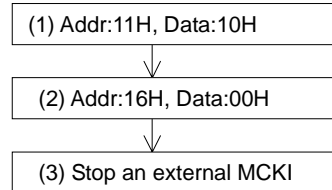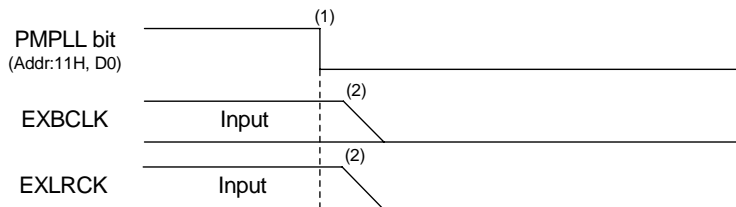Sampling Frequency: 44.1kHz

(1) Addr:11H, Data:10H

↓

(2) Addr:16H, Data:00H

↓

(3) Stop an external MCKI

Figure 53. Clock Stopping Sequence (1)

<Example>
(1) Power down PLL: PMPLL=M/S bits = "1" → "0"
(2) Stop MCKO clock: MCKO bit = "1" → "0"
(3) Stop an external master clock.

### 2. PLL Slave Mode (EXLRCK, EXBCLK pin)



Example

Audio I/F Format : I2S
PLL Reference clock: EXBCLK
BCLK frequency: 64fs
Sampling Frequency: 44.1kHz

(1) Addr:11H, Data:0CH

↓

(2) Stop the external clocks
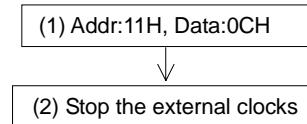
Figure 54. Clock Stopping Sequence (2)

<Example>
(1) Power down PLL: PMPLL bit = "1" → "0"
(2) Stop the external EXBCLK and EXLRCK clocks

 * Clock stop sequence is the same for Slave&Bypass Mode.

3. PLL Slave Mode (MCKI pin)
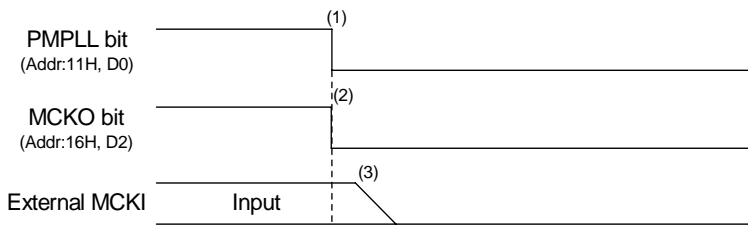


Example
 Audio I/F Format: I2S
 PLL Reference clock: MCKI= 11.2896MHz
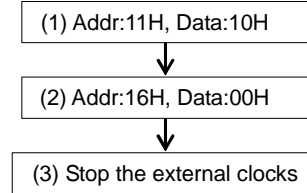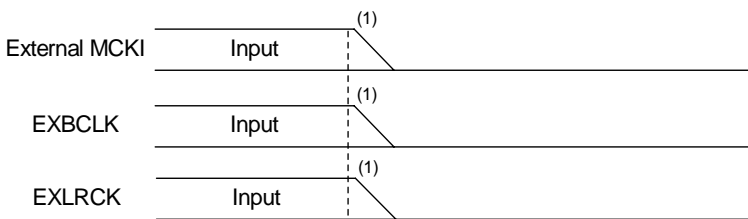 EXBCLK frequency: 64fs
 Sampling Frequency: 44.1kHz

| (1) Addr:11H, Data:10H |
| ↓ |
| (2) Addr:16H, Data:00H |
| ↓ |
| (3) Stop the external clocks |

Figure 55. Clock Stopping Sequence (3)

<Example>
   (1)   Power down PLL: PMPLL bit = "1" → "0"
   (2)   Stop MCKO output: MCKO bit = "1" → "0"
   (3)   Stop the external master clock.

4. EXT Slave Mode



Example
 Audio I/F Format :I2S
 Input MCKI frequency:256fs
 Sampling Frequency:44.1kHz

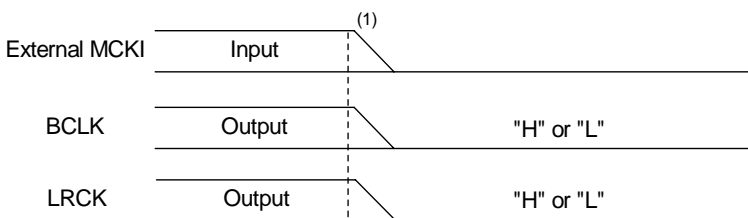| (1) Stop the external clocks |
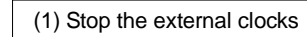
Figure 56. Clock Stopping Sequence (4)

<Example>
   (1)  Stop the external MCKI, EXBCLK and EXLRCK clocks.

   * Clock stop sequence is the same for Bypass Mode.

5. EXT Master Mode



Example
 Audio I/F Format :I2S
 Input MCKI frequency:256fs
 Sampling Frequency:44.1kHz

| (1) Stop MCKI |

Figure 57. Clock Stopping Sequence (5)

<Example>
   (1)  Stop MCKI. BCLK and LRCK are fixed to "H" or "L".

**■ Power down**

Power supply current is typ. 20μA by stopping clocks and setting PMVCM bit = "0" after all blocks except for VCOM are powered-down. Power supply current can be shut down (typ. 1μA) by stopping clocks and setting the PDN pin = "L". When the PDN pin = "L", the registers are initialized.

---
**PACKAGE**
---

# ● 24pin QFN (Unit: mm)
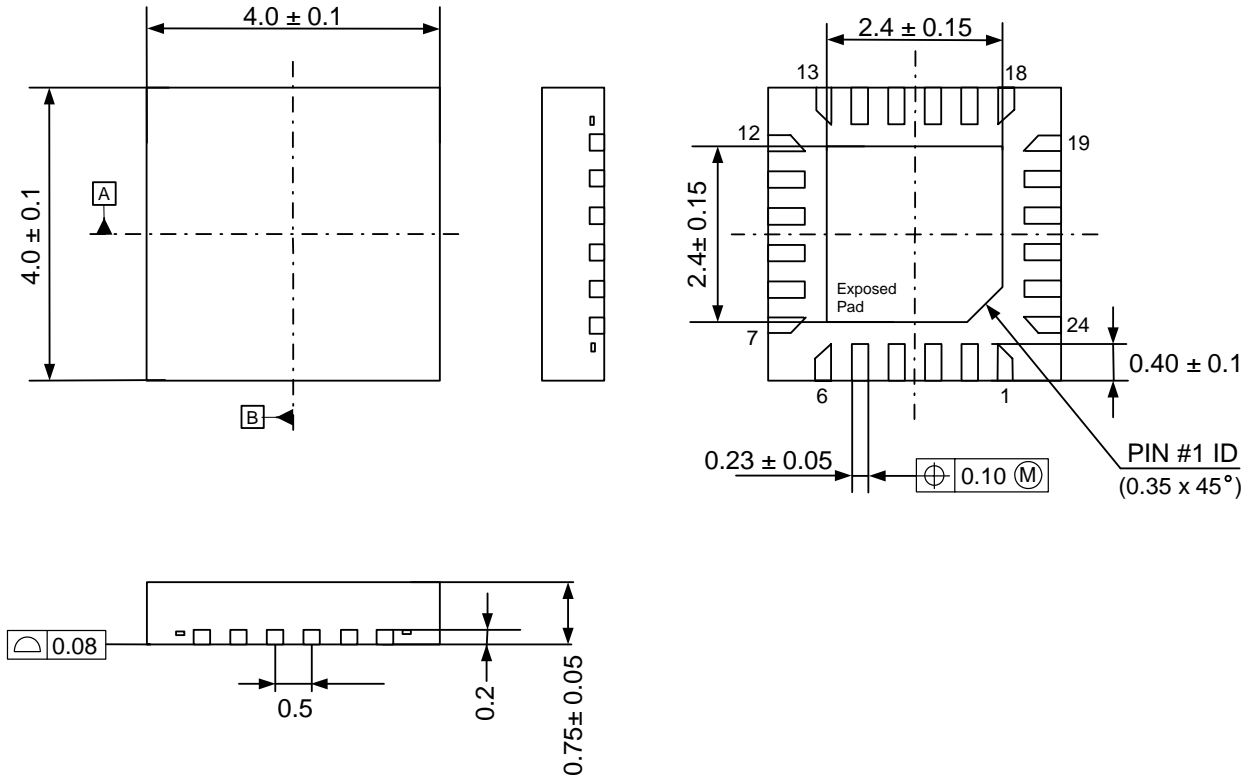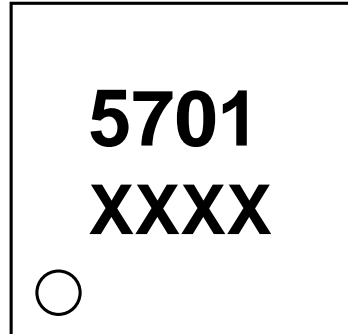
Note) The exposed pad on the bottom surface of the package must be open or connected to the ground.
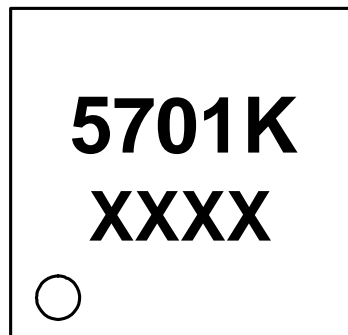
## ■ Material & Lead finish

| | |
|---|---|
| Package molding compound: | Epoxy |
| Lead frame material: | Cu |
| Lead frame surface treatment: | Solder (Pb free) plate |

| MARKING |
|---|

## AK5701VN

**5701**
**XXXX**

○
1

XXXX : Date code identifier (4 digits)

## AK5701KN

**5701K**
**XXXX**

○
1

XXXX : Date code identifier (4 digits)

## REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 05/08/04 | 00 | First Edition | | |
| 05/11/22 | 01 | Error correction | 8 | Switching Characteristics (PLL Slave Mode)<br>tBCKL(min): 240ns → 0.4 x tBCK<br>tBCKH(min): 240ns → 0.4 x tBCK |
| | | | 25 | PLL Slave Mode<br>a) Mode 1: EXBCLK or EXLRCK → MCKI<br>b) Mode 2: MCKI → EXBCLK or EXLRCK |
| | | | 35 | ALC Operation<br>The sentence of "The IVL and IVR are then set to the same value for both channels." was deleted. |
| | | | 57 | Control Sequence (MIC Recording)<br>Figure 51 (7) Data=01H → 04H<br>(2) 72H&73H → 12H&13H<br>(3) 7AH → 1AH<br>(4) 7BH → 1BH<br>(5) 7CH → 1CH |
| 07/08/30 | 02 | Product Addition | 1, 3, 5, 62 | AK5701KN was added.<br>(1) Ambient Temperature<br>AK5701VN : −30 ~ +85°C<br>AK5701KN : −40 ~ +85°C<br>(2) Marking<br>AK5701VN : "5701"<br>AK5701KN : "5701K" |
| | | Spec Addition | 11 | 1. Control Interface Timing(CSP pin = "L")<br>(1) CSN "↓" to CCLK "↑"<br>→ CSN Edge to CCLK "↑"<br>(2) CCLK "↑" to CSN "↑"<br>→ CCLK "↑" to CSN Edge<br>2. Control Interface Timing(CSP pin = "H")<br>(1) CSN "↑" to CCLK "↑"<br>→ CSN Edge to CCLK "↑"<br>(2) CCLK "↑" to CSN "↓"<br>→ CCLK "↑" to CSN Edge<br>3. Note 22 was added. |
| | | Error Correction | 30 | Figure 26 ~ Figure 29 :<br>ECTBCLK(32fs)/BCLK(32fs)<br>No of 1st bit in Fugure 15 → 31 |
| | | | 31 | Figure 30 ~ Figure 33 : BCLK(64fs)<br>No of 1st bit in Fugure : 15 → 31 |
| | | Spec Addition | 40 | Serial Control I/F<br>1. CSP pin = "L"<br>"CSN should be set to "H" once after 16 CCLKs for each address." was added.<br>2. CSP pin = "H"<br>"CSN should be set to "L" once after 16 CCLKs for each address." was added. |

**AKM**

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