AK4688

Asynchronous Stereo CODEC with Capless Line I/O

GENERAL DESCRIPTION

The AK4688 is a stereo audio CODEC. The integrated ADC and DAC interfaces accept up to 24-bit input/output data and support an asynchronous operation. The input range of the pre-amplifier, that supports line inputs, is adjustable by an external resistor. A ground referenced 2Vrms output with a 3.3V single power supply is achieved by an integrated charge pump, reducing external parts such as AC-coupling capacitors and mute circuits. The ADC block of the AK4688 achieves a dynamic range of 99dB, and the DAC block achieves a dynamic range of 105dB. The AK4688 is suitable for digital recording systems, digital TVs, Blu-ray recorders and Home theater systems.

FEATURES

- ☐ **Asynchronous ADC/DAC Operation**
- ☐ **Capless Stereo Pre-amplifier for Line Input/Output**
- ☐ **24bit Stereo ADC**
  - **- 64x Oversampling**
  - **- Sampling Rate up to 48kHz**
  - **- Linear Phase Digital Anti-Alias Filter**
  - **- S/(N+D): 83dB**
  - **- Dynamic Range, S/N: 99dB**
  - **- Digital HPF for Offset Cancellation**
- ☐ **24bit Stereo DAC**
  - **- 128x Oversampling**
  - **- Sampling Rate up to 192kHz**
  - **- 24bit 8 times Digital Filter**
  - **- S/(N+D): 95dB**
  - **- Dynamic Range, S/N: 105dB**
  - **- De-emphasis Filter**
- ☐ **High Jitter Tolerance**
- ☐ **External Master Clock Input:**
  - **256fs, 384fs, 512fs 768fs (fs=32kHz ~ 48kHz)**
  - **128fs, 192fs, 256fs 384fs (fs=64kHz ~ 96kHz)**
  - **128fs, 192fs (fs=128kHz ~ 192kHz)**
- ☐ **2 Audio Serial I/F (PORT1, PORT2)**
  - **- Master/Slave mode (PORT1)**
  - **- I/F format**
    - **PORT1, 2: MSB, LSB justified (16/24 bit), I^2S**
- ☐ **Hardware / I^2C-bus Control**
- ☐ **Operating Voltage:**
  - **- Digital I/O and Charge Pump: 3.0V ~ 3.6V**
  - **- ADC Analog: 3.0V ~ 3.6V**
  - **- DAC Analog: 3.0V ~ 3.6V**
- ☐ **Package: 36pin QFN**

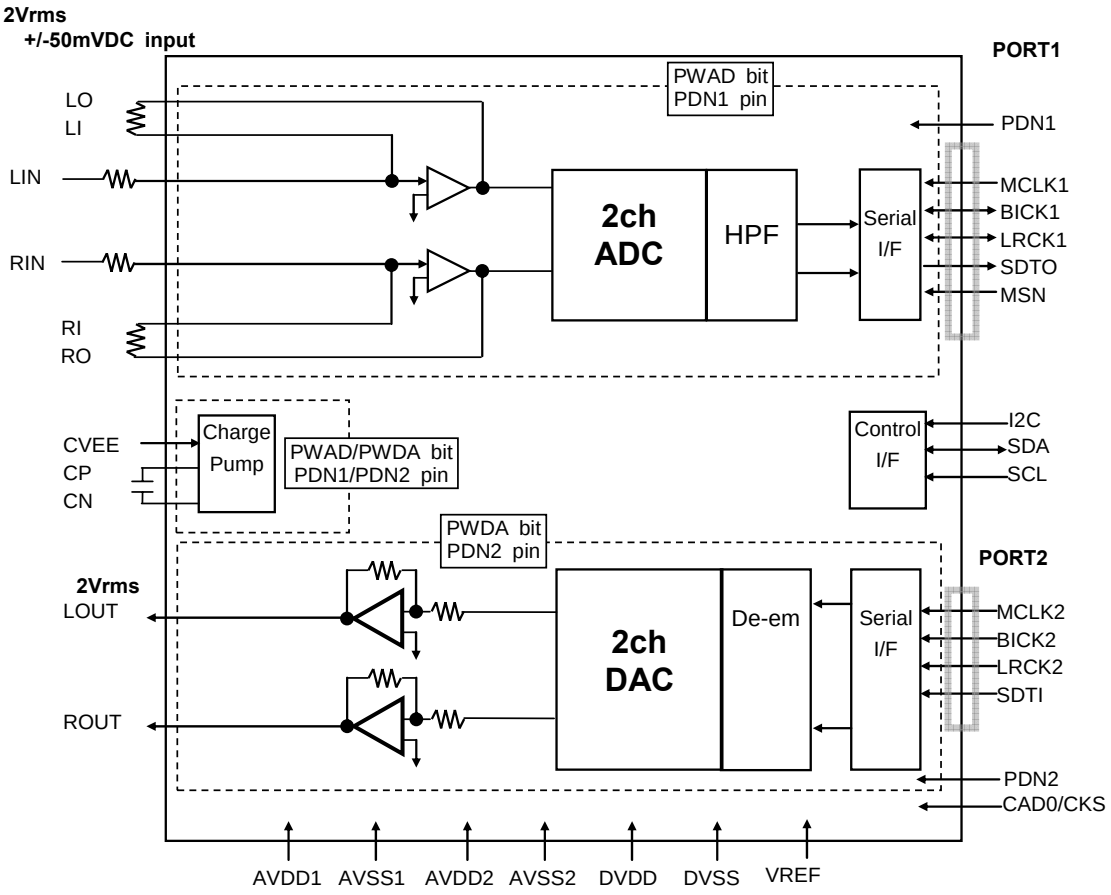


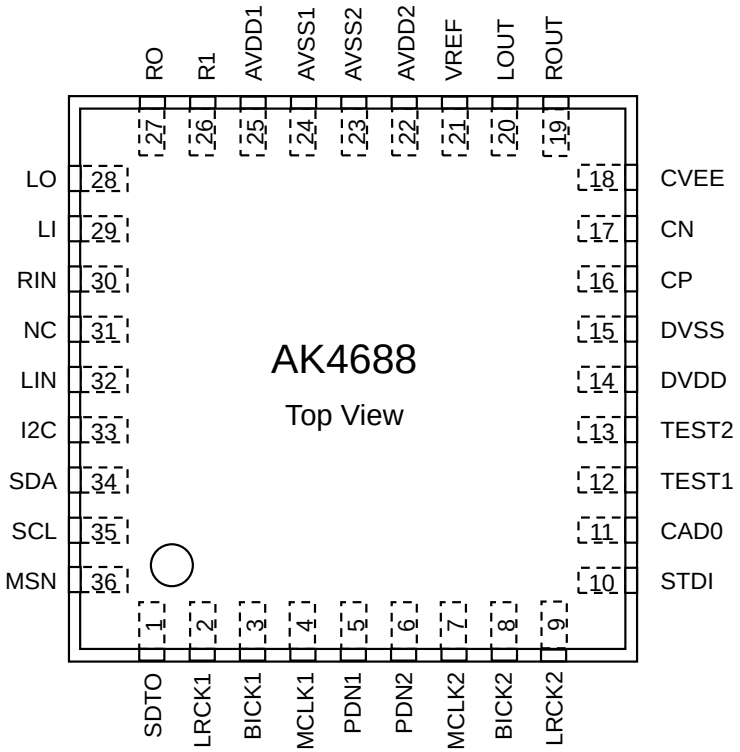
Figure 1. AK4688 Block Diagram

■ Ordering Guide

AK4688EN	-20 ~ +85°C	36pin QFN (0.5mm pitch)
AKD4688	Evaluation Board for the AK4688	

■ Pin Layout

36 pin QFN (0.5mm pitch)



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	SDTO	O	Audio Serial Data Output Pin (for PORT1)
2	LRCK1	I/O	Channel Clock Pin (for PORT1)
3	BICK1	I/O	Audio Serial Data Clock Pin (for PORT1)
4	MCLK1	I	ADC Master Clock Input Pin (for PORT1)
5	PDN1	I	Power-Down Mode for ADC When "L", the ADC is powered-down.
6	PDN2	I	Power-Down Mode for DAC When "L", the DAC is powered-down.
7	MCLK2	I	DAC Master Clock Input Pin (for PORT2)
8	BICK2	I	Audio Serial Data Clock Pin (for PORT2)
9	LRCK2	I	Input Channel Clock Pin (for PORT2)
10	SDTI	I	Audio Serial Data Input Pin (for PORT2)
11	CAD0	I	CAD Address Pin (I2C pin = "H")
	CKS	I	ADC MCLK Speed Select Pin (I2C pin = "L") "H": MCLK=768fs, "L": MCLK=256fs
12	TEST1	I	This pin must be connected to the ground
13	TEST2	I	This pin must be connected to the ground
14	DVDD	-	Digital Power Supply Pin, 3.0V~3.6V
15	DVSS	-	Digital Ground Pin, 0V
16	CP	I	Positive Charge Pump Capacitor Terminal Pin (for Analog Input/Output)
17	CN	I	Negative Charge Pump Capacitor Terminal Pin (for Analog Input/Output)
18	CVEE	O	Charge Pump Circuit Negative Voltage Output Pin (for Analog Input/Output)
19	ROUT	O	Rch Analog Output Pin
20	LOUT	O	Lch Analog Output Pin
21	VREF	O	Reference Output Pin Connect to AVSS2 with a 1μF low ESR capacitor over all temperatures.
22	AVDD2	-	DAC Analog Power Supply Pin, 3.3V~3.6V
23	AVSS2	-	ADC Analog Ground Pin, 0V
24	AVSS1	-	ADC Analog Ground Pin, 0V
25	AVDD1	-	ADC Analog Power Supply Pin, 3.0V~3.6V
26	RI	O	Rch Feedback Resistor Input Pin
27	RO	O	Rch Feedback Resistor Output Pin
28	LO	O	Lch Feedback Resistor Output Pin
29	LI	O	Lch Feedback Resistor Input Pin
30	RIN	I	Rch Input Pin
31	NC	-	This pin must be connected to the ground
32	LIN	I	Lch Input Pin
33	I2C	I	I^2C Pin "H"= I^2C control, "L"= H/W control
34	SDA	I/O	Control Data Pin (I2C pin = "H") When the I2C pin = "L" (H/W control), the SDA pin must be connected to DVSS.
35	SCL	I	Control Data Clock Pin (I2C pin = "H") When the I2C pin = "L" (H/W control), the SCL pin must be connected to DVSS.
36	MSN	I	PORT1 Master Mode Select Pin. "L"(connected to the ground): Slave mode. "H"(connected to DVDD) : Master mode.

Note: All digital input pins must not be allowed to float.

ABSOLUTE MAXIMUM RATINGS

(AVSS1=AVSS2=DVSS=0V; Note 1)

Parameter	Symbol	min	max	Unit
Power Supply	DVDD	-0.3	4.0	V
	AVDD1	-0.3	4.0	V
	AVDD2	-0.3	4.0	V
Input Current (any pins except for supplies)	IIN	-	±10	mA
Digital Input Voltage (MCLK1-2, PDN1-2, LRCK1-2, SDTI, BICK1-2, SDA, SCL, MSN, CAD0 pins)	VIND	-0.3	DVDD+0.3	V
Analog Input Voltage (LIN1-3, RIN1-3 pins)	VINA	-0.3	AVDD1+0.3	V
Ambient Operating Temperature	Ta	-20	85	°C
Storage Temperature	Tstg	-65	150	°C

Note 1. AVSS1, AVSS2 and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS1=AVSS2=DVSS= 0V; Note 1)

Parameter	Symbol	min	typ	max	Unit
Power Supply (Note 2)	DVDD	3.0	3.3	3.6	V
	AVDD1	3.0	3.3	3.6	V
	AVDD2	3.0	3.3	3.6	V

Note 2. The AVDD1 and AVDD2 must be the same voltage.
The voltage difference between DVDD and other voltages (AVDD1 and AVDD2) must be less than 0.3V.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD1=AVDD2 = DVDD= 3.3V; AVSS1=AVSS2=DVSS =0V; fs=48kHz; BICK=64fs;
Signal Frequency=1kHz; 24bit Data; Measurement Frequency = 20Hz~ 20kHz at fs=48kHz, 20Hz~40kHz at fs=96kHz;
20Hz~40kHz at fs=192kHz, all blocks are synchronized, unless otherwise specified)

Parameter		min	typ	max	Unit
Pre-Amp Characteristics:					
Feedback Resistance Rf		12	39	92	kΩ
Input Resistance Ri		18	47	92	kΩ
Output Level LO / RO pins (ADC=0dBFs) (Note 3)		1.82	1.91	2.00	Vrms
Load Resistance R_L (Note 4)		18			kΩ
Load Capacitance C_L (Note 4)				20	pF
Analog Input (LIN, RIN pin) to ADC Analog Input Characteristics					
Resolution				24	Bits
S/(N+D) (-1dBFS)	fs=48kHz	-	83		dB
DR (-60dBFS)	fs=48kHz, A-weighted	-	99		dB
S/N (input off)	fs=48kHz, A-weighted	-	99		dB
Interchannel Isolation (Note 5)		-	100		dB
Interchannel Gain Mismatch			0	-	dB
Gain Drift			50	-	ppm/°C
Power Supply Rejection (Note 6)			50		dB
DAC to Analog Output (LOUT, ROUT pin) Characteristics					
Resolution				24	Bits
S/(N+D) (0dBFS)	fs=48kHz	-	95		dB
	fs=96kHz	-	93		dB
	fs=192kHz	-	93		dB
DR (-60dBFS)	fs=48kHz, A-weighted	-	105		dB
	fs=96kHz, A-weighted	-	105		dB
	fs=192kHz, A-weighted	-	105		dB
S/N ("0" data)	fs=48kHz, A-weighted	-	105		dB
	fs=96kHz, A-weighted	-	105		dB
	fs=192kHz, A-weighted	-	105		dB
Interchannel Isolation		-	100		dB
Interchannel Gain Mismatch			0	-	dB
DC Offset (at output pin)		–5	0	+5	mV
Gain Drift			50	-	ppm/°C
Output Voltage	LOUT/ROUT= 2 x AVDD2/3.3	1.85	2	2.15	Vrms
Load Resistance		5			kΩ
Load Capacitance (C1)				30	pF
Power Supply Rejection (Note 6)			62		dB

Note 3. Input range for ADC full scale when the external input resistance is 47kΩ, feedback resistance is 39kΩ and input signal is 2.3Vrms.

Note 4. R_L or C_L of Figure 3. Load resistance and capacitance when the output signal of the LO/RO pin is used for an external device.

Note 5. This value is the channel isolation for all other channels between LIN and RIN.

Note 6. PSR is applied to AVDD1, AVDD2 and DVDD with 1kHz, 50mVpp.

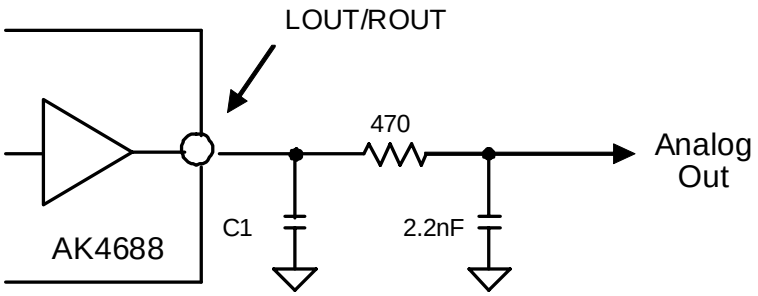


Figure 2. Lineout Circuit Example

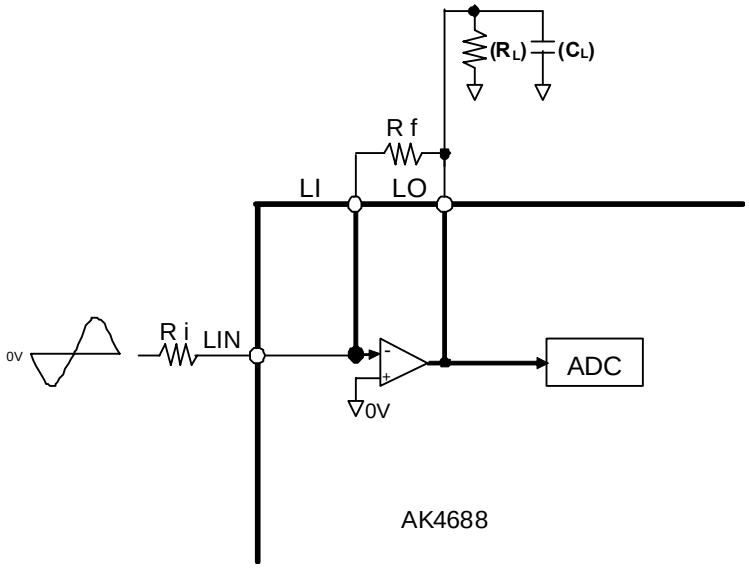


Figure 3. External Circuit of Pre-Amp

Power Supplies				
Parameter	**min**	**typ**	**max**	**Unit**
Power Supply Current				
Normal Operation (PDN1 pin = PDN2 pin = "H")				
AVVD1		3	-	mA
AVDD2		11	-	mA
DVDD		13	-	mA
DVDD+AVDD1+AVDD2		27	40	mA
Power-Down Mode (PDN1 pin = PDN2 pin = "L"; Note 7)				
DVDD+AVDD1+AVDD2		1	20	μA

Note 7. PDN1-2 and TEST1-2 pins are held at DVSS, and all digital inputs including clock pins (MCLK1-2, BICK1-2, LRCK1-2, SDTI, SDA, SCL, MSN and CAD0 pins) are held at DVDD or DVSS. However, the LRCK and BICK pins should be open since these pins become output state when the MSN pin is fixed to DVDD.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD1=AVDD2= DVDD= 3.3V; fs=48kHz)

Parameter		**Symbol**	**min**	**typ**	**max**	**Unit**
ADC Digital Filter (Decimation LPF):						
Passband (Note 8)	±0.1dB	PB	0		18.8	kHz
	-0.2dB		-	21.1	-	kHz
	-3.0dB		-	21.7	-	kHz
Stopband		SB	28.5			kHz
Stopband Attenuation		SA	73			dB
Group Delay (Note 10)		GD		17		1/fs
Group Delay Distortion		ΔGD		0		μs
ADC Digital Filter (HPF):						
Frequency Response (Note 8)	-3dB	FR		1.0		Hz
	-0.1dB			7.1		Hz
DAC Digital Filter:						
Passband ±0.05dB (Note 9)		PB	0		21.7	kHz
-6.0dB			-	24.0	-	kHz
Stopband (Note 9)		SB	26.3			kHz
Passband Ripple		PR			± 0.05	dB
Stopband Attenuation		SA	64			dB
Group Delay (Note 10)		GD	-	24	-	1/fs
De-emphasis Filter (DEM = ON)						
De-emphasis Error (DC Reference)	fs = 32kHz		-	-	–1.5/0	dB
	fs = 44.1kHz		-	-	–0.2/+0.2	dB
	fs = 48kHz		-	-	0/+0.6	dB
DAC Digital Filter + Analog Filter: (DEM = OFF)						
Frequency Response	20.0kHz fs=44.1kHz	FR	-	± 0.2	-	dB
	40.0kHz fs=96kHz	FR	-	± 0.3	-	dB
	80.0kHz fs=192kHz	FR	-	± 1.0	-	dB

Note 8. The passband and stopband frequencies scale with fs.
For example, 21.8kHz at –0.1dB is 0.454 x fs (DAC). The reference frequency of these responses is 1kHz.

Note 9. The passband and stopband frequencies scale with fs (system sampling rate).
For example, PB=0.4535×fs(@±0.05dB), SB=0.546×fs.

Note 10. The calculating delay time occurred by digital filtering. This time is from an input of the analog signal until 24bit data of both channels is set into the output register of PORT1. For DAC, this time is from setting 16/24bit data of both channels into the input register of PORT2 until an analog signal is output.

DC CHARACTERISTICS

(Ta= 25°C; AVDD1=AVDD2= DVDD= 3.3V)

Parameter	Symbol	min	typ	max	Unit
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=-400μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout= -400μA(except SDA pin), 3mA(SDA pin))	VOL	-		0.4	V
Input Leakage Current	Iin	-	-	±10	μA

SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD1=AVDD2 =DVDD= 3.3V; C_L= 20pF (except for SDA pin), Cb=400pF(SDA pin))

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Frequency	fECLK	8.192		36.864	MHz
Duty	dECLK	40	50	60	%
Master Clock					
256fsn, 128fsd:	fCLK	8.192		12.288	MHz
Pulse Width Low	tCLKL	0.37			1/fCLK
Pulse Width High	tCLKH	0.37			1/fCLK
384fsn, 192fsd:	fCLK	12.288		18.432	MHz
Pulse Width Low	tCLKL	0.37			1/fCLK
Pulse Width High	tCLKH	0.37			1/fCLK
512fsn, 256fsd, 128fsq:	fCLK	16.384		24.576	MHz
Pulse Width Low	tCLKL	0.37			1/fCLK
Pulse Width High	tCLKH	0.37			1/fCLK
768fsn, 384fsd, 192fsq:	fCLK	24.576		36.864	MHz
Pulse Width Low	tCLKL	0.37			1/fCLK
Pulse Width High	tCLKH	0.37			1/fCLK
LRCK1Timing (Slave Mode)					
	fsn	32		48	kHz
Duty Cycle	Duty	45		55	%
LRCK2Timing (Slave Mode)					
Normal Speed Mode	fsn	32		48	kHz
Double Speed Mode	fsd	32		96	kHz
Quad Speed Mode	fsq	128		192	kHz
Duty Cycle	Duty	45		55	%
LRCK1 Timing (Master Mode)					
Normal Speed Mode	fsn	32		48	kHz
Duty Cycle	Duty		50		%
Power-down & Reset Timing					
PDN Pulse Width (Note 11)	tPD	150			ns
PDN "↑" to SDTO valid (Note 12)	tPDV		2640		1/fs

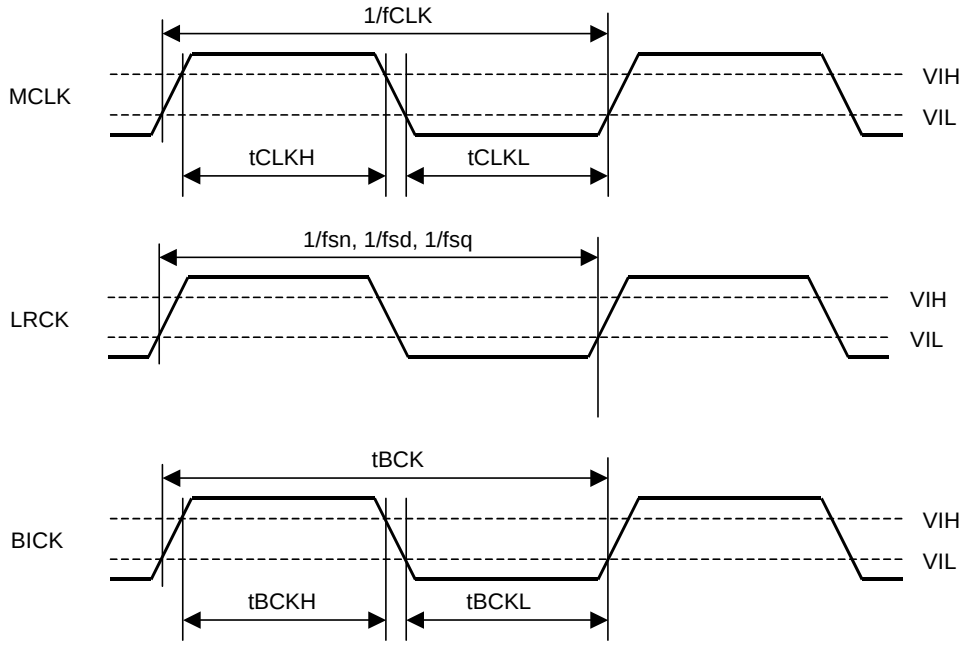
Note 11. Refer to the "■ System Reset" paragraph for the reset by PDN1 and PDN2 pins.

Note 12. After a rising edge of PDN1, the internal counter starts by divided clock of MCLK and ADC power down is released by a falling edge of CVEE after 64/fs on LRCK, then SDTIO is output 528/fs later.

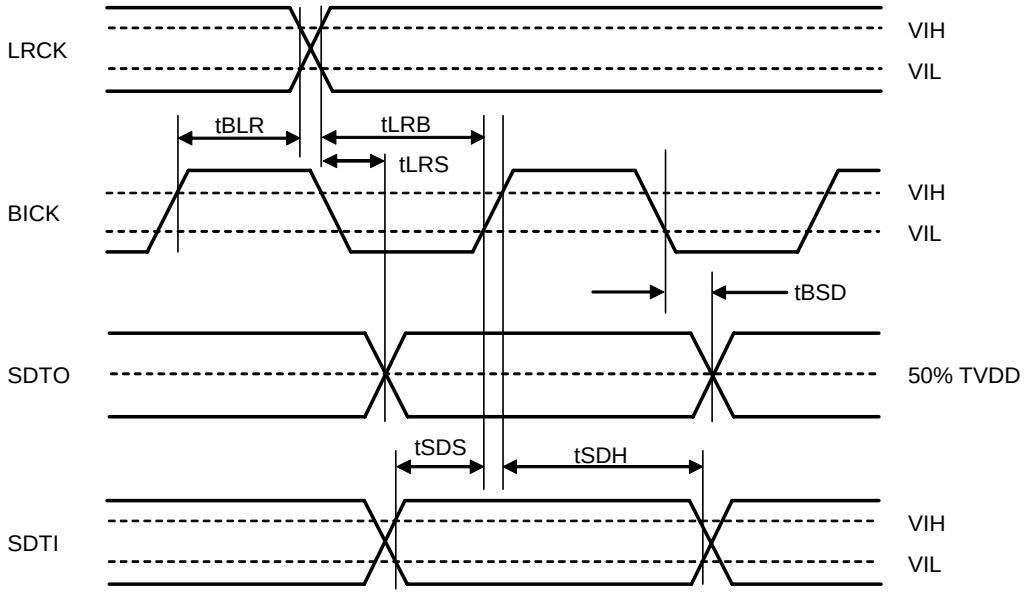
Parameter	Symbol	min	typ	max	Unit
Audio Interface Timing (Slave Mode)					
PORT2(DAC)					
BICK2 Period	tBCK	81			ns
BICK2 Pulse Width Low	tBCKL	20			ns
Pulse Width High	tBCKH	20			ns
LRCK2 Edge to BICK2 "↑" (Note 13)	tLRB	20			ns
BICK2 "↑" to LRCK2 Edge (Note 13)	tBLR	20			ns
SDTI Hold Time	tSDH	10			ns
SDTI Setup Time	tSDS	10			ns
PORT1 (ADC)					
BICK1 Period	tBCK	324			ns
BICK1 Pulse Width Low	tBCKL	128			ns
Pulse Width High	tBCKH	128			ns
LRCK1 Edge to BICK1 "↑" (Note 13)	tLRB	80			ns
BICK1 "↑" to LRCK1 Edge (Note 13)	tBLR	80			ns
LRCK1 to SDTO (MSB)	tLRS			80	ns
BICK1 "↓" to SDTO	tBSD			80	ns
Audio Interface Timing (Master Mode)					
BICK1 Frequency	fBCK		64fs		Hz
BICK1 Duty	dBCK		50		%
BICK1 "↓" to LRCK1 Edge	tMBLR	-20		20	ns
BICK1 "↓" to SDTO	tBSD			20	ns
Control Interface Timing (I^2C Bus):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 14)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	-		50	ns
Capacitive load on bus	Cb	0		400	pF

Note 13. BICK rising edge must not occur at the same time as LRCK edge.
Note 14. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.
Note 15. I^2C-bus is a trademark of NXP B.V.

■ Timing Diagram

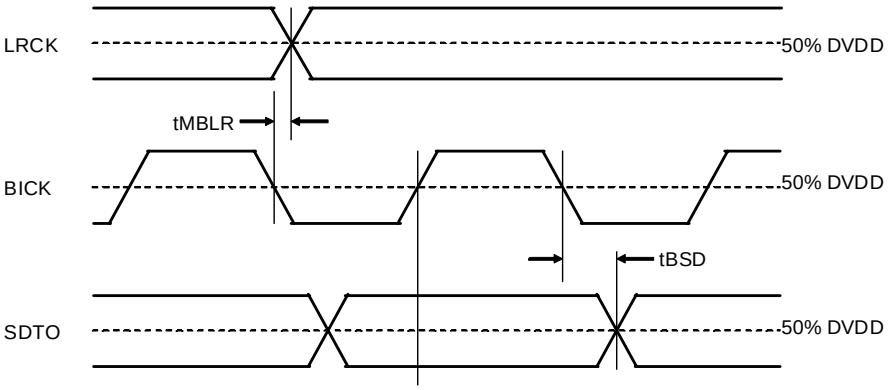


Clock Timing (Normal mode)

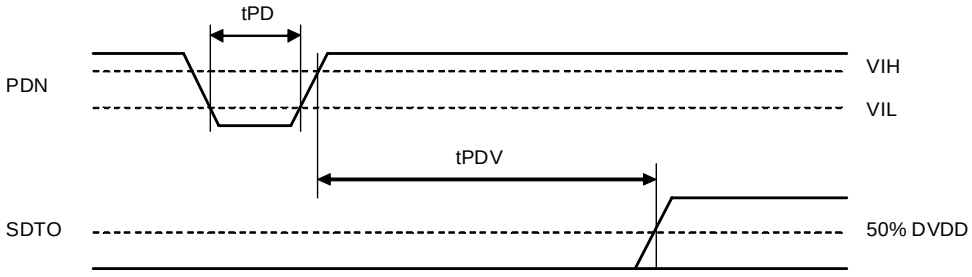


Audio Interface Timing

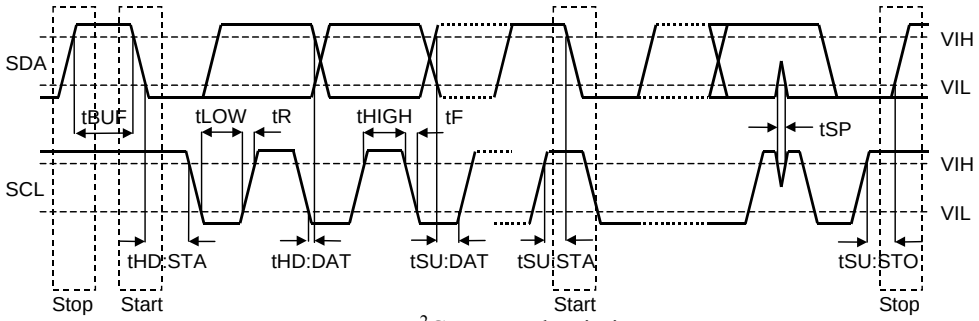
LRCK= LRCK1, LRCK2
BICK= BICK1, BICK2



Audio Interface timing (Master Mode)



Power Down & Reset Timing



I^{2}C Bus mode Timing

OPERATION OVERVIEW

■ System Clock

The AK4688 has two audio serial interfaces (PORT1 and PORT2) which can be operated asynchronously. The PORT2 is the audio data interface for DAC, and the PORT1 is for ADC. At each PORT, the external clocks, which are required to operate the AK4688 in slave mode, are MCLK1 (MCLK2), LRCK1 (LRCK2) and BICK1 (BICK2). The MCLK1 (MCKK2) must be synchronized with LRCK1 (LRCK2) but the phase is not critical.

The AK4688 has independent power-down function for ADC and DAC controlled by the PDN1 and PDN2 pins (or PWAD and PWDA bits). In I^2C control mode, the AK4688 is in normal operation when PDN1pin=PDN2 pin= "H" and PWAD bit = PWDA bit = "1" (Table 1, Table 3). In H/W control mode (Table 2, Table 4), the AK4688 is in normal operation when PDN1 pin = PDN2 pin = "H". The AK4688 is automatically powered down when MCLK1 clock is stopped in master mode (MSN pin = "H"), or when MCLK1 (MCLK2), LRCK1 (LRCK2) and BICK1 (BICK2) are stopped in slave mode (MSN pin = "L"). In this case, the ADC output is "0" data and DAC output is pulled down to VSS. The power-down state is released and the AK4688 starts operation when MCLK1 is input in master mode (MSN pin = "H"), or when MCLK1 (MCLK2), LRCK1 (LRCK2) and BICK1 (BICK2) are input in slave mode (MSN pin = "L").

When the reset is released (PDN1/2 pin = "L" → "H"), such as after power up the device, the ADC/DAC of AK4688 is in power-down state until MCLK1/2, LRCK1/2 and BICK1/2 are input.

PDN1 pin	PWAD bit	Master mode: MCLK1 Slave mode: MCLK1,LRCK1 and BICK1	ADC stauts	ADC OUT
L	×	×	Power down	0
H	0	×	Power down	0
H	1	Non-active	Power down	0
H	1	active	Power up	ADC output

(×: Don't Care)

Table 1. System CLOCK for ADC (I^2C Control Mode, PORT1)

PDN1 pin	Master mode: MCLK1 Slave mode: MCLK1,LRCK1 and BICK1	ADC stauts	ADC OUT
L	×	Power down	0
H	Non-active	Power down	0
H	active	Power up	ADC output

(×: Don't Care)

Table 2. System CLOCK for ADC (H/W Control Mode, PORT1)

PDN2 pin	PWDA bit	MCLK2,LRCK2 and BICK2	DAC stauts	DAC OUT
L	×	×	Power down	VSS
H	0	×	Power down	VSS
H	1	Non-active	Power down	VSS
H	1	active	Power up	DAC output

(×: Don't Care)

Table 3. System CLOCK for DAC (I^2C Control Mode, PORT2)

PDN2 pin	MCLK2,LRCK2 and BICK2	DAC stauts	DAC OUT
L	×	Power down	VSS
H	Non-active	Power down	VSS
H	active	Power up	DAC output

(×: Don't Care)

Table 4. System CLOCK for DAC (H/W Control Mode, PORT2)

■ Master/Slave Mode

The MSN pin controls master/slave mode of the PORT1. The PORT2 supports slave mode only. In master mode, LRCK1 and BICK1 pins are output pins. In slave mode, LRCK1 (LRCK2) and BICK1 (BICK2) pins are input pins (Table 5).

MSN pin	PORT1 (ADC) BICK1, LRCK1	PORT2 (DAC) BICK2, LRCK2
L	Input (slave mode)	Input (slave mode)
H	Output "L"(master mode)	Input (slave mode)

Table 5. Master/Salve Mode

■ PORT1 (ADC) Clock Control

In master mode (MSN pin = "H"), the required clock is MCLK1. The CKS1-0 bits and the CKS pin select the clock frequency (Table 6, Table 7). The ADC is in power-down state until MCLK1, BICK1 and LRCK1 are supplied.

CKS1 bit	CKS0 bit	Clock Speed
0	0	256fs
0	1	384fs
1	0	512fs
1	1	768fs (default)

Table 6. PORT1(ADC) Master Clock Control (Master Mode, I²C Control Mode)

CKS pin	Clock Speed
L	256fs
H	768fs

Table 7. PORT1(ADC) Master Clock Control (Master Mode, H/W Control Mode)

In slave mode (MSN pin = "L"), required clocks are MCLK1, BICK1 and LRCK1. The master clock (MCLK1) must be synchronized with LRCK1 but the phase is not critical. After exiting reset following a power-up (PDN1 pin = "L" → "H"), the ADC of AK4688 is in power-down state until MCLK1, LRCK1 and BICK1 are input.

The ADC only supports Normal Speed Mode (fs = 32k ~ 48kHz).

LRCK1	MCLK1 (MHz)				BICK1 (MHz)
Fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920	12.2880	16.3840	24.5760	2.0480
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 8. PORT1(ADC) System Clock Example

■ PORT2 (DAC) Clock Control

External clocks (MCLK2, BICK2 and LRCK2) must always be present whenever the DAC is in normal operation (PDN pin = "H" or PWDA2 bit= "1"). The master clock (MCLK2) must be synchronized with LRCK2 but the phase is not critical. MCLK2 clock is used for interpolation filter and delta sigma modulator. During operation, DAC is automatically reset and the analog output goes to 0V (typ) if MCLK2, LRCK2 and BICK2 are stopped. This reset is released, and the DAC starts operation when MCLK2, LRCK2 and BICK2 are input again. The DAC is in power-down mode until MCLK2, BICK2 and LRCK2 are supplied.

There are two modes for controlling the sampling speed of DAC. One is the Manual Setting Mode (ACKS bit = "0") using the DFS1-0 bits, and the other is Auto Setting Mode (ACKS bit = "1").

1. Manual Setting Mode (ACKS bit = "0")

When the ACKS bit = "0", DAC is in Manual Setting Mode and the sampling speed is selected by DFS1-0 bits (Table 9).

DFS1 bit	DFS0 bit	DAC Sampling Speed (fs)		
0	0	Normal Speed Mode	32kHz~48kHz	(default)
0	1	Double Speed Mode	64kHz~96kHz	
1	0	Quad Speed Mode	128kHz~192kHz	
1	1	Not Available	-	

Table 9. PORT2(DAC) Sampling Speed (ACKS bit = "0", Manual Setting Mode)

LRCK2	MCLK2 (MHz)				BICK2 (MHz)
Fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920	12.2880	16.3840	24.5760	2.0480
44.1kHz	11.2896	16.9344	22.5792	33.8688	2.8224
48.0kHz	12.2880	18.4320	24.5760	36.8640	3.0720

Table 10. PORT2(DAC) system Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK2	MCLK2 (MHz)				BICK2 (MHz)
Fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896	16.9344	22.5792	33.8688	5.6448
96.0kHz	12.2880	18.4320	24.5760	36.8640	6.1440

Table 11. PORT2(DAC)system Clock Example(Double Speed Mode @Manual Setting Mode)

LRCK2	MCLK2 (MHz)				BICK2 (MHz)
Fs	128fs	192fs	256fs	384fs	64fs
176.4kHz	22.5792	33.8688	-	-	11.2896
192.0kHz	24.5760	36.8640	-	-	12.2880

Table 12. PORT2(DAC) system Clock Example (Quad Speed Mode @Manual Setting Mode)

2. Auto Setting Mode (ACKS bit = "1")

When the ACKS bit = "1", DAC is in Auto Setting Mode and the sampling speed is selected automatically by the ratio of MCLK2/LRCK2, as shown in Table 13 and Table 14. In this mode, the settings of DFS1-0 bits are ignored.

MCLK2	DAC Sampling Speed (fs) LRCK2	
512fs, 768fs	Normal Speed Mode	32kHz~48kHz
256fs, 384fs	Double Speed Mode	64kHz~96kHz
128fs, 192fs	Quad Speed Mode	128kHz~192kHz

Table 13. PORT2(DAC) Sampling Speed (ACKS bit = "1", Auto Setting Mode)

LRCK	MCLK (MHz)							Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	1152fs	
32.0kHz	-	-	-	-	16.3840	24.5760	36.8640	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	-	
48.0kHz	-	-	-	-	24.5760	36.8640	-	
32.0kHz			8.192	12.288				Double
44.1kHz			11.2896	16.9344				
48.0kHz			12.288	18.432				
88.2kHz	-	-	22.5792	33.8688	-	-	-	
96.0kHz	-	-	24.5760	36.8640	-	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	-	

Table 14. System Clock Example

When MCLK= 256fs/384fs, the AK4688 supports sampling rate of 32kHz~96kHz (Table 15). However, when the sampling rate is 32kHz~48kHz, DR and S/N will degrade as compared to when MCLK= 512fs/768fs.

MCLK	DR, S/N
256fs/384fs	102dB
512fs/768fs	105dB

Table 15. MCLK Frequency and DR, S/N (fs = 48kHz)

■ De-emphasis Filter

The DAC of AK4688 includes a digital de-emphasis filter (tc=50/15μs) by IIR filter. Setting the DEM1 bit to "1" enables the de-emphasis filter. Refer to "FILTER CHARACTERISTICS" about the gain error when this filter is ON. The de-emphasis filter is OFF in double speed mode (MCLK2= 256fs/38fs) and quad speed mode (MCLK2=128fs/192fs). The filter setting is executed in I^2C control mode and DEM bit controls ON/OFF of the filter. (Table 16)

DEM bit	De-emphasis Filter	
1	ON	
0	OFF	(default)

Table 16. De-emphasis Control (Normal Speed Mode)

■ Digital High Pass Filter

The ADC has a digital high pass filter for DC offset cancellation. The cut-off frequency of the HPF is 1.0Hz at fs=48kHz and frequency response scales with sampling rate (fs).

■ Audio Serial Interface Format

Each PORT1/2 can select audio interface format independently. The DIF1 bit controls audio data format of the PORT1. The DIF21-20 bits control the audio data format of the PORT2. In all modes the serial data is MSB-first, 2's complement format. The SDTO pin is clocked out on the falling edge of BICK1 and the SDTI pin is latched on the rising edge of BICK2. SDTI input formats can be used for 16-24bit data by zeroing the unused LSBs.

1. PORT1 (ADC) Setting

The MSN pin and DIF1 bit select following four serial data formats (Table 17).

Mode	MSN pin	DIF1 bit	SDTO	LRCK1		BICK1		
				L/R	I/O	speed	I/O	
0	L	0	24/16bit Left Justified	H/L	I	≥ 48fs or 32fs	I	(default)
1	L	1	24bit, I^2S	L/H	I	≥ 48fs	I	
2	H	0	24bit Left Justified	H/L	O	64fs	O	(default)
3	H	1	24bit, I^2S	L/H	O	64fs	O	

Table 17. Audio Interface Format (ADC)

2. PORT2 (DAC) Setting

The DIF21-20 bits select following four serial data formats (Table 18).

Mode	DIF21 bit	DIF20 bit	SDTI	LRCK2		BICK2		
				L/R	I/O	speed	I/O	
0	0	0	16bit, Right justified	H/L	I	≥ 32fs	I	
1	0	1	24bit, Right justified	H/L	I	≥ 48fs	I	
2	1	0	24bit, Left justified	H/L	I	≥ 48fs	I	(default)
3	1	1	24bit, I^2S	L/H	I	≥ 48fs	I	

Table 18. Audio Interface Format (DAC)

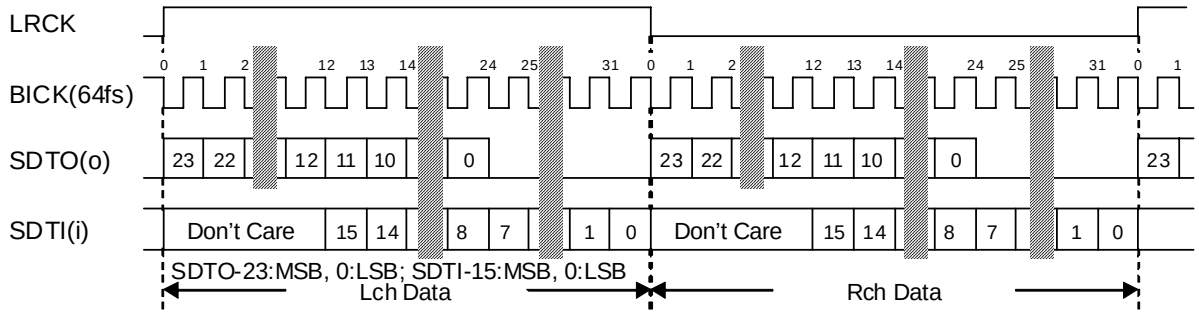


Figure 4. PORT1= Mode0/2, PORT2=Mode0 Timing

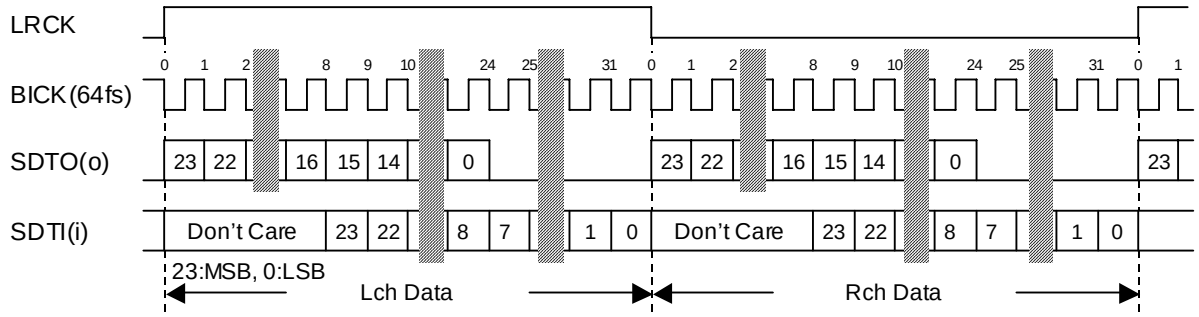


Figure 5. PORT1= Mode0/2, PORT2=Mode1 Timing

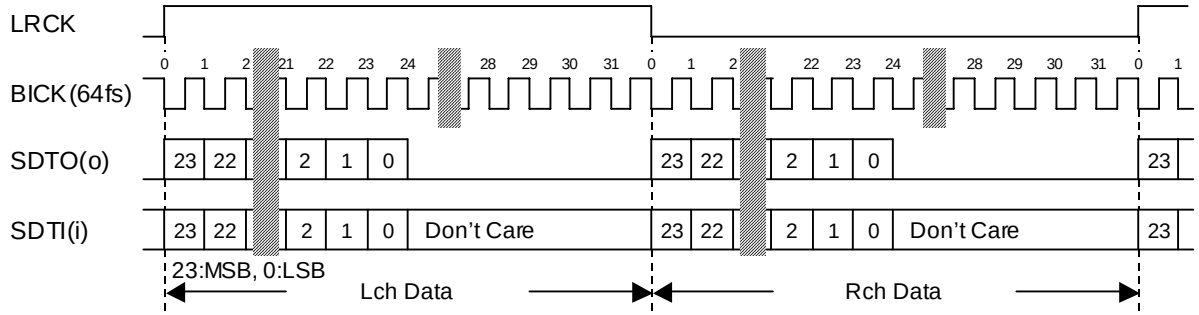


Figure 6. PORT1= Mode0/2, PORT2=Mode2 Timing

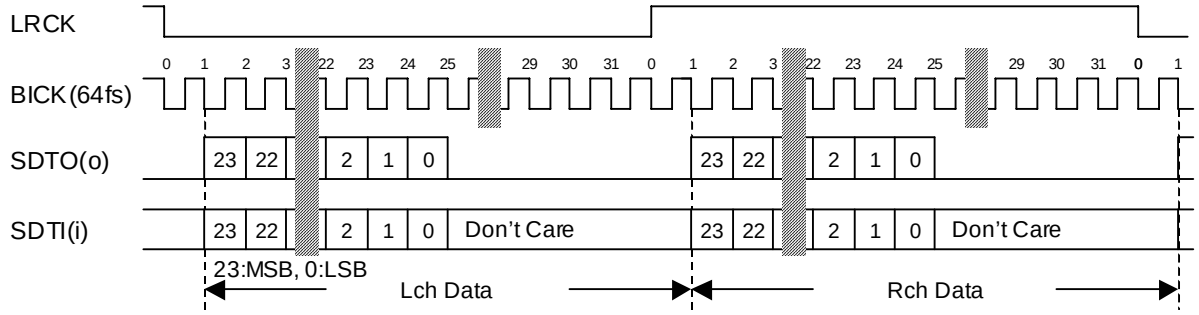


Figure 7. PORT1= Mode1/3, PORT2=Mode3 Timing

■ Pre-Amp and Input ATT

The input attenuation circuit is constructed by connecting input resistors (Ri) to LIN/RIN pin and feedback resistors (Rf) between LI/RI pin and LO/RO pin (Figure 8). The input voltage tolerance of the LO/RO pin is typically 1.91Vrms. Therefore, excessive inputs such as 2Vrms or 4Vrms to the LIN/RIN pin via Ri resistors must be attenuated to 1.91Vrms by these Ri and Rf resistors. Table 19 shows resistance examples of Ri and Rf.

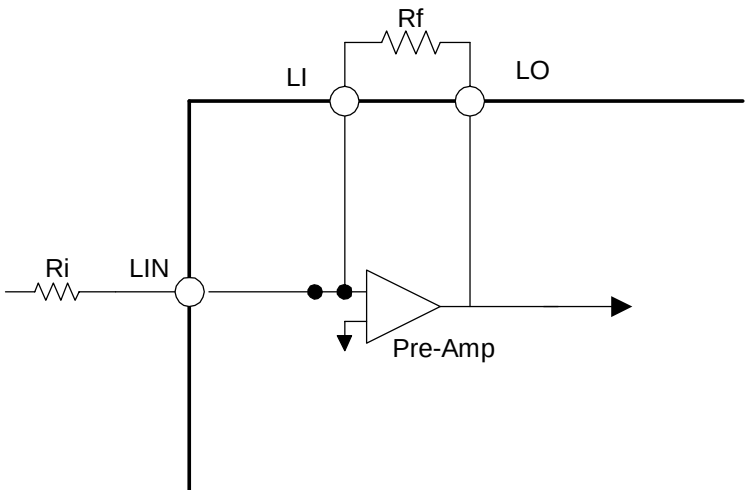


Figure 8. Pre-Amp and Input ATT

Input Range	Ri (kΩ)	Rf (kΩ)	ATT Gain (dB)	LO/RO pin	ADC output (typ)
4Vrms	47	20	-7.42	1.70Vrms	-1.0dBFS
2.2Vrms	47	39	-1.62	1.82Vrms	-0.39dBFS
1Vrms	47	82	+4.83	1.74Vrms	-0.78dBFS

Table 19. Input ATT example

■ Charge Pump Circuit

The internal charge pump circuit generates negative voltage (CVEE) from CVDD voltage for analog input and output.

The power up time of charge pump circuit is 1.3ms@48kHz. When PWAD and PWDA bits = "1", the ADC and DAC are powered-up after the charge pump circuit is powered-up.

The power-up conditions of the charge pump circuit are:

I^2C Control Mode
- PDN1 pin = "H", PWAD bit = "1" and MCLK1, LRCK1 and BICK1 (MCLK1 only in master mode) are input.
- PDN2 pin = "H", PWDA bit = "1" and MCLK2, LRCK2 and BICK2 are input.

H/W Control Mode
- PDN1 pin = "H" and MCLK1, LRCK1 and BICK1 (MCK1 only in master mode) are input.
- PDN2 pin = "H" and MCLK2, LRCK2 and BICK2 are input.

PDN1 pin	PWAD bit	Master mode: MCLK1 Slave mode: MCLK1,LRCK1, BICK1	PDN2 pin	PWDA bit	MCLK2, BICK2, LRCK2	CP status
H	1	active	×	×	×	ON
x	x	×	H	1	active	ON

(×: Don't Care)

Table 20. Charge Pump Power ON Conditions (I^2C Control Mode)

PDN1 pin	Master mode: MCLK1 Slave mode: MCLK1, LRCK1, BICK1	PDN2 pin	MCLK2, BICK2, LRCK2	CP status
H	Active	×	×	ON
x	×	H	active	ON

(×: Don't Care)

Table 21. Charge Pump Power ON Conditions (H/W Control Mode)

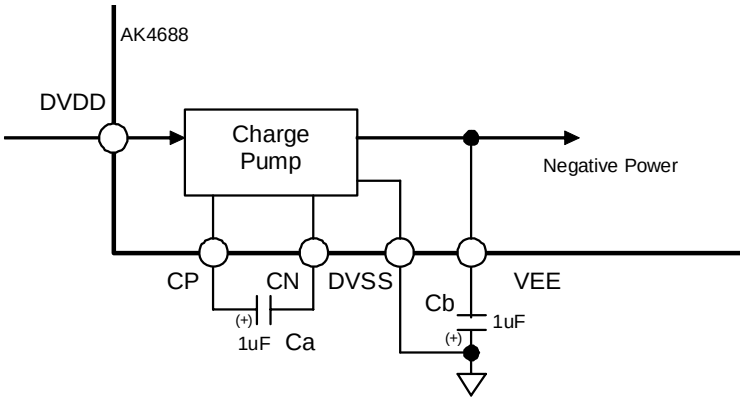


Figure 9. Charge Pump Circuit

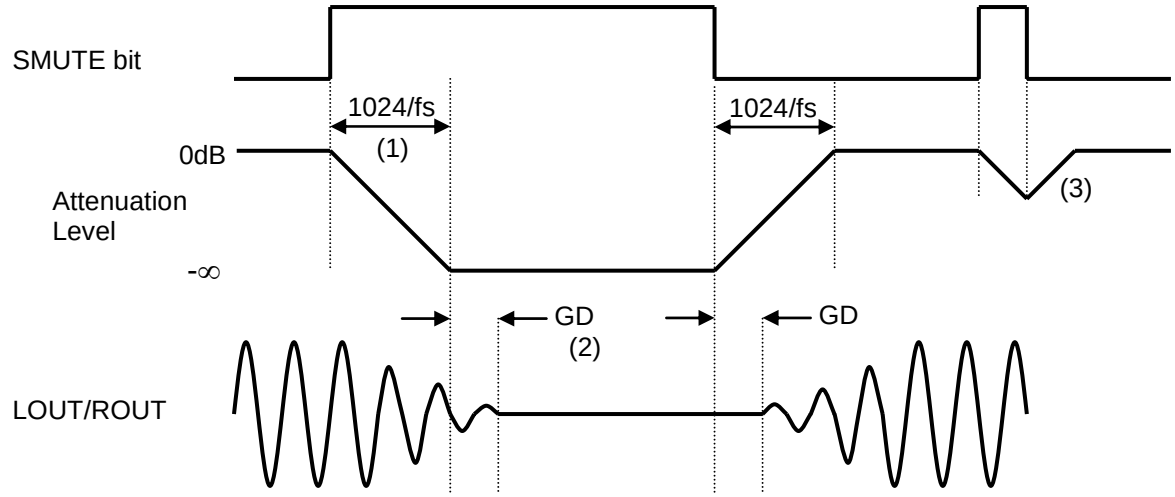
Note: Connect a 1μF low ESR capacitor between CP and CN pins, and between DVSS and VEE pins.

■ Analog Input/Output (LIN/RIN, LOUT/ROUT pins)

Power supply voltage for analog input/output is applied from a regulator for positive power and a charge-pump for negative power. The analog output is single-ended and centered on 0V (AVSS2). Therefore, a capacitor for AC-coupling can be removed. The minimum load resistance is 5kΩ. When the DAC input signal level is 0dBFS, the output voltage is 2Vrms.

■ Soft Mute

The DAC has a soft mute function. The soft mute operation is performed at digital domain. When the SMUTE bit goes to "1", the input data is attenuated by -∞ in 1024LRCK cycle. When the SMUTE bit returns to "0", the mute is cancelled and the attenuation level gradually changes to 0dB in 1024 LRCK cycle. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the attenuation level returns to 0dB in the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) In normal speed mode, the input data is attenuated to -∞ in 1024LRCK cycle. This time is 2048LRCK cycles (2048/fs) in Double Speed Mode, and 4096LRCK cycle (4096/fs) in Quad Speed Mode.

(2) The analog output corresponding to the digital input has group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and the attenuation level returns to 0dB in the same cycle.

Figure 10. Soft Mute Function

■ System Reset

When power-up the AK4688, the PDN1 and PDN2 pins should be "L" and changed to "H" after all power supplies (DVDD, AVDD1, and AVDD2) are supplied. After this reset is released (PDN1 and PDN2 pins = "L" → "H"), all blocks are in power-down mode. This ensures that all internal registers are reset to their initial values. ADC internal circuit, control registers for ADC (Addr: 01h-02h) and PWAD bit are reset by PDN1 pin = "L". DAC internal circuit, control registers for DAC (Addr: 03h) and PWDA bit are reset by the PDN2 pin = "L". When both PDN1 and PDN2 pins are "L", all blocks, registers and charge pump are powered-down. In H/W control mode, register settings are ignored, and the power-down control by PDN1 and PDN2 pins are available.

■ Power ON/OFF Sequence

The ADC and DAC blocks of the AK4688 are placed in power-down mode by bringing the PDN1 pin and PDN2 pin to "L" respectively and both digital filters are reset at the same time. The PDN1 pin = PDN2 pin ="L" also reset the control registers to their default values. In power-down mode, the DAC outputs 0V and the SDTO pin goes to "L". This reset must always be executed after power-up.
In master mode, the ADC starts operation on the rising edge of MLCK1 after power-down mode is released by a status change of the PDN1 pin from "L" to "H". In slave mode, when power down mode is released by a status change of the PDN1 pin from "L" to "H", the ADC starts operation on the rising edge of LRCK1 following MLCK1, LRCK1 and BICK1 inputs.
The DAC starts operation on the rising of the LRCK2, after power-down mode is released by a status change of the PDN2 pin from "L" to "H", and MCLK2, LRCK2 and BICK2 are input.

The analog initialization cycle of ADC starts after exiting the power-down mode. Therefore, the output data, SDTO becomes available after 2640 cycles of LRCK1 clock. In case of the DAC, an analog initialization cycle starts after exiting the power-down mode. The analog outputs are 0V during the initialization. Figure 11 shows power-down and power-up sequence.

The ADC and DAC can be powered-down individually by PWAD and PWDA bits. Register values are not initialized by these bits. When PWAD bit = "0", the ADC output goes to "L". When PWDA bit = "0", the DAC output goes to 0V.

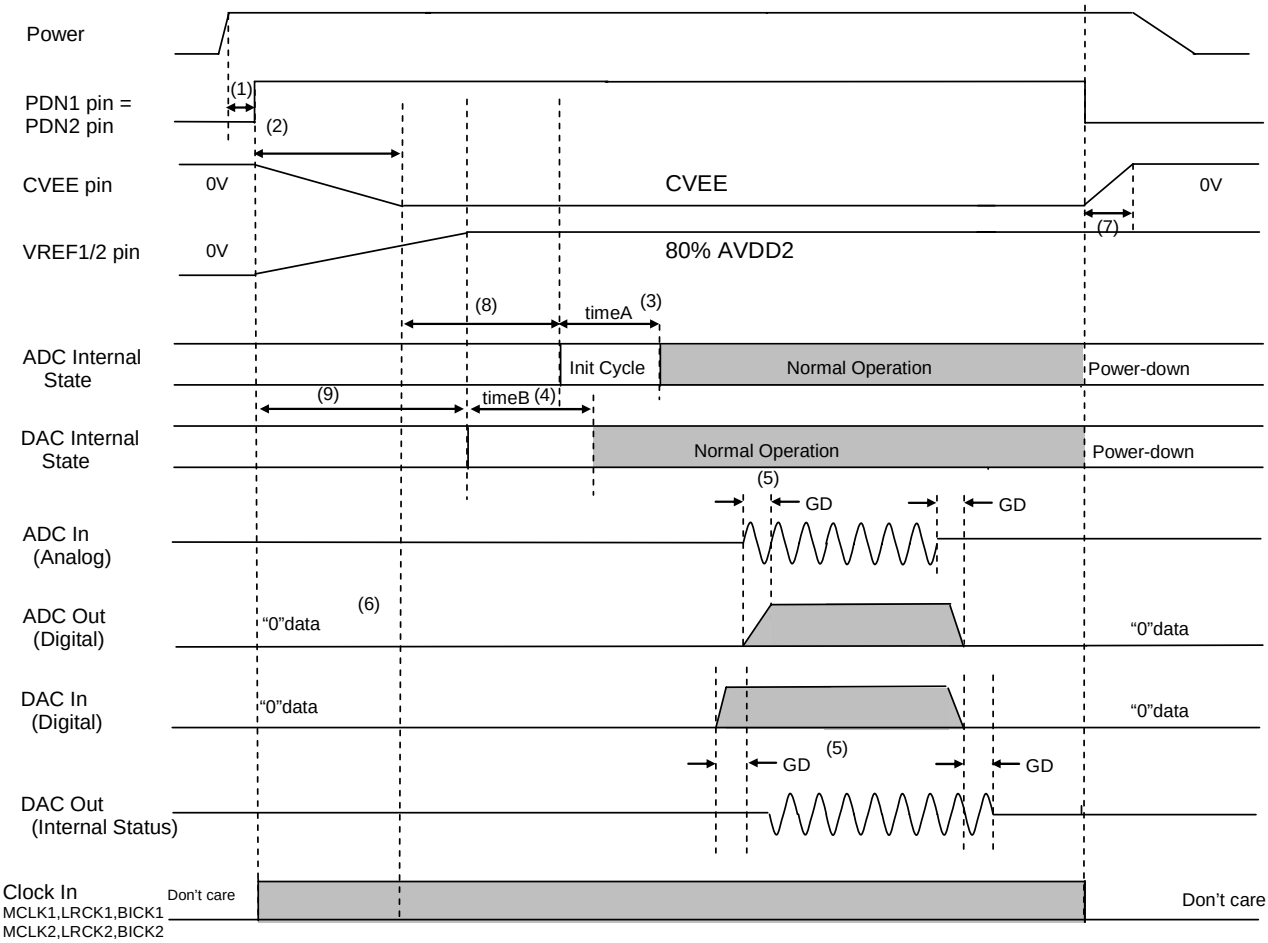


Figure 11. Power-up/down sequence example

Notes:

(1) The PDN1 and PDN2 pins should be changed from “L” to “H” after power up.
“L” time of 150ns or more is needed to reset the AK4688. The PDN pins must be held to “L” until all power supply pins are fed. After all powers are risen up, the PDN1 and PDN2 pins should be set to “H”.

(2) Charge Pump Circuit Power-up:
When MCLK1/2, BICK1/2 and LRCK1/2 are input after the PDN1/2 pin = “L” → “H”, the voltage on the CVEE pin rises to CVEE voltage approximately in 1.3msec@48kHz.
Note: If the PWAD and PWDA bits are set to “1”, or PDN1 and PDN2 pins are set to “H” during a power-up sequence of the charge-pump, ADC and DAC are initialized after the charge-pump circuit is powered on.

(3) The analog block of ADC is initialized after exiting the power-down state. timeA=528/fs

(4) The analog block of DAC is initialized after exiting the power-down state.
In case of connecting a 1μF capacitor to the VREF2 pin, timeB is shown below.
timeB= 6/fs x 8 x 2: Normal Speed Mode
timeB=12/fs x 8 x 2: Double Speed Mode
timeB= 24/fs x 8 x 2: Quad Speed Mode
D/A data input become available after the timeB period.

(5) Digital outputs corresponding to analog inputs and analog outputs corresponding to digital inputs have group delay (GD).

(6) ADC outputs “0” data in power-down state.

(7) Charge Pump Circuit Power-down
(PDN1 pin = “H”→“L” or No MCLK1, BICK1 and LRCK1 inputs) and (PDN2 pin = “H”→“L” or No MCLK2, BICK2 and LRCK2 inputs)
The CVEE pin output becomes 0V according to a flying capacitor and an internal resistor. The internal resistance is 50kΩ (typ). Therefore, when the CVEE pin has a flying capacitor of 1μF, the time constant is 50msec (typ).

(8) It takes 2048/fs for VREF1 stabilization after the charge pump is powered up.

(9) It takes approximately 5msec (typ) until VREF1/2 rises up after power-down mode of ADC/DAC is released.

■ Serial Control Interface

The AK4688 supports fast-mode I^{2}C-bus system (max: 400kHz).

1. Data Transfer

In order to access any IC devices on the I^{2}C BUS, input a start condition first, followed by a single slave address which includes the device address. IC devices on the BUS compare this slave address with their own addresses and the IC device which has an identical address with the slave-address generates an acknowledgement. The IC device with the identical address executes either a read or a write operation. After the command execution, input a stop condition.

1-1. Data Change

Change the data on the SDA line while SCL line is "L". SDA line condition must be stable and fixed while the clock is "H". Change the Data line condition between "H" and "L" only when the clock signal on the SCL line is "L". Change the SDA line condition while SCL line is "H" only when the start condition or stop condition is input.

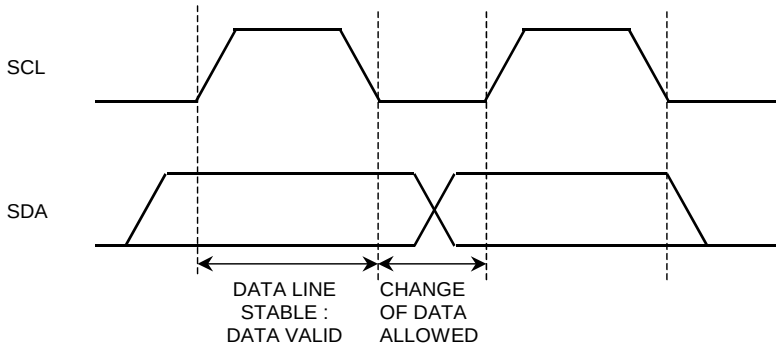


Figure 12. Data Transfer

1-2. Start Condition and Stop Condition

A start condition is generated by the transition of "H" to "L" on the SDA line while the SCL line is "H". All instructions are initiated by a start condition. A stop condition is generated by the transition of "L" to "H" on SDA line while SCL line is "H". All instructions end by a stop condition.

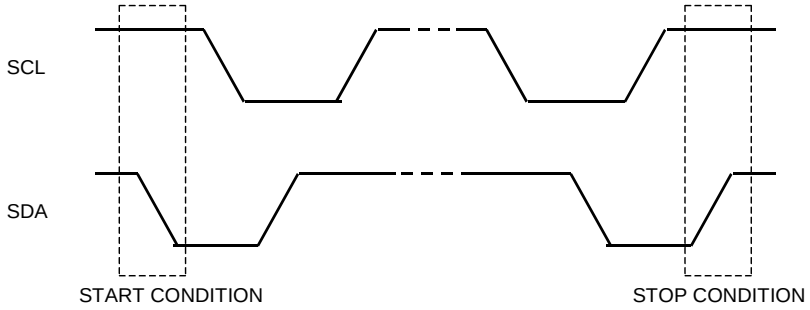


Figure 13. START and STOP Conditions

1-3. Acknowledge

An external device that is sending data to the AK4688 releases the SDA line ("H") after receiving one-byte of data. An external device that receives data from the AK4688 then sets the SDA line to "L" at the next clock. This operation is called "acknowledgement", and it enables verification that the data transfer has been properly executed. The AK4688 generates an acknowledgement upon receipt of a start condition and Slave address. For a write instruction, an acknowledgement is generated whenever receipt of each byte is completed. For a read instruction, succeeded by generation of an acknowledgement, the AK4688 releases the SDA line after outputting data at the designated address, and it monitors the SDA line condition. When the master side generates an acknowledgement without sending a stop condition, the AK4688 outputs data at the next address location. When no acknowledgement is generated, the AK4688 ends data output (not acknowledged).

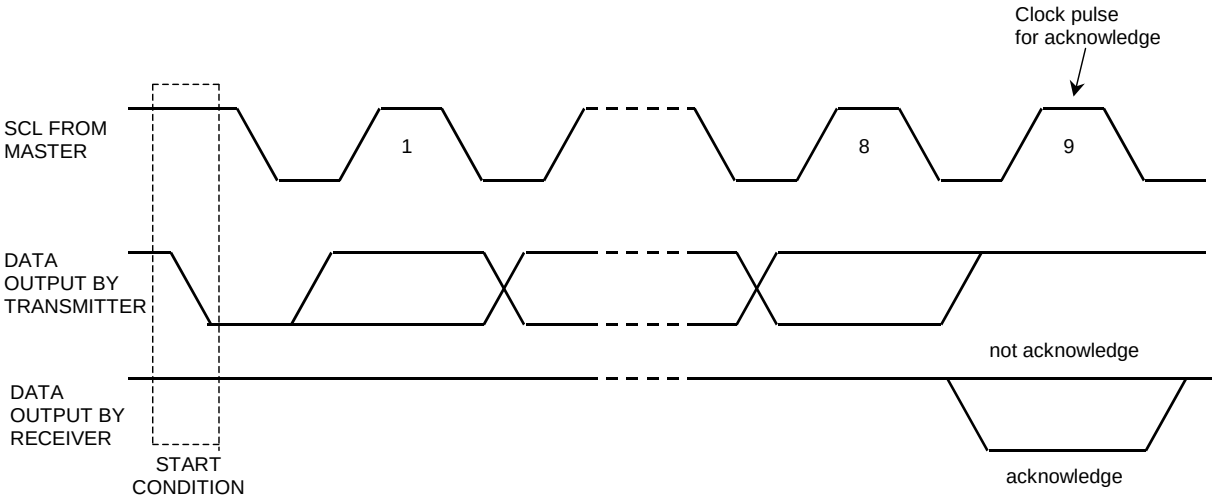


Figure 14. Acknowledge on the I^2C-bus

1-4. FIRST BYTE

The First Byte which includes the Slave-address is input after the Start condition is set, and a target IC device that will be accessed on the bus is selected by the Slave-address. The Slave-address is configured with the upper 7-bits. Data of the upper 6-bits is "001001". The next 1 bit is the address bit that selects the desired IC (CAD0 bit). Set CAD0 bit according to the CAD0 pin setting (CAD0 pin = "L": CAD0 bit = "0", CAD0 pin = "H": CAD0 bit = "1"). When the Slave-address is inputted, an external device that has the identical device address generates an acknowledgement and executes commands. The 8th bit of the First Byte (LSB) is allocated as R/W bit. When the R/W bit is "1", a read instruction is executed, and when it is "0", a write instruction is executed.

0	0	1	0	0	1	CAD0	R/W

Figure 15. The First Byte

2. WRITE Operations

Set R/W bit = "0" for the WRITE operation of the AK4688.
After receipt of the start condition and the first byte, the AK4688 generates an acknowledge, and awaits the second byte (register address). The second byte consists of the address for control registers of AK4688. The format is MSB first, and those most significant 3-bits are "Don't care".

*	*	*	A4	A3	A2	A1	A0

(*: Don't care)

Figure 16. The Second Byte

After receipt of the second byte, the AK4688 generates an acknowledge, and awaits the third byte. Those data after the second byte contain control data. The format is MSB first, 8bits.

D7	D6	D5	D4	D3	D2	D1	D0

Figure 17. Byte Structure after the Second Byte

The AK4688 is capable of more than one byte write operation by one sequence.
After receipt of the third byte, the AK4688 generates an acknowledge, and awaits the next data again. The master can transmit more than one data word instead of terminating the write cycle after the first data word is transferred. After the receipt of each data, the internal address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 03H prior to generating a stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

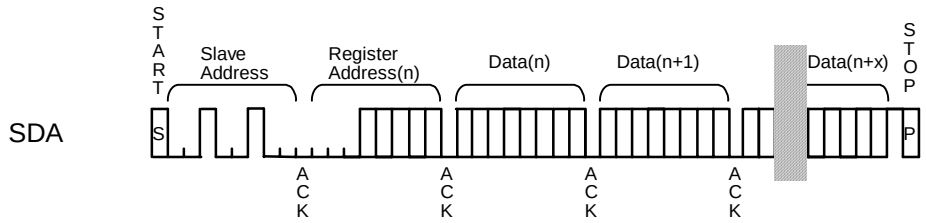


Figure 18. WRITE Operation

3. READ Operations

Set R/W bit = "1" for a READ operation of the AK4688.
The master can read next address's data by generating an acknowledge instead of terminating the write cycle after the receipt of the first data word. After the receipt of each data, the internal 3bits address counter is incremented by one, and the next data is taken into next address automatically. If the address exceeds 03H prior to generating stop condition, the address counter will "roll over" to 00H and the previous data will be overwritten.

The AK4688 supports two basic read operations: CURRENT ADDRESS READ and RANDOM READ.

3-1. CURRENT ADDRESS READ

The AK4688 contains an internal address counter that maintains the address of the last word accessed, incremented by one. Therefore, if the last access (either a read or write) was to address "n", the next CURRENT READ operation would access data from the address "n+1".
After receipt of the slave address with R/W bit set to "1", the AK4688 generates an acknowledge, transmits 1byte data, which address is set by the internal address counter, and increments the internal address counter by 1. If the master does not generate an acknowledge but generate stop condition, the AK4688 discontinues transmission

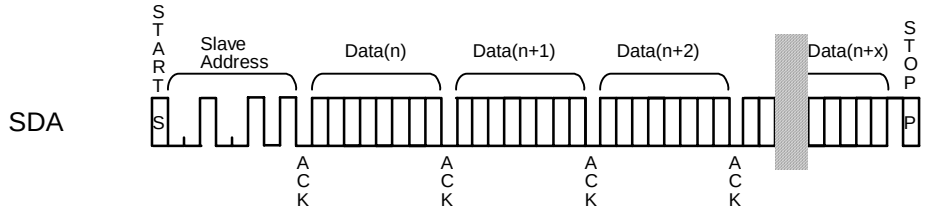


Figure 19. CURRENT ADDRESS READ

3-2. RANDOM READ

Random read operation allows the master to access any memory location at random. Prior to issuing the slave address with the R/W bit set to "1", the master must first perform a "dummy" write operation.
The master issues a start condition, slave address(R/W bit="0") and then the register address to read. After the register address's acknowledge, the master immediately reissues the start condition and the slave address with the R/W bit set to "1". Then the AK4688 generates an acknowledge, 1byte data and increments the internal address counter by 1. If the master does not generate an acknowledge but generate the stop condition, the AK4688 discontinues transmission.

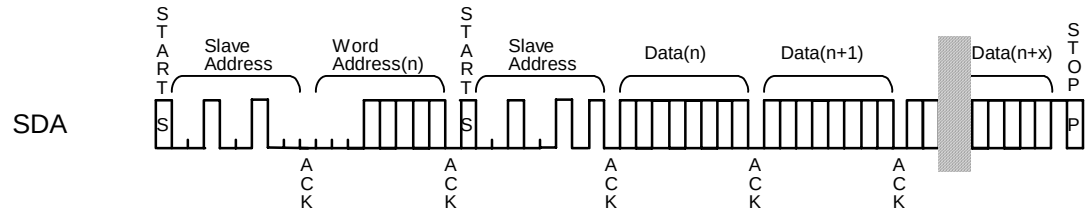


Figure 20. RANDOM READ

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Powerdown/Control	0	0	0	0	0	0	PWDA	PWAD
01H	(Reserved)	0	0	0	0	0	0	0	0
02H	ADC Clock	0	0	0	DIF1	0	CKS1	CKS0	0
03H	DAC Clock	0	ACKS	DFS1	DFS0	DEM	DIF21	DIF20	SMUTE

Note: For addresses from 04H to 1FH, data must not be written.

All registers are initialized to their default values by setting the PDN1 and PDN2 pins to “L”.

ADC is powered down by setting the PDN1 pin to “L”. Registers for ADC (Addr: 01h-02h) and PWAD bit are initialized.

DAC is powered down by setting the PDN2 pin to “L”. Registers for DAC (Addr: 03h) and PWDA bit are initialized.

ADC is powered down by setting the PWAD bit to “0”. However, registers for ADC (Addr: 01h-02h) are not initialized.

DAC is powered down by setting the PWDA bit to “0”. However, registers for DAC (Addr: 03h) is not initialized.

The bits defined as 0 must contain a “0” value.

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Power down/Control	0	0	0	0	0	0	PWDA	PWAD
R/W		RD	RD	RD	RD	RD	RD	R/W	R/W
Default		0	0	0	0	0	0	0	0

PWAD: ADC Power-down Control
0: Power-down (default)
1: Normal operation

PWDA: DAC Power-down Control
0: Power-down (default)
1: Normal operation

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	(Reserved)	0	0	0	0	0	0	0	0
R/W		RD	RD	RD	RD	RD	RD	RD	RD
Default		0	0	0	0	0	0	0	0

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	ADC Clock	0	0	0	DIF1	0	CKS1	CKS0	0
R/W		RD	RD	RD	R/W	RD	R/W	R/W	RD
Default		0	0	0	0	0	1	1	0

CKS1-0: PORT1 (ADC) Clock Control in Master Mode
See Table 6.

DIF1: PORT1 Audio Format Select
See Table 17.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	DAC Clock	0	ACKS	DFS1	DFS0	DEM	DIF21	DIF20	SMUTE
R/W		RD	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Default		0	1	0	0	0	1	0	0

SMUTE: Soft Mute control for DAC
0: Normal Operation (default)
1: LOUT/ROUT outputs soft-muted

DIF21-20: PORT2 Audio Format Select
See Table 18.

DEM: DAC De-emphasis Response Control
See Table 16.

DFS1-0: PORT2 (DAC) Sampling Speed Control
See Table 9. DFS1-0 bits setting is ignored in Auto Setting Mode (ACKS bit = "1").

ACKS: PORT2 (DAC) Auto Setting Mode Control
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode (default)
The MCLK frequency is detected automatically when ACKS bit= "1". In this case, DFS1-0 bits settings are ignored. When ACKS bit = "0", DFS1-0 bits select the sampling speed mode, and the MCLK frequency is automatically detected in each mode.

SYSTEM DESIGN

Figure 21 shows the system connection diagram. An evaluation board (AKD4688) demonstrates the optimum layout, power supply arrangements and measurement results.

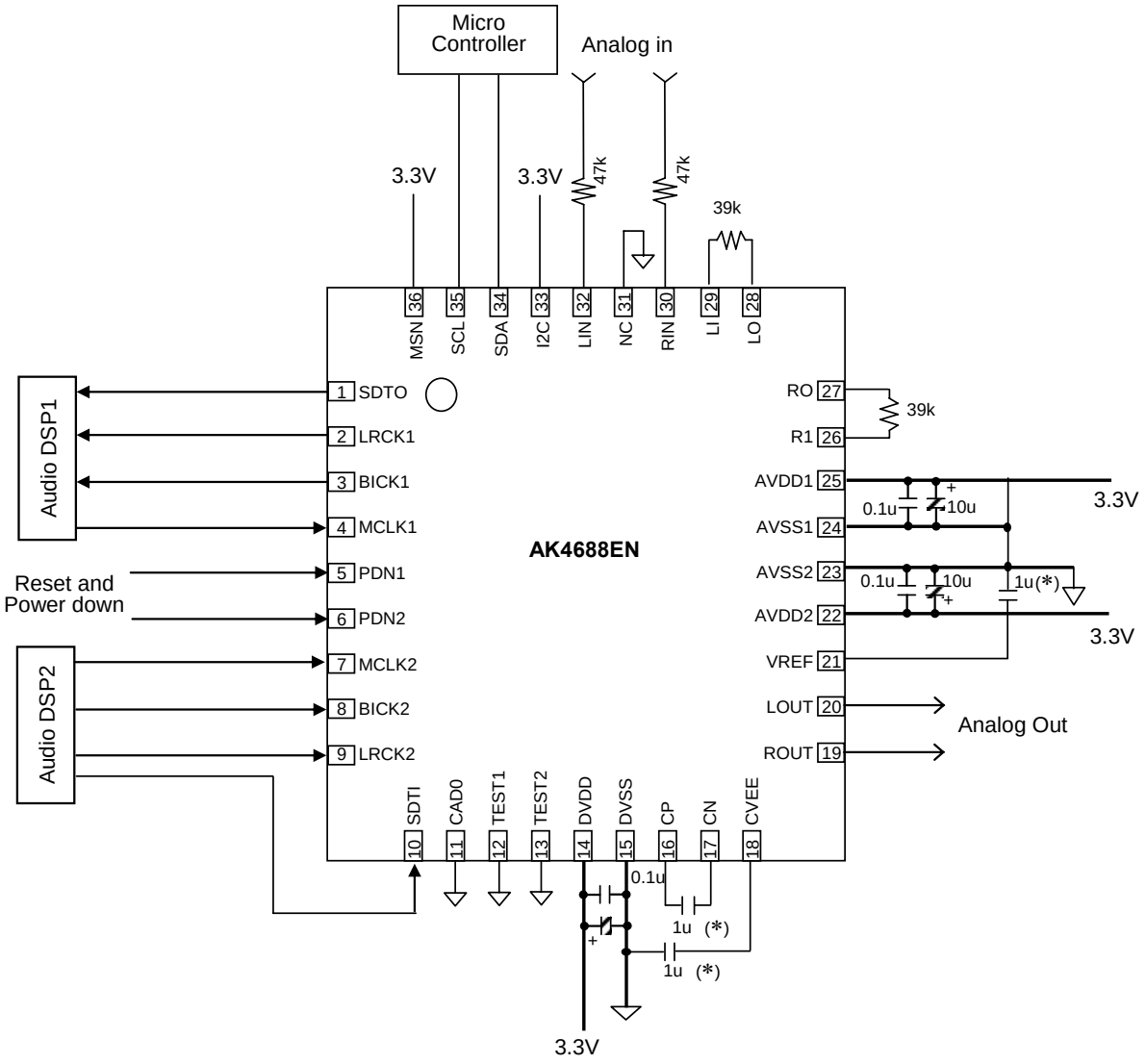


Figure 21. Typical Connection Diagram (I^2C Control mode, CAD0 pin = "L", Master mode)

Notes:

(1) Use low ESR (Equivalent Series Resistance) capacitors for the capacitors with (*). When using polarized capacitors, the positive polarity pin should be connected to the CP or VREF1/2 pin, and the negative polarity pin should be connected to the CVEE pin.

(2) AVSS1, AVSS2 and DVSS must be connected to the same analog ground plane.

(3) Digital input pins should not be allowed to float.

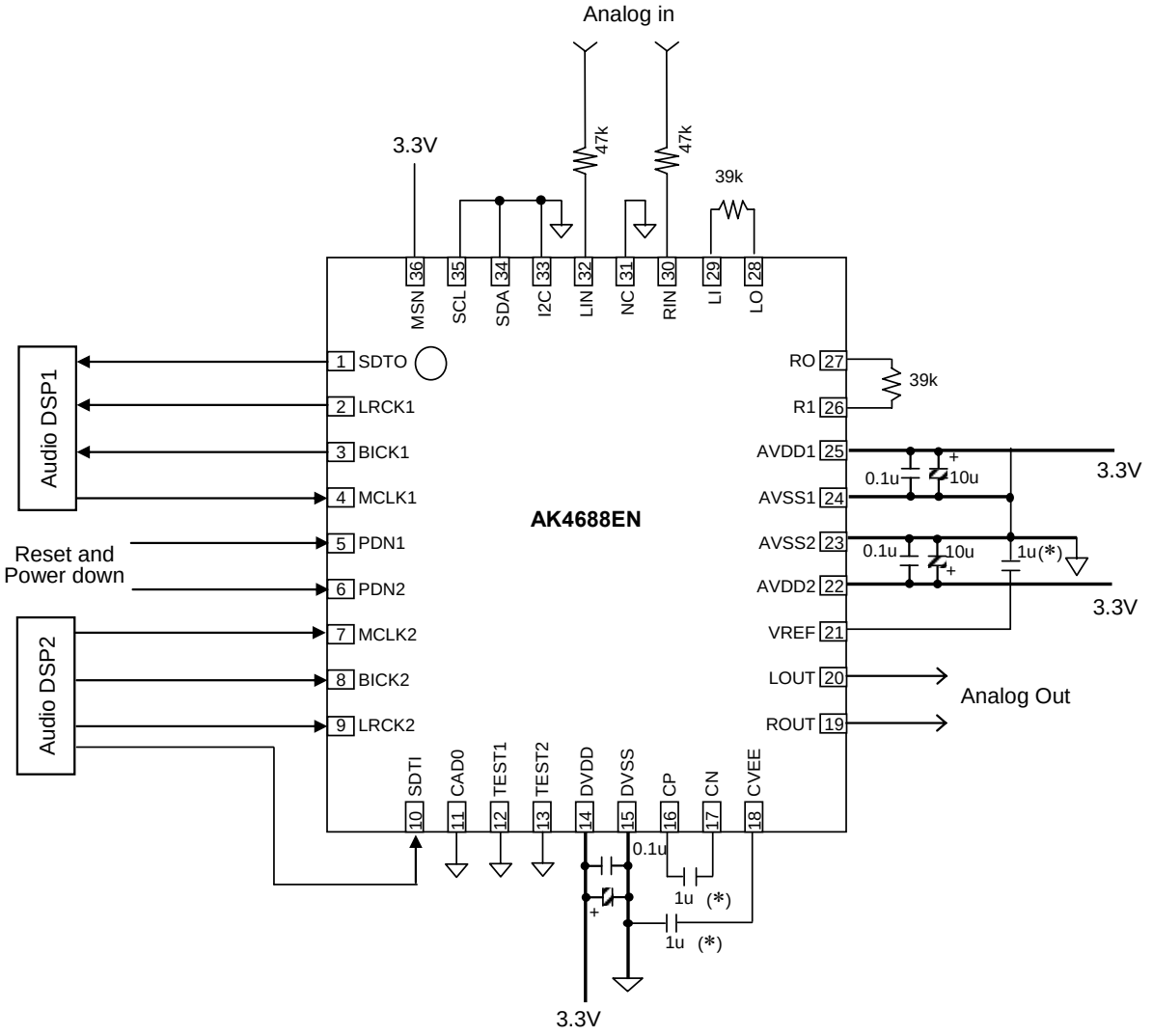


Figure 22. Typical Connection Diagram (H/W Control mode, MCLK=768fs, Master mode)

Notes:

(1) Use low ESR (Equivalent Series Resistance) capacitors for the capacitors with (*). When using polarized capacitors, the positive polarity pin should be connected to the CP or VREF1/2 pin, and the negative polarity pin should be connected to the CVEE pin.

(2) AVSS1, AVSS2 and DVSS must be connected to the same analog ground plane.

(3) Digital input pins should not be allowed to float.

1. Grounding and Power Supply Decoupling

The AK4688 requires careful attention to power supply and grounding arrangements. AVDD1, AVDD2 and DVDD are usually supplied from the system's analog supply. If AVDD1, AVDD2 and DVDD are supplied separately, the power up sequence is not critical. **AVSS1, AVSS2 and DVSS of the AK4688 must be connected to the same analog ground plane.** System analog ground and digital ground should be wired separately and connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors should be as near to the AK4688 as possible, with the small value ceramic capacitor being the nearest.

2. Voltage Reference Inputs

The voltage difference between AVDD1 and AVSS1 sets the analog input range, and the voltage difference between AVDD2 and AVSS2 sets the analog output range. VREF is a signal common of this chip. A 1μF ceramic capacitor connected between the AVSS1/AVSS2 and VREF pins eliminates the effects of high frequency noise. No load current may be drawn from the VREF pin. All signals, especially clocks, should be kept away from the VREF pin in order to avoid unwanted coupling into the AK4688.

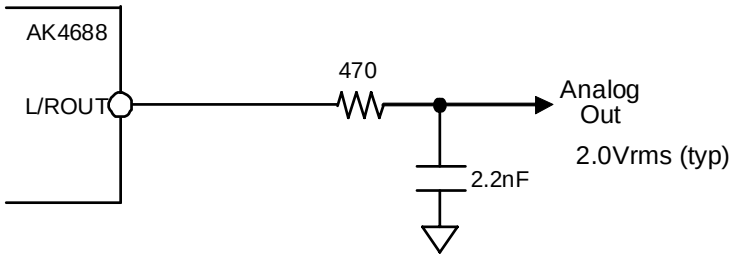
3. Analog Inputs

The analog input is single-ended and supplied to the Pre-amp via external resistors. Select the feedback resistance to make the pre-amp output match to the input range (typ. 1.91Vrms) of the ADC (LO and RO pins). The ADC output data format is 2's complement. The internal digital HPF removes the DC offset. The AK4688 samples the analog inputs at 64fs. The digital filter rejects noise above the stop band except for multiples of 64fs. The AK4688 includes an anti-aliasing filter (RC filter) to attenuate a noise around 64fs.

4. Analog Outputs

The analog outputs are single-ended and centered around the AVSS2 (0V typ.) voltage. The output signal range is typically 2.0Vrms (typ @AVDD2=3.3V). The internal switched-capacitor filter (SCF) and continuous-time filter (CTF) attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Using a 1st-order LPF (Figure 23) can reduce noise beyond the audio passband.

The output voltage is a positive full scale for 7FFFFFH (@24bit) and a negative full scale for 800000H (@24bit). The ideal output is 0V (VSS) for 000000H (@24bit). The DC offset is within ±5mV.



(fc = 154kHz, gain = -0.28dB @ 40kHz, gain = -1.04dB @ 80kHz)

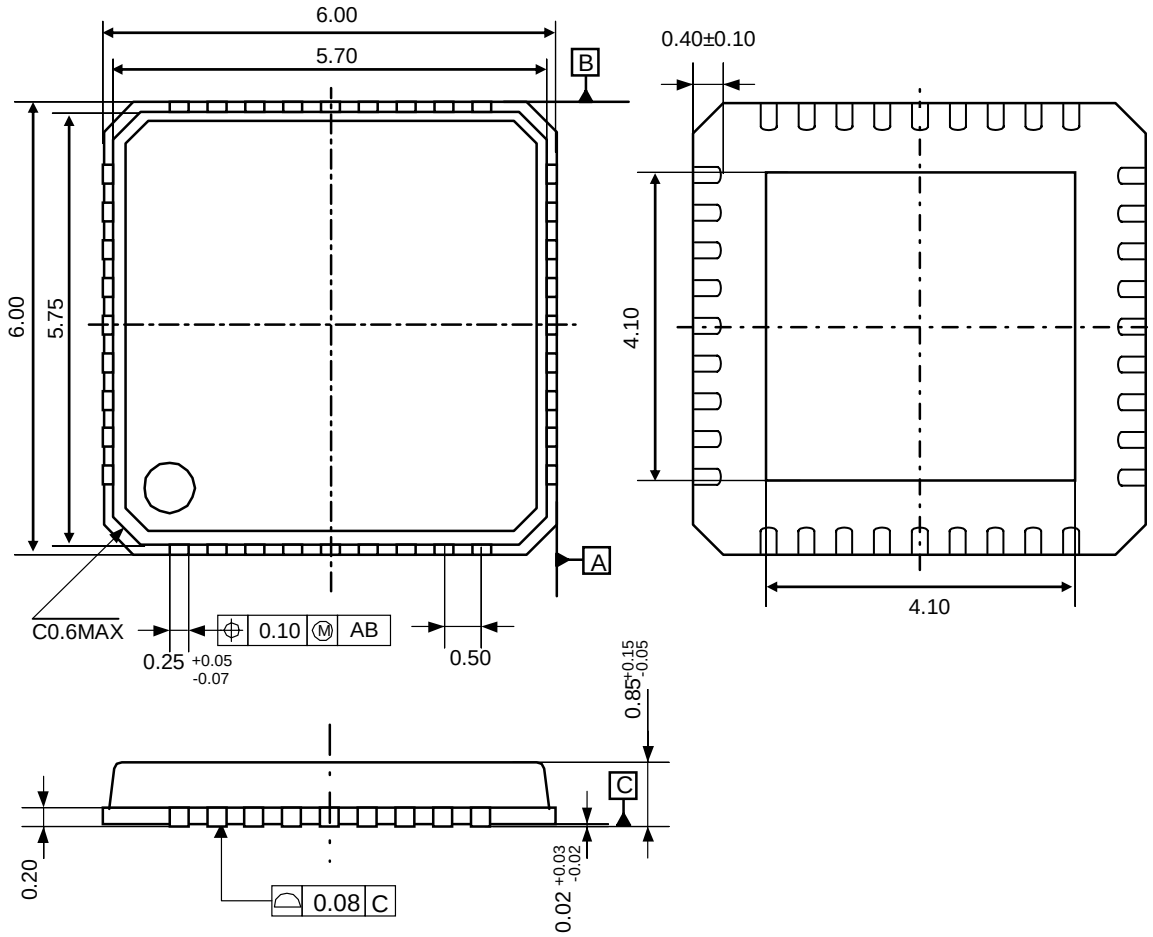
Figure 23. External Circuit Example1

5. Attention to the PCB Wiring

LIN and RIN pins are the summing nodes of the Pre-Amp. Attention should be given to avoid coupling with other signals on those nodes. This can be accomplished by making the wire length of the input resistors as short as possible. The same theory also applies to the LI/RI pins and feedback resistors; keep the wire length to a minimum. Unused input pins among LIN and RIN pins must be left open.

PACKAGE

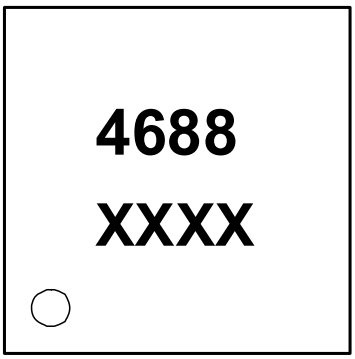
36-pin QFN (Unit: mm)



■ Material & Lead Finish

Package molding compound: Epoxy, Halogen (Br and Cl) free
Lead frame material: Cu
Lead frame surface treatment: Solder (Pb free) plate

MARKING



Pin #1 indication
Date Code: XXXX (4 digits)

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
12/05/29	00	First Edition		

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