= Preliminary =

AK7601A

High Feature Digital Audio Processor with SRC

GENERAL DESCRIPTION

AK7601A is a high feature audio processor with audio CODEC (3ch ADC, 6ch DAC) and delay line memory operates 5.0V single power supply. The analog inputs support quasi-differential/single-ended with 4:1 stereo selector in front of 2-channeled 97dB ADC, and monaural ADC for guidance sound. The digital inputs supports 3:1 input selector with asynchronous Sample Rate Converter (SRC) for digital source such as DVD, Blu-ray, digital broadcasting, etc. The high performance 6-channeled DAC integrates full-range digital volume control and achieves 102dB with single end outputs. The delay line memory covers 36ms in total. Time alignment of 6m or less is possible since the delay line memory can store for 18ms data for both left and right channels. The AK7601A can achieve high performance car audio system easily by supporting two stereo 7-band EQ and time alignment functions.

FEATURES

1. **2ch 24bit ADC**
   - **Quasi-Differential/Single-ended inputs with 4:1 Stereo Selector**
   - **S/(N+D): 90dB**
   - **DR, S/N: 97dB**
   - **Digital HPF for cancelling DC offset**
2. **1ch 24bit ADC for Monaural Audio Input**
   - **Single-ended input**
   - **S/(N+D): 90dB**
   - **DR, S/N: 97dB**
   - **Digital HPF for cancelling DC offset**
3. **6ch 24bit DAC**
   - **Single-ended output**
   - **S/(N+D): 90dB**
   - **DR, S/N: 102dB**
4. **Asynchronous Sample Rate Converter(SRC) for Digital Input**
   - **3:1 Input Selector**
   - **Input Sampling Rate: 8kHz ~ 96kHz**
   - **Data Format: MSB justified, LSB justified, I^2S compatible (slave mode only)**
5. **Digital Processing**
   - **Two Stereo 7Band EQ (Second-order IIR-filter setting is also available)**
   - **Digital De-emphasis Filter**
   - **Adjustable Delay Memory Control**
     Maximum Delay Time:
     Lch 18ms, Rch 18ms (for 1 stereo input / 3 stereo outputs)
     Delay Resolution: 1/fs
   - **X'Over filter:**
     Front L, Front R: 2^{nd} order IIR Filter x 3 stages
     Rear L, Rear R, Subwoofer L, Subwoofer R: 2^{nd} order IIR Filter x 2 stages
   - **Spectrum analyzer: Variable 4-Band**
   - **Soft Mute**
   - **Zero Detect Function**
6. **Smooth Volume**
7. **Master Clock**
   - **Master Mode: 22.5792MHz**
8. **μP Interface: I^2C Bus (Ver 1.0, 400kHz mode)**

9. **Power Supply**
   - **Analog: AVDD = 4.5 ~ 5.5V**
   - **Digital: DVDD = 3.0 ~ 5.5V**
10. **Power Consumption: 80mA**
11. **Ta = - 40 ~ 85℃**
12. **Package: 48LQFP(0.5mm pitch)**

■ Block Diagram

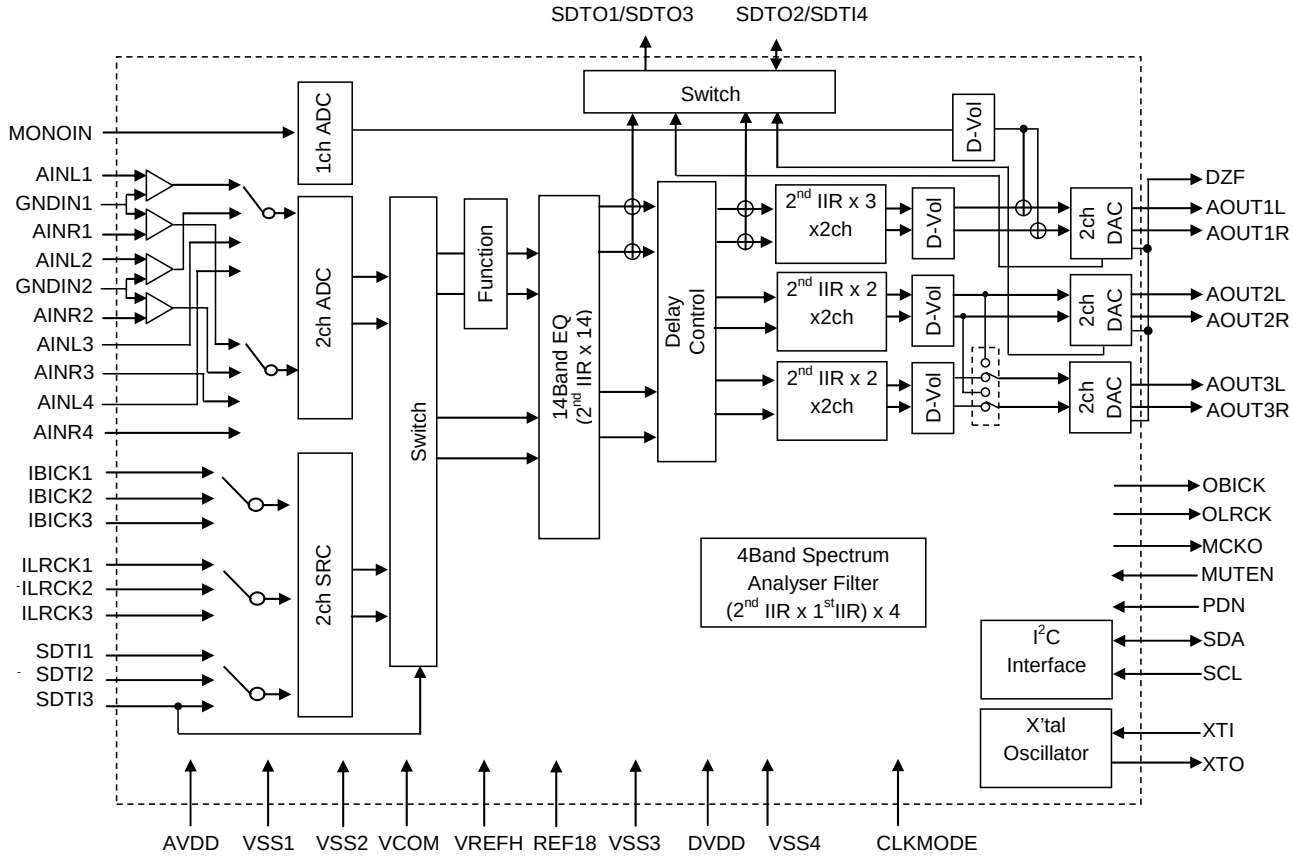


Figure 1. Block Diagram

■ Ordering Guide

AK7601AVQ	-40 ~ +85°C	48pin LQFP(0.5mm pitch)
AKD7601A	Evaluation board for AK7601A	

■ Pin Layout

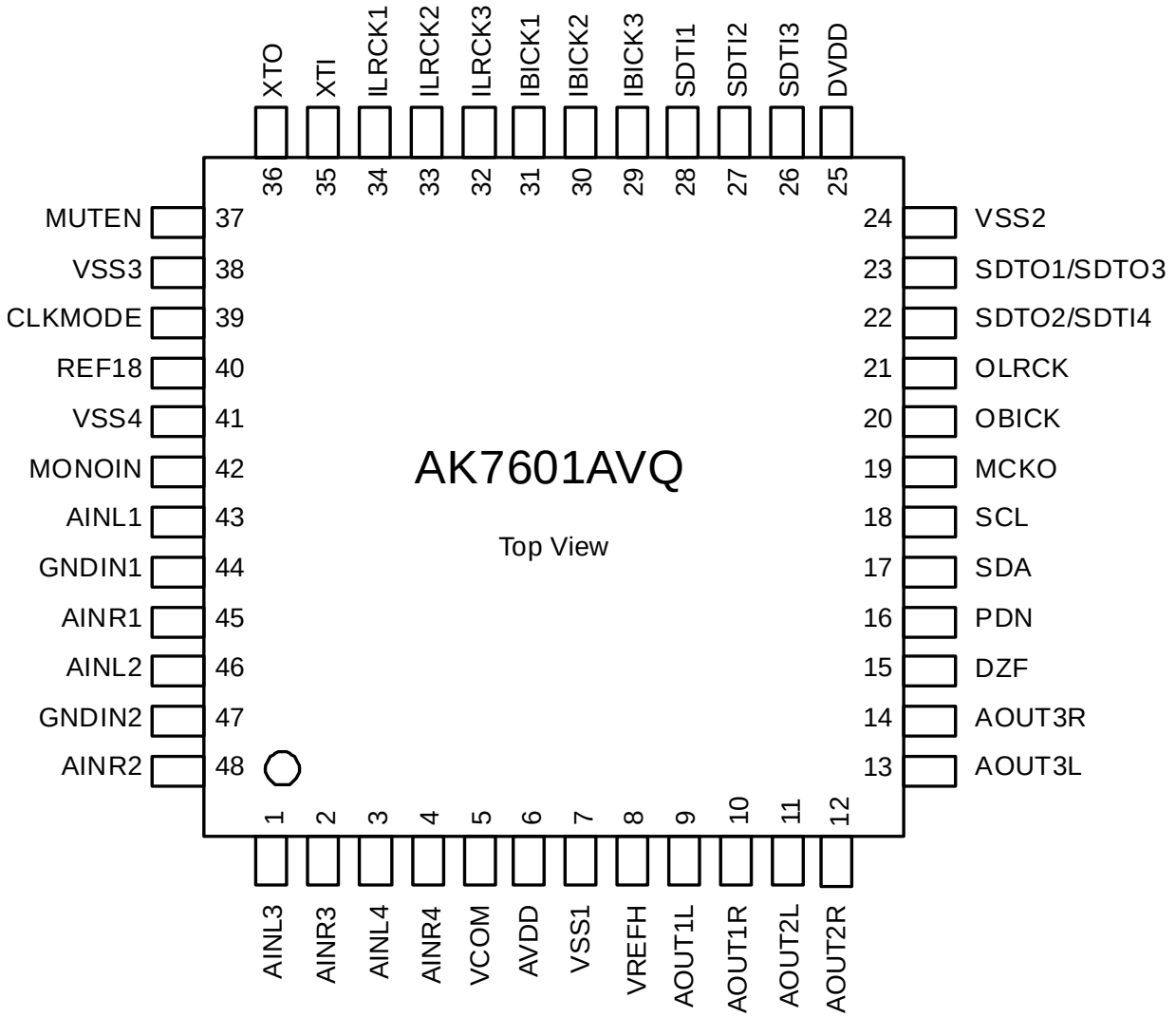


Figure 2. Pin Layout

PIN FUNCTION

No.	Pin Name	I/O	Function
1	AINL3	I	Lch Single-ended Input 3 Pin
2	AINR3	I	Rch Single-ended Input 3 Pin
3	AINL4	I	Lch Single-ended Input 4 Pin
4	AINR4	I	Rch Single-ended Input 4 Pin
5	VCOM	O	VCOM pin
6	AVDD	-	Analog Power Supply Pin 4.5~5.5V
7	VSS1	-	Ground Pin, 0V
8	VREFH	-	Positive Voltage Reference Input Pin, AVDD
9	AOUT1L	O	DAC1 Lch Output pin.
10	AOUT1R	O	DAC1 Rch Output pin
11	AOUT2L	O	DAC2 Lch Output pin
12	AOUT2R	O	DAC2 Rch Output pin
13	AOUT3L	O	DAC3 Lch Output pin
14	AOUT3R	O	DAC3 Rch Output pin
15	DZF	O	Zero detect pin
16	PDN	I	Power-Down & Reset Pin When "L", the AK7601A is powered-down and the control registers are reset to default state.
17	SDA	I/O	Control Data Input Pin : SDA (I^2C Bus) (Note 2)
18	SCL	I	Control Data Clock Pin : SCL (I^2C Bus)
19	MCKO	O	Master Clock Output Pin
20	OBICK	O	Output Audio Serial Data Clock Pin
21	OLRCK	O	Output Channel Clock Pin
22	SDTO2/SDTI4	I/O	Audio Serial Data Input 4 / Output 2 Pin (Note 3)
23	SDTO1/SDTO3	O	Audio Serial Data Output 1/3 Pin
24	VSS2	-	Ground Pin, 0V
25	DVDD	-	Digital Power Supply 1 Pin, 3.0 ~5.5V
26	SDTI3	I	Audio Serial Data Input 1 Pin
27	SDTI2	I	Audio Serial Data Input 2 Pin
28	SDTI1	I	Audio Serial Data Input 3 Pin
29	IBICK3	I	Input Audio Serial Data Clock Pin 3 Pin
30	IBICK2	I	Input Audio Serial Data Clock Pin 2 Pin
31	IBICK1	I	Input Audio Serial Data Clock Pin 1 Pin
32	ILRCK3	I	Input Channel Clock 3 Pin
33	ILRCK2	I	Input Channel Clock 2 Pin
34	ILRCK1	I	Input Channel Clock 1 Pin
35	XTI	I	X'tal Input Pin
36	XTO	O	X'tal Output Pin
37	MUTEN	I	AK7601A Mute Pin L: Mute H: Normal Operation
38	VSS3(DVSS)	-	Ground Pin 0V
39	CLKMODE	I	CLK Mode Pin (X'tal/External CLK select pin) L: X'tal Mode H External CLK Input Mode The PDN pin must set "H" → "L" → "H" before changing this pin "L" → "H".
40	REF18	O	Internal regulator 1.8V Output pin
41	VSS4	-	Ground Pin, 0V
42	MONOIN	I	Monaural ADC Input Pin
43	AINL1	I	Lch Differential Input 1 Pin
44	GNDIN1	I	Input Ground 1 Pin
45	AINR1	I	Rch Differential Input 1 Pin
46	AINL2	I	Lch Differential Input 2 Pin
47	GNDIN2	I	Input Ground 2 Pin
48	AINR2	I	Rch Differential Input 2 Pin

Note 1. All digital input pins must not be allowed to float.
Note 2. Input pin when powered-down.
Note 3. Output pin when powered-down

■Handling of Unused Pin

The unused I/O pins should be processed appropriately as below

Classification	Pin Name	Setting
Analog	AINL1, GNDIN1, AINR1, AINL2, GNDIN2, AINR2, AINL3, AINR3, AINL4, AINR4, MONOIN	Open
	AOUT1L, AOUT1R, AOUT2L, AOUT2R, AOUT3L, AOUT3R	Open
Digital	IBICK1, IBICK2, IBICK3, ILRCK1, ILRCK2, ILRCK3, SDTI1, SDTI2, SDTI3, SDTI4	Connect to VSS2
	OBICK, OLRCK, MCKO, SDTO1/SDTO3, SDTO2, XTO	Open

ABSOLUTE MAXMUM RATING

(VSS1=VSS2=VSS3=VSS4=0V; Note 4)

Parameter		Symbol	min	max	Unit
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 5)		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage (Note 6)		VIND	-0.3	DVDD+0.3	V
Ambient Temperature (power applied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 4. All indicated voltages are with respect to ground VSS1, VSS2, VSS3 and VSS4 must be connected to the analog ground plane.

Note 5. Analog input pins are AINL1-4, AINR1-4, GNDIN1-2 and MONOIN.

Note 6. Digital input pins are SDTI1-4, ILRCK1-3, IBICK1-3, MUTEN, SDA, and SCL.

WARNING: Operating at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these critical conditions.

RECOMMENDED OPERATING CONDITIONS

(VSS1=VSS2=VSS3=VSS4 =0V; Note 4)

Parameter		Symbol	min	typ	max	Unit
Power Supplies	Analog	AVDD	4.5	5.0	5.5	V
(Note 7)	Digital	DVDD	3.0	5.0	AVDD	V

Note 7. The power up sequence between AVDD and DVDD is not critical but the PDN pin must be “L” until all power supplies are ON, then put the PDN pin to “H”. All power supplies of the AK7601A are must be ON. Do not turn any power supply off (means the same voltage as ground or floating) independently. When using the AK7601A with I²C bus, the power supply of the AK7601A must not be turned off unless the power supplies of the surrounding device are turned off.

* AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD=5.0V, DVDD =5.0V; VSS1=VSS2=VSS3=VSS4=0V; VREFH=AVDD, fs=44.1kHz; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz at; unless otherwise specified)

Parameter			min	typ	max	Unit
ADC Analog Input Characteristics (Pseudo differential inputs)						
Resolution					24	Bits
S/(N+D)	BW=20kHz	-1dBFS	83	90		dB
		-60dBFS		35		
DR (-60dBFS with A-weighted)			90	97		dB
S/N (A-weighted)			90	97		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Input Voltage	AIN=0.65xVREFH		3.09	3.25	3.41	Vpp
Input Resistance	AINL1, AINR1, AINL2, AINR2		22	45		kΩ
	GNDIN1, GNDIN2		22	90		kΩ
Power Supply Rejection (Note 8)				55		dB
Common Mode Rejection Ratio (CMRR) (Note 9)			40			dB
ADC Analog Input Characteristics (Single-ended inputs)						
Resolution					24	Bits
S/(N+D)	BW=20kHz	-1dBFS	83	90		dB
		-60dBFS		35		
DR (-60dBFS with A-weighted)			90	97		dB
S/N (A-weighted)			90	97		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Input Voltage	AIN=0.65xVREFH		3.09	3.25	3.41	Vpp
Input Resistance (AINL3, AINR3, AINL4, AINR4)			22	45		kΩ
Power Supply Rejection (Note 8)				55		dB
ADC Analog Input Characteristics (Monaural input)						
Resolution					24	Bits
S/(N+D)	BW=20kHz	-1dBFS	83	90		dB
		-60dBFS		35		
DR (-60dBFS with A-weighted)			90	97		dB
S/N (A-weighted)			90	97		dB
Gain Drift				20	-	ppm/°C
Input Voltage	AIN=0.65xVREFH		3.09	3.25	3.41	Vpp
Input Resistance			22	45		kΩ
Power Supply Rejection (Note 8)				55		dB
DAC Analog Output Characteristics (single outputs)						
Resolution					24	Bits
S/(N+D)	BW=20kHz	0dBFS	83	90		dB
		-60dBFS		39		
DR (-60dBFS with A-weighted)			93	102		dB
S/N (A-weighted)			93	102		dB
Interchannel Isolation			90	110		dB
Interchannel Gain Mismatch				0	0.5	dB
Gain Drift				20	-	ppm/°C
Output Voltage	AOUT=0.65xVREFH		3.09	3.25	3.41	Vpp
Load Resistance (AC Load)			5			kΩ
Load Capacitance					30	pF
Power Supply Rejection (Note 8)				55		dB

ADC to DAC Characteristics (single outputs)						
Resolution					24	Bits
S/(N+D)	BW=20kHz	-1dBFS	80	87		dB
		-60dBFS		34		
DR	(-60dBFS with A-weighted)		87	96		dB
S/N	(A-weighted)		87	96		dB

Note 8. PSR is applied to AVDD and DVDD with 1kHz, 50mVpp. This is the value of convoluted sinusoidal voltage of 1kHz and 50mVpp when the VREFH pin is held +5V.

Note 9. This is a value when the frequency range is 20Hz ~ 20kHz assuming an external capacitor is 10uF±30% and GDNIN1/2 amplitude is 100mVpp.

SRC CHARACTERISTICS

(Ta=25°C; AVDD=5.0V, DVDD =5.0V; VSS1=VSS2=VSS3=VSS4=0V; VREFH=AVDD, fs=44.1kHz; Signal Frequency=1kHz; 24bit Data; Measurement Frequency=20Hz~20kHz; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
SRC Characteristics:					
Resolution				24	Bits
Input Sample Rate	FSI	8		96	kHz
Output Sample Rate	FSO		44.1		kHz
THD+N (Input = 1kHz, 0dBFS, Note 10) FSI =48kHz			-130	-100	dB
Dynamic Range (Input = 1kHz, –60dBFS, Note 10) FSI = 48kHz			136	120	dB
Dynamic Range (Input = 1kHz, -60dBFS, A-weighted, Note 10) FSI = 48kHz			140		dB
Ratio between Input and Output Sample Rate	FSO/FSI	44.1/96		44.1/8	-

Note 10. Measured by Audio Precision System Two Cascade.

Parameter	min	typ	max	Unit
Power Supplies				
Power Supply Current				
Normal Operation (PDN pin = "H")				
AVDD		54	73	mA
DVDD		11	15	mA
Power-down mode (PDN pin = "L")				
AVDD+DVDD (Note 12)		10	100	μA

Note 11. Power supply current values are for when ADC, DAC and SRC are in operation.

Note 12. When the AK7601A is not in operation. All digital input pins including clock pins are held to VSS2.

FILTER CHARACTERISTICS

(Ta= -40 ~ +85°C; AVDD=4.5~ 5.5V, DVDD=3.0~ 5.5V)

Parameter		Symbol	min	typ	max	Unit
ADC Digital Filter (Decimation LPF):						
Passband (Note 13)	±0.1dB	PB	0	-	17.3	kHz
	−0.2dB		-	18.3	-	kHz
	−3.0dB		-	21.1	-	kHz
Stopband (Note 13)		SB	25.7	-	-	kHz
Passband Ripple		PR	-	-	±0.04	dB
Stopband Attenuation		SA	68	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	16	-	1/fs
ADC Digital Filter (HPF):						
Frequency Response (Note 13)	−3dB	FR	-	0.86	-	Hz
	−0.1dB		-	5.9	-	Hz
DAC Digital Filter (LPF):						
Passband (Note 13)	±0.06dB	PB	0	-	20.0	kHz
	−6.0dB		-	22.05	-	kHz
Stopband (Note 13)		SB	24.1	-	-	kHz
Passband Ripple		PR	-	-	±0.1	dB
Stopband Attenuation		SA	54	-	-	dB
Group Delay Distortion		ΔGD	-	0	-	μs
Group Delay (Note 14)		GD	-	20	-	1/fs
DAC Digital Filter + Analog Filter:						
Frequency Response (Note 15)	20~20kHz	FR	-	±0.1	-	dB

Note 13. The passband and stopband frequencies scale with fs (system sampling rate). For example, when fs= 44.1kHz, DAC is PB=0.45412*fs (@±0.06dB).

Note 14. The calculated delay time induced by digital filtering. This time is from the input of an analog signal to the setting of 24bit data both channels to the ADC output register for ADC. This time is from the set of 24bit data to the input registers to the output of analog signal for DAC.

Note 15. The reference frequency of these responses is 1kHz.

SRC Digital Filter		Symbol	min	typ	max	Unit
Passband -0.01dB	0.985 ≤ FSO/FSI < 5.513	PB	0		0.4583FSI	kHz
	0.656 ≤ FSO/FSI < 0.985	PB	0		0.4167FSI	kHz
	0.492 ≤ FSO/FSI < 0.656	PB	0		0.2177FSI	kHz
	0.459 ≤ FSO/FSI < 0.492	PB	0		0.1948FSI	kHz
Stopband	0.985 ≤ FSO/FSI < 5.513	SB	0.5417FSI			kHz
	0.656 ≤ FSO/FSI < 0.985	SB	0.5021FSI			kHz
	0.492 ≤ FSO/FSI < 0.656	SB	0.2813FSI			kHz
	0.459 ≤ FSO/FSI < 0.492	SB	0.2604FSI			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI < 5.513	SA	121.2			dB
	0.656 ≤ FSO/FSI < 0.985	SA	121.4			dB
	0.492 ≤ FSO/FSI < 0.656	SA	100.2			dB
	0.459 ≤ FSO/FSI < 0.492	SA	103.3			dB
Group Delay (Ts=1/fs) (Note 16)		GD		64		Ts

Note 16.This delay is the period from the rising edge of ILRCK, just after the SDTI data is input, to the rising edge of OLRCK, just after the SDTO data is output, when there is no phase difference between ILRCK and OLRCK.

DC CHARACTERISTICS

(Ta=-40°C~+85°C; AVDD= 4.5~5.5V, DVDD=3.0~5.5V)

Parameter		Symbol	min	typ	max	Unit
High-Level Input Voltage (PDN, SDA, SCL, SDTI1-4, ILRCK1-3, IBICK1-3, MUTEN, XTI pins)		VIH	70%DVDD	-	-	V
(CLKMODE pin)		VIH	80%DVDD	-	-	V
Low-Level Input Voltage (PDN, SDA, SCL, SDTI1-4, ILRCK1-3, IBICK1-3, MUTEN, XTI pins)		VIL	-	-	30%DVDD	V
(CLKMODE pin)		VIL	-	-	20%DVDD	V
High-Level Output Voltage (SDTO1-3, OLRCK, OBICK, OMCLK, SDA, DZF pins: Iout=-100µA)		VOH	DVDD-0.5	-	-	V
Low-Level Output Voltage (SDTO1-3, OLRCK, OBICK, OMCLK, DZF pins: Iout= 100µA)		VOL	-	-	0.5	V
(SDA pin: Iout= 3mA)		VOL	-	-	0.4	V
Input Leakage Current	PDN, SDA, SCL, SDTI1-4, ILRCK1-3, IBICK1-3, MUTEN, XTI	Iin	-	-	±10	µA

SWITCHING CHARACTERISTICS

(Ta=-40~+85°C; AVDD=4.5~5.5V; DVDD=3.0~5.5V; C_L=20pF; unless otherwise specified)

Parameter	Symbol	min	typ	max	Unit
Master Clock Timing					
Crystal Resonator		-		-	
Frequency	fXTAL	-	22.5792	-	MHz
MCKO Output					
Frequency MCKO1-0 bit = "10"	fMCK	-	22.5792	-	MHz
MCKO1-0 bit = "01"	fMCK	-	11.2896	-	MHz
Duty cycle 512fs (Note 17)	dMCK	40	50	60	%
256fs (Note 17)	dMCK	45	50	55	%
External Clock					
Frequency	fCLK	22.35	22.5792	22.80	MHz
Pulse Width Low	tCLKL	18			ns
Pulse Width High	tCLKH	18			ns
MCKO Output					
Frequency 512fs	fMCK	22.35	22.5792	22.80	MHz
Duty cycle (Note 18)	dMCK	40	50	60	%
Input LRCK (ILRCK1-3)					
Frequency	FSI	8		96	kHz
Duty Cycle	Duty	48	50	52	%
Output LRCK (OLRCK)					
Frequency	FSO	-	44.1	-	kHz
Duty Cycle	Duty		50		%
Audio Interface Timing					
OBICK Frequency	fBCK	-	64fs	-	Hz
OBICK Duty	dBCK	-	50	-	%
OBICK "↓" to OLRCK	tMBLR	–20	-	20	ns
OBICK "↓" to SDTO1~3	tBSD	–20	-	20	ns
SDTI3-4 Hold Time	tSDH	30			ns
SDTI3-4 Setup Time	tSDL	30			ns
Input PORT					
IBICK1-3 Period	tBCK	1/64fs			ns
IBICK1-3 Pulse Width Low	tBCKL	65			ns
Pulse Width High	tBCKH	65			ns
ILRCK1-3 Edge to IBICK1-3 "↑" (Note 19)	tLRB	30			ns
IBICK1-3 "↑" to ILRCK1-3 Edge (Note 19)	tBLR	30			ns
SDTI1-3 Hold Time from IBICK1-3 "↑"	tSDH	30			ns
SDTI1-3 Setup Time to IBICK1-3 "↑"	tSDS	30			ns

Note 17. According to the crystal oscillator values in Table 2.
Note 18. In the case of MCKO1-0bits = "10" (22.5792MHz), these are the values when External Clock Duty is 50%.
Note 19. BICK rising edge must not occur at the same time as LRCK edge.

Parameter	Symbol	min	typ	max	Unit
Control Interface Timing (I^2C Bus mode):					
SCL Clock Frequency	fSCL	-		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3		-	µs
Start Condition Hold Time (prior to first clock pulse)	tHD:STA	0.6		-	µs
Clock Low Time	tLOW	1.3		-	µs
Clock High Time	tHIGH	0.6		-	µs
Setup Time for Repeated Start Condition	tSU:STA	0.6		-	µs
SDA Hold Time from SCL Falling (Note 20)	tHD:DAT	0		-	µs
SDA Setup Time from SCL Rising	tSU:DAT	0.1		-	µs
Rise Time of Both SDA and SCL Lines	tR	-		0.3	µs
Fall Time of Both SDA and SCL Lines	tF	-		0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6		-	µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb	-		400	pF
Power-down & Reset Timing					
PDN Pulse Width (Note 21)	tPD	150			ns

Note 20. Data must be held long enough to bridge the 300ns-transition time of SCL.
Note 21. The AK7601A can be reset by bringing the PDN pin = “L”.
Note 22. I^2C-bus is a trademark of NXP B.V.

■ **Timing Diagram**

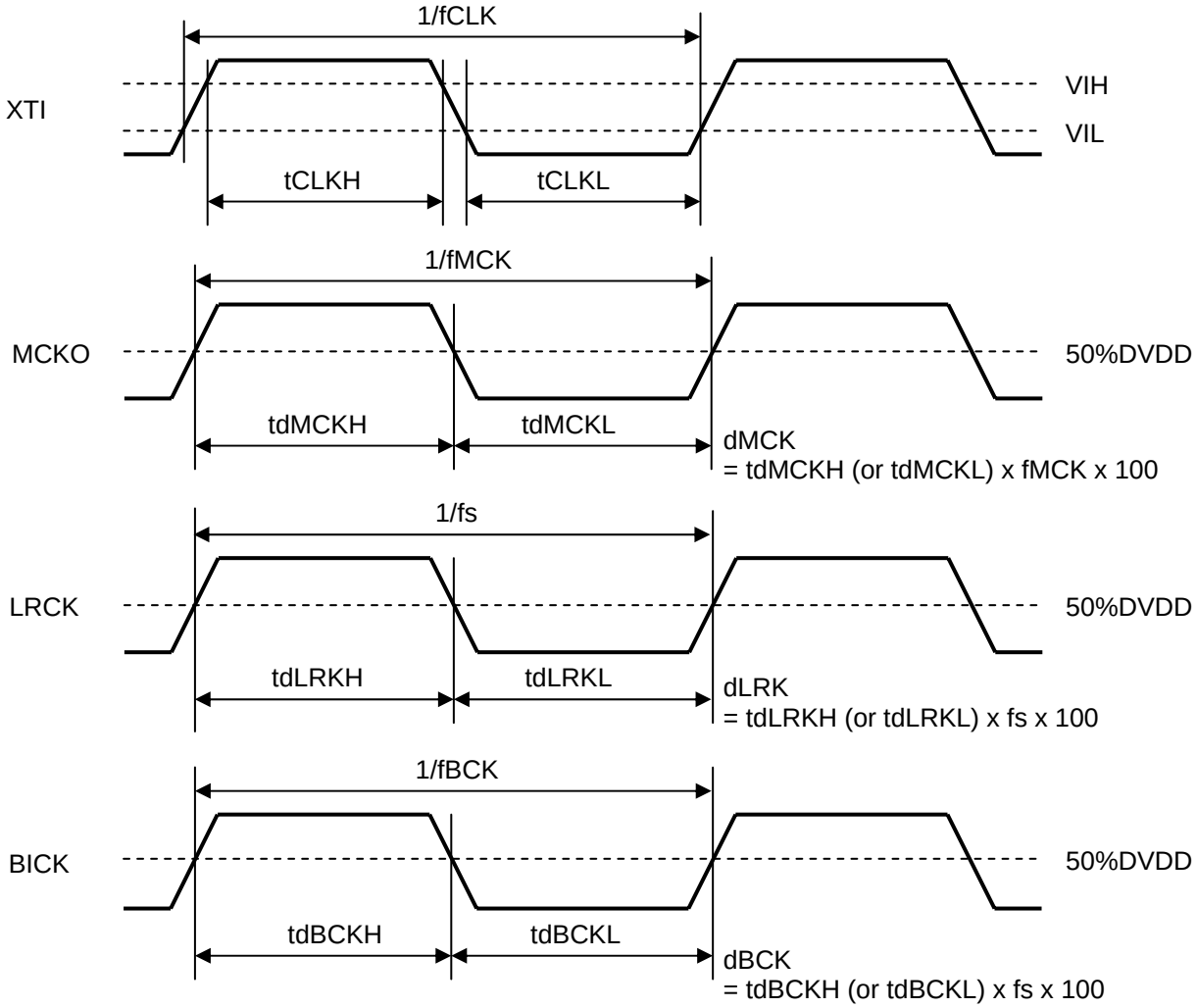


Figure 3. Clock Timing

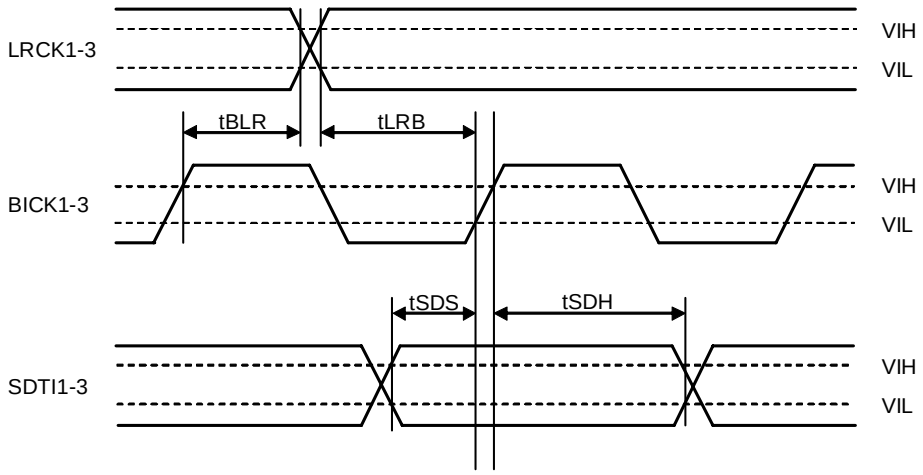


Figure 4. Audio Interface Timing (Input Port)

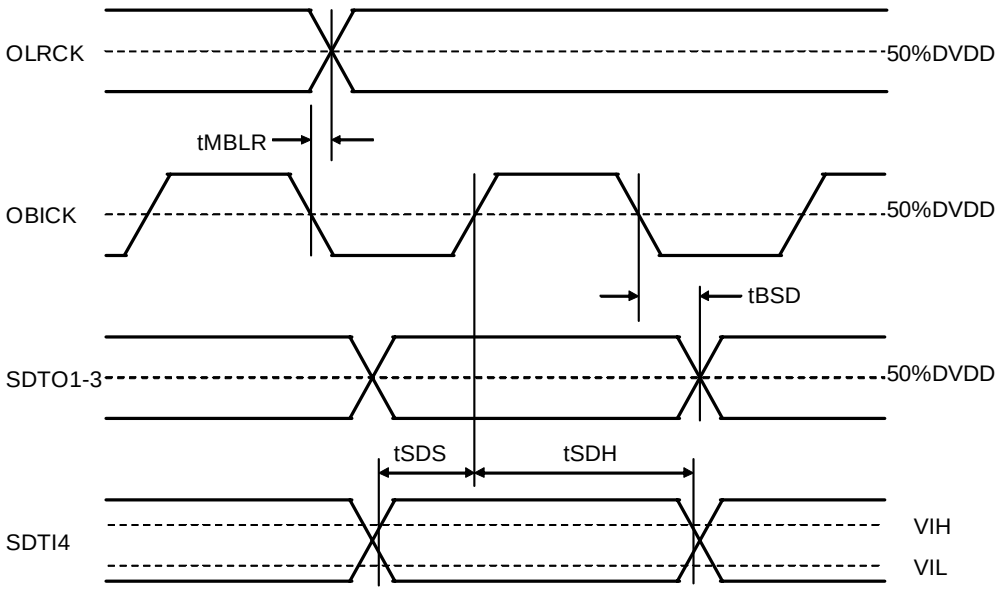


Figure 5. Audio Interface Timing (Output Port)

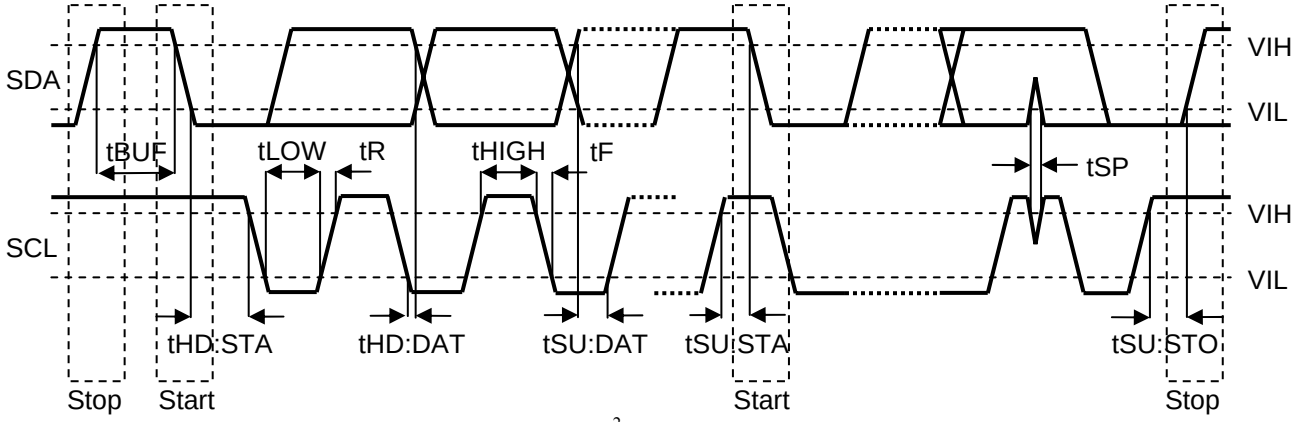


Figure 6. I^2C Bus Mode Timing

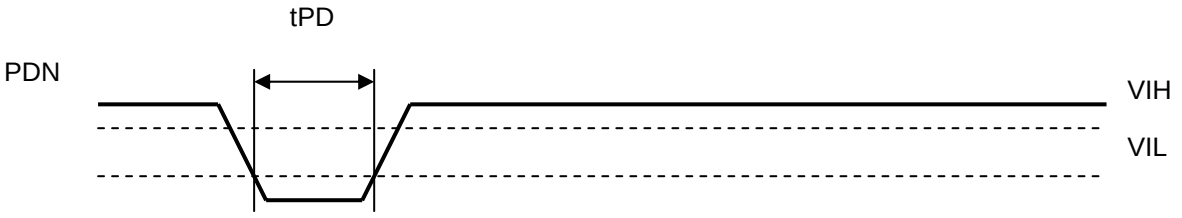
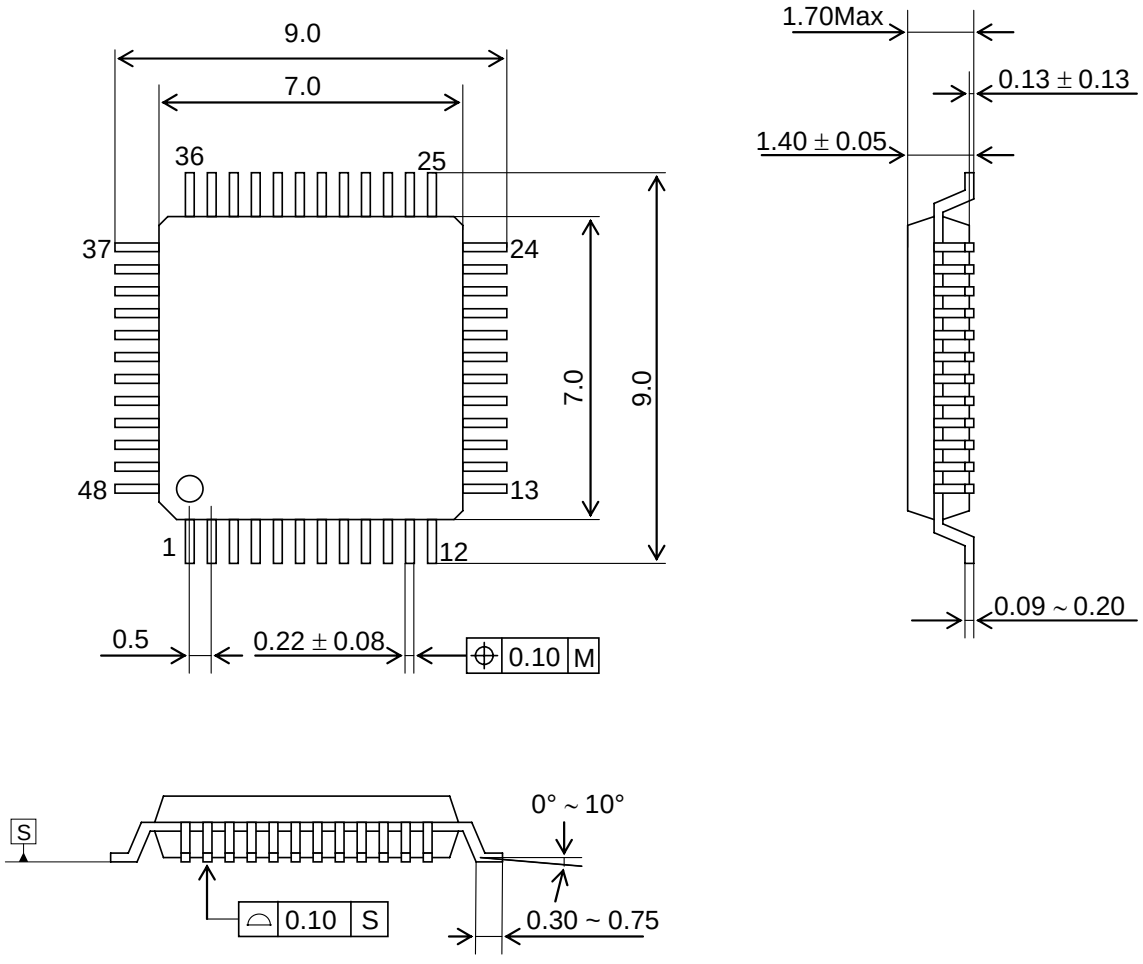


Figure 7. Power Down & Reset Timing

PACKAGE

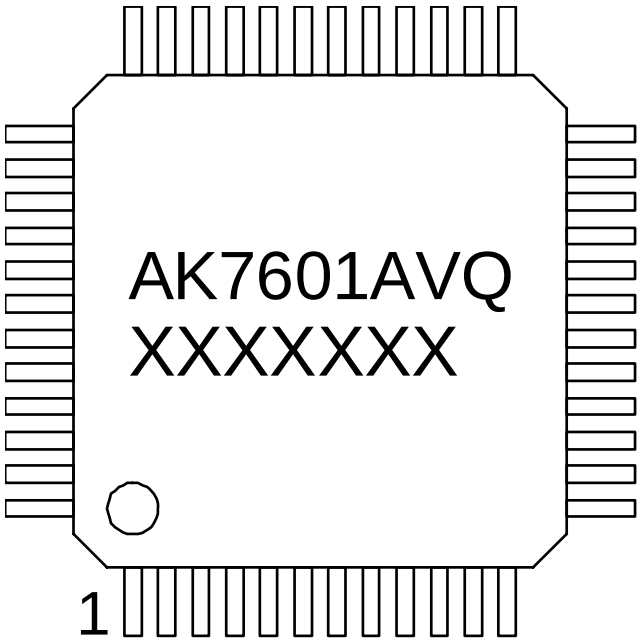
48pin LQFP(Unit: mm)



■ Materials and Lead Specification

Package: Epoxy
Lead frame: Copper
Lead-finish: Soldering plate (Pb free)

MARKING



1) Pin #1 indication
2) Date Code: XXXXXXX(7 digits)
3) Marking Code: AK7601AVQ

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