AK4126

6ch 192kHz / 24-Bit Asynchronous SRC

GENERAL DESCRIPTION

AK4126 is a 6ch digital sample rate converter (SRC). The input sample rate ranges from 8kHz to 192kHz. The output sample rate is from 8kHz to 192kHz. By using the AK4126, the system can take very simple configuration because the AK4126 has an internal PLL and does not need any master clock Then the AK4126 is suitable for the application interfacing to different sample rates like multi-channel high-end Car Audio, DVD recorder, etc.

FEATURES

1. SRC
- **6 channels input/output**
- **Asynchronous Sample Rate Converter**
- **Input Sample Rate Range (fsi): 8kHz ~ 192kHz**
- **Output Sample Rate Range (fso): 8kHz ~ 192kHz**
- **Input to Output Sample Rate Ratio: 1/6 to 6**
- **THD+N: –130dB**
- **Dynamic Range: 140dB (A-weighted)**
- **I/F format: MSB justified, LSB justified and I^2S compatible**
- **PLL for Internal Operation Clock**
- **Digital De-emphasis Filter (32kHz, 44.1kHz and 48kHz)**
- **Soft Mute Function**

2. Power Supply
- **AVDD, DVDD: 3.0 ~ 3.6V (typ. 3.3V)**

3. Ta = –40 ~ 85°C

4. Package: 64LQFP

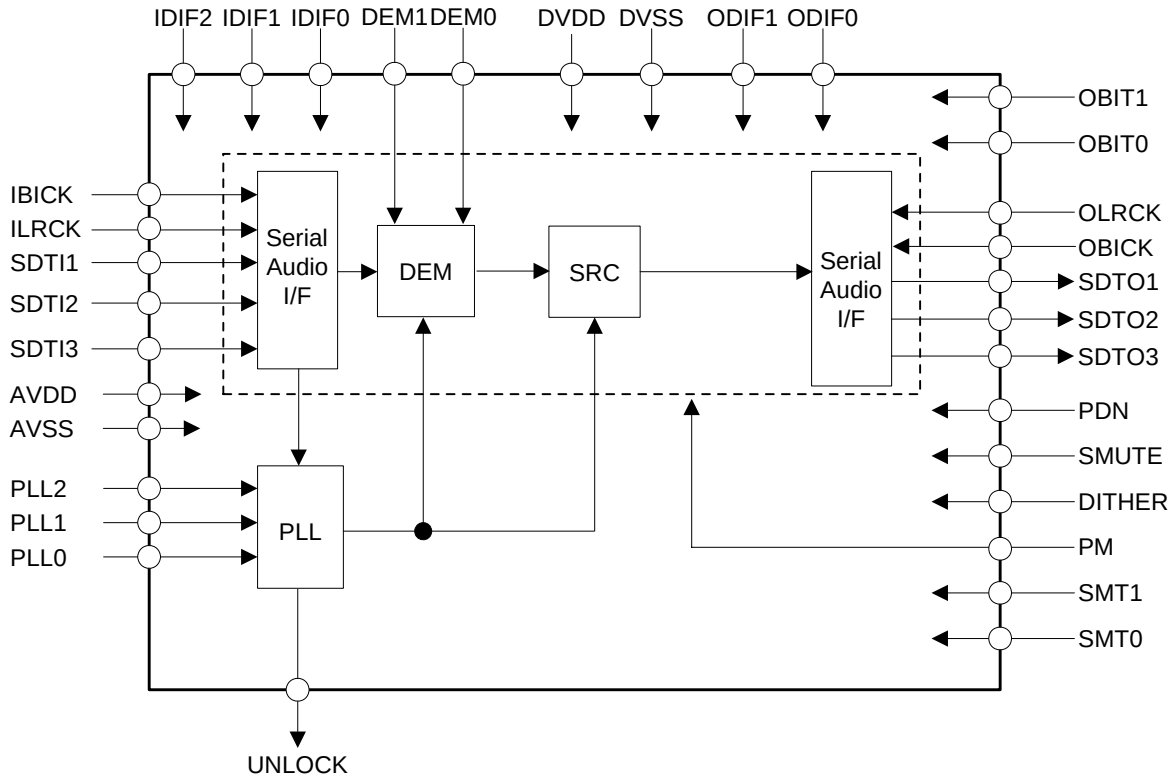


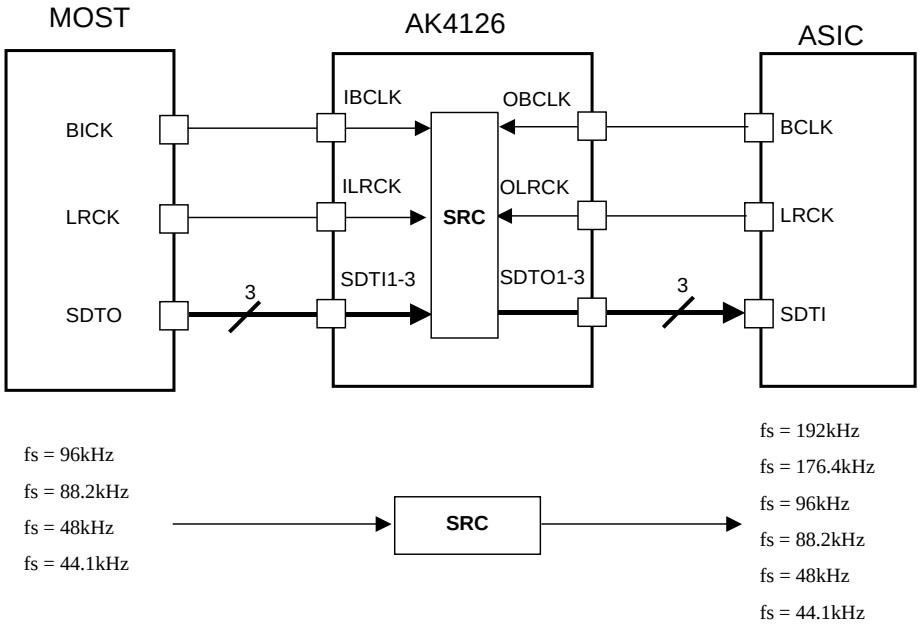
Figure 1. AK4126 Block Diagram

■ Compatibility with AK4125

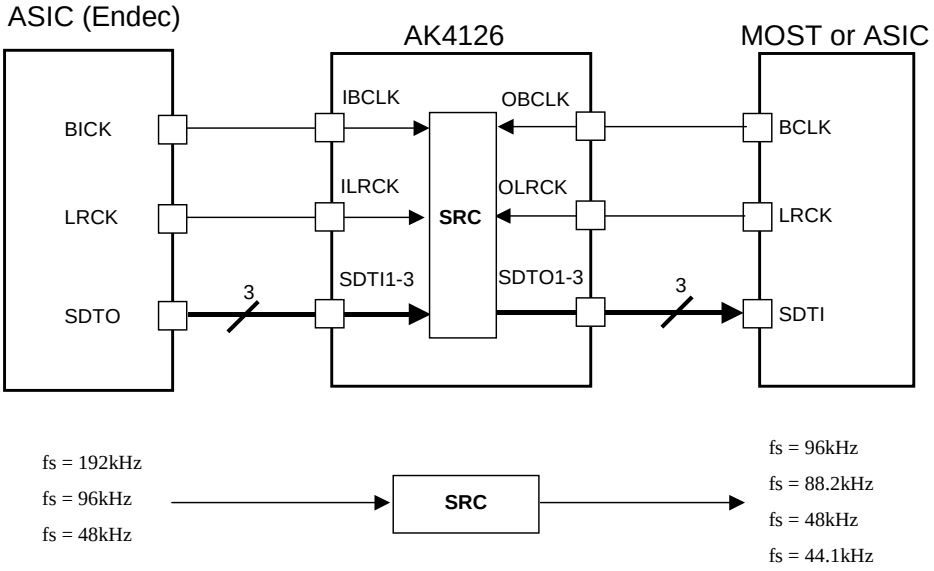
Parameter	AK4126	AK4125
Channel	6ch	2ch
Maximum Sampling Frequency	192kHz	216kHz
Maximum BICK Frequency	64fs	128fs
Bypass Mode	No	Yes
Master Mode	No	Yes
De-emphasis	Yes	No
Variable Soft Mute Cycle	Yes	No
Group Delay	typ. 57/fs	typ. 56/fs
Package	64LQFP(12mm x 12mm)	30VSOP (9.7mm x 7.6mm)

■ Application Block Circuit Example

1. Most ➔ Amp Unit



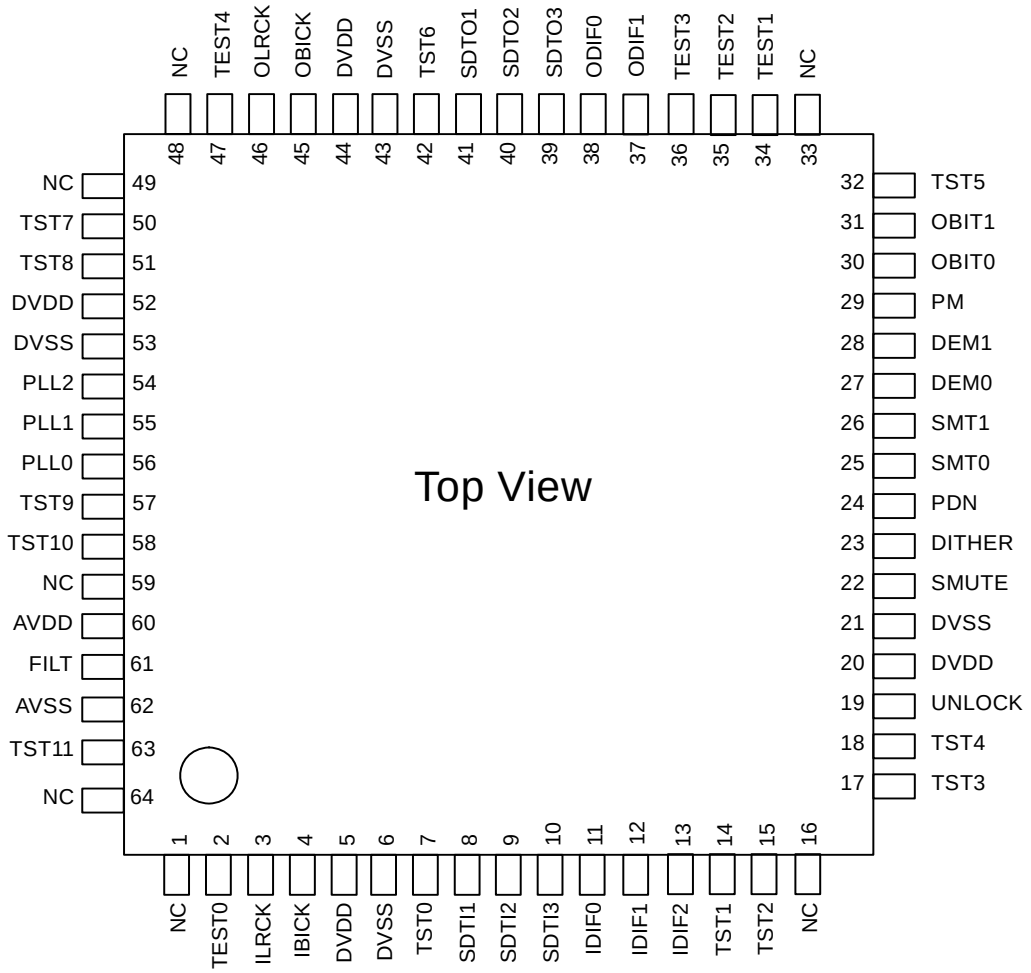
2. DVD (5.1ch) ➔ MOST or ASIC



■ Ordering Guide

AK4126VQ	–40 ~ +85°C	64LQFP (0.5mm pitch)
AKD4126	Evaluation Board for AK4126	

■ Pin Layout



PIN / FUNCTION

No.	Pin Name	I/O	Function
1, 16, 33,48, 49,59, 64	NC	-	No Connect Pin. No internal bonding. This pin must be connected to DVSS.
2	TEST0	I	TEST Pin This pin must be connected to DVSS.
3	ILRCK	I	Input Channel Clock Pin
4	IBICK	I	Audio Serial Data Clock Pin
5	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
6	DVSS	-	Digital Ground Pin
7	TST0	I	TEST Pin This pin must be connected to DVSS.
8	SDTI1	I	Audio Serial Data Input #1 Pin
9	SDTI2	I	Audio Serial Data Input #2 Pin
10	SDTI3	I	Audio Serial Data Input #3 Pin
11	IDIF0	I	Audio Interface Format #0 Pin for Input PORT
12	IDIF1	I	Audio Interface Format #1 Pin for Input PORT
13	IDIF2	I	Audio Interface Format #2 Pin for Input PORT
14	TST1	I	TEST Pin This pin must be connected to DVSS.
15	TST2	I	TEST Pin This pin must be connected to DVSS.
17	TST3	I	TEST Pin This pin must be connected to DVSS.
18	TST4	I	TEST Pin This pin must be connected to DVSS.
19	UNLOCK	O	Unlock Status Pin
20	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
21	DVSS	-	Digital Ground Pin
22	SMUTE	I	Soft Mute Pin “H” : Soft Mute, “L” : Normal Operation
23	DITHER	I	Dither Enable Pin “H” : Dither ON, “L” : Dither OFF
24	PDN	I	Power-Down Mode Pin “H”: Power up, “L”: Power down reset and initializes the control register. The AK4126 should be reset once by bringing PDN pin = “L” upon power-up.
25	SMT0	I	Soft Mute Timer Select #0 Pin
26	SMT1	I	Soft Mute Timer Select #1 Pin
27	DEM0	I	De-emphasis Control #0 Pin
28	DEM1	I	De-emphasis Control #1 Pin
29	PM	I	4ch/6ch Mode Select Pin
30	OBIT0	I	Bit Length Select #0 Pin for Output Data
31	OBIT1	I	Bit Length Select #1 Pin for Output Data

Note: All input pins should not be left floating.

PIN / FUNCTION

No.	Pin Name	I/O	Function
32	TST5	I	TEST Pin This pin must be connected to DVSS.
34	TEST1	I	TEST Pin **This pin must be connected to DVDD.**
35	TEST2	I	TEST Pin This pin must be connected to DVSS.
36	TEST3	I	TEST Pin This pin must be connected to DVSS.
37	ODIF1	I	Audio Interface Format #1 Pin for Output PORT
38	ODIF0	I	Audio Interface Format #0 Pin for Output PORT
39	SDTO3	O	Audio Serial Data Output #3 Pin for Output PORT
40	SDTO2	O	Audio Serial Data Output #2 Pin for Output PORT
41	SDTO1	O	Audio Serial Data Output #1 Pin for Output PORT
42	TST6	I	TEST Pin This pin must be connected to DVSS.
43	DVSS	-	Digital Ground Pin
44	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
45	OBICK	I	Audio Serial Data Clock Pin for Output PORT
46	OLRCK	I	Output Channel Clock Pin for Output PORT
47	TEST4	I	TEST Pin This pin must be connected to DVSS.
50	TST7	I	TEST Pin This pin must be connected to DVSS.
51	TST8	I	TEST Pin This pin must be connected to DVSS.
52	DVDD	-	Digital Power Supply Pin, 3.0 ~ 3.6V
53	DVSS	-	Digital Ground Pin
54	PLL2	I	PLL Mode Select #2 Pin
55	PLL1	I	PLL Mode Select #1 Pin
56	PLL0	I	PLL Mode Select #0 Pin
57	TST9	I	TEST Pin This pin must be connected to DVSS.
58	TST10	I	TEST Pin This pin must be connected to DVSS.
60	AVDD	-	Analog Power Supply Pin, 3.0 ~ 3.6V
61	FILT	O	PLL Loop Filter Pin
62	AVSS	-	Analog Ground Pin
63	TST11	O	TEST Pin This pin must be open.

Note: All input pins should not be left floating.

■ Handling of Unused pins

The unused digital I/O pins should be processed appropriately as below.

Classification	Pin Name	Setting
Digital	SMUTE, DITHER, PM, TEST0, TEST2 ~4, NC, TST0 ~10, SDTI1, SDTI2, SDTI3	These pins must be connected to DVSS.
	TEST1	This pin must be connected to DVDD.
	UNLOCK, SDTO1, SDTO2, SDTO3, TST11	These pins must be open.

ABSOLUTE MAXIMUM RATINGS

(AVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies:	Analog	AVDD	–0.3	4.6	V
(Note 2)	Digital	DVDD	–0.3	4.6	V
Input Current, Any Pin Except Supplies		IIN	-	±10	mA
Digital Input Voltage (Note 3)		VIND	–0.3	DVDD+0.3	V
Ambient Temperature (Power applied) (Note 4)		Ta	–40	85	°C
Storage Temperature		Tstg	–65	150	°C

Note 1. All voltages with respect to ground.
Note 2. AVSS and DVSS must be connected to the same ground.
Note 3. IDIF2-0, DEM1-0, ODIF1-0, OBIT1-0, OLRCK, OBICK, PDN, SMUTE, PM, SMT1-0, TEST4-0, TST10-0, PLL2-0, SDTI3-1, ILRCK and IBICK pins
Note 4. In case that wiring density is 100%.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS=DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies:	Analog	AVDD	3.0	3.3	3.6	V
(Note 5)	Digital	DVDD	3.0	3.3	3.6	V
	Difference	AVDD - DVDD	-0.3	0	+0.3	V

Note 1. All voltages with respect to ground.
Note 5. The power up sequence between AVDD and DVDD is not critical.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

SRC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.3V; AVSS=DVSS=0V; Signal Frequency = 1kHz; data = 24bit;
Measurement bandwidth = 20Hz ~ FSO/2; unless otherwise specified.)

Parameter	Symbol	min	typ	max	Units
SRC Characteristics:					
Resolution				24	Bits
Input Sample Rate	FSI	8		192	kHz
Output Sample Rate	FSO	8		192	kHz
THD+N (Input = 1kHz, 0dBFS, Note 6)					
FSO/FSI = 44.1kHz/48kHz		-	–130	-	dB
FSO/FSI = 48kHz/44.1kHz		-	–124	-	dB
FSO/FSI = 48kHz/192kHz		-	–133	-	dB
FSO/FSI = 192kHz/48kHz		-	–124	-	dB
Worst Case (FSO/FSI = 32kHz/176.4kHz)		-	-	–91	dB
Dynamic Range (Input = 1kHz, –60dBFS, Note 6)					
FSO/FSI = 44.1kHz/48kHz		-	136	-	dB
FSO/FSI = 48kHz/44.1kHz		-	136	-	dB
FSO/FSI = 48kHz/192kHz		-	136	-	dB
FSO/FSI = 192kHz/48kHz		-	136	-	dB
Worst Case (FSO/FSI = 48kHz/32kHz)		132	-	-	dB
Dynamic Range (Input = 1kHz, –60dBFS, A-weighted, Note 6)					
FSO/FSI = 44.1kHz/48kHz		-	140	-	dB
Ratio between Input and Output Sample Rate	FSO/FSI	1/6		6	-

Note 6. Measured by Audio Precision System Two Cascade.

FILTER CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband –0.01dB	0.985 ≤ FSO/FSI ≤ 6.000	PB	0		0.4583FSI	kHz
	0.905 ≤ FSO/FSI < 0.985	PB	0		0.4167FSI	kHz
	0.714 ≤ FSO/FSI < 0.905	PB	0		0.3195FSI	kHz
	0.656 ≤ FSO/FSI < 0.714	PB	0		0.2852FSI	kHz
	0.536 ≤ FSO/FSI < 0.656	PB	0		0.2182FSI	kHz
	0.492 ≤ FSO/FSI < 0.536	PB	0		0.2177FSI	kHz
	0.452 ≤ FSO/FSI < 0.492	PB	0		0.1948FSI	kHz
	0.357 ≤ FSO/FSI < 0.452	PB	0		0.1458FSI	kHz
	0.324 ≤ FSO/FSI < 0.357	PB	0		0.1302FSI	kHz
	0.246 ≤ FSO/FSI < 0.324	PB	0		0.0917FSI	kHz
	0.226 ≤ FSO/FSI < 0.246	PB	0		0.0826FSI	kHz
	0.1667 ≤ FSO/FSI < 0.226	PB	0		0.0583FSI	kHz
Stopband	0.985 ≤ FSO/FSI ≤ 6.000	SB	0.5417FSI			kHz
	0.905 ≤ FSO/FSI < 0.985	SB	0.5021FSI			kHz
	0.714 ≤ FSO/FSI < 0.905	SB	0.3965FSI			kHz
	0.656 ≤ FSO/FSI < 0.714	SB	0.3643FSI			kHz
	0.536 ≤ FSO/FSI < 0.656	SB	0.2974FSI			kHz
	0.492 ≤ FSO/FSI < 0.536	SB	0.2813FSI			kHz
	0.452 ≤ FSO/FSI < 0.492	SB	0.2604FSI			kHz
	0.357 ≤ FSO/FSI < 0.452	SB	0.2116FSI			kHz
	0.324 ≤ FSO/FSI < 0.357	SB	0.1969FSI			kHz
	0.246 ≤ FSO/FSI < 0.324	SB	0.1573FSI			kHz
	0.226 ≤ FSO/FSI < 0.246	SB	0.1471FSI			kHz
	0.1667 ≤ FSO/FSI < 0.226	SB	0.1020FSI			kHz
Passband Ripple		PR			±0.01	dB
Stopband Attenuation	0.985 ≤ FSO/FSI ≤ 6.000	SA	121.2			dB
	0.905 ≤ FSO/FSI < 0.985	SA	121.4			dB
	0.714 ≤ FSO/FSI < 0.905	SA	115.3			dB
	0.656 ≤ FSO/FSI < 0.714	SA	116.9			dB
	0.536 ≤ FSO/FSI < 0.656	SA	114.6			dB
	0.492 ≤ FSO/FSI < 0.536	SA	100.2			dB
	0.452 ≤ FSO/FSI < 0.492	SA	103.3			dB
	0.357 ≤ FSO/FSI < 0.452	SA	102.0			dB
	0.324 ≤ FSO/FSI < 0.357	SA	103.6			dB
	0.246 ≤ FSO/FSI < 0.324	SA	104.0			dB
	0.226 ≤ FSO/FSI < 0.246	SA	103.3			dB
	0.1667 ≤ FSO/FSI < 0.226	SA	73.2			dB
Group Delay	(Note 7)	GD	-	57	-	1/fs

Note 7. This value is the time from the rising edge of LRCK after data is input to rising edge of LRCK after data is output, when LRCK for Output data corresponds with LRCK for Input.

DC CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
High-Level Output Voltage (Iout=−400μA)	VOH	DVDD−0.4	-	-	V
Low-Level Output Voltage (Iout=400μA)	VOL	-	-	0.4	V
Input Leakage Current	Iin	-	-	±10	μA
Power Supplies					
Power Supply Current					
Normal operation (PDN pin = "H")					
FSI=FSO=48kHz: AVDD=DVDD=3.3V			48	-	mA
FSI=FSO=192kHz: AVDD=DVDD=3.3V			192	-	mA
AVDD=DVDD=3.6V				250	mA
Power down (PDN pin = "L") (Note 8)					
AVDD+DVDD			10	100	μA

Note 8. All digital input pins are held DVSS.
This value is measured after the internal SRAM is initialized by inputting "0" data to SDTI1, SDTI2, and SDTI3 during (ILRCK x 100) cycles.

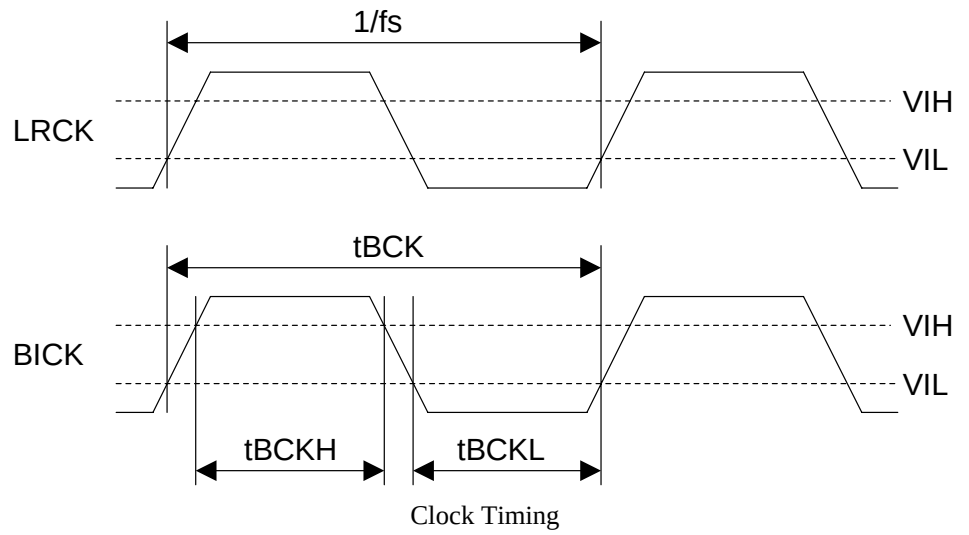
SWITCHING CHARACTERISTICS

(Ta=25°C; AVDD=DVDD=3.0 ~ 3.6V; C_L=20pF)

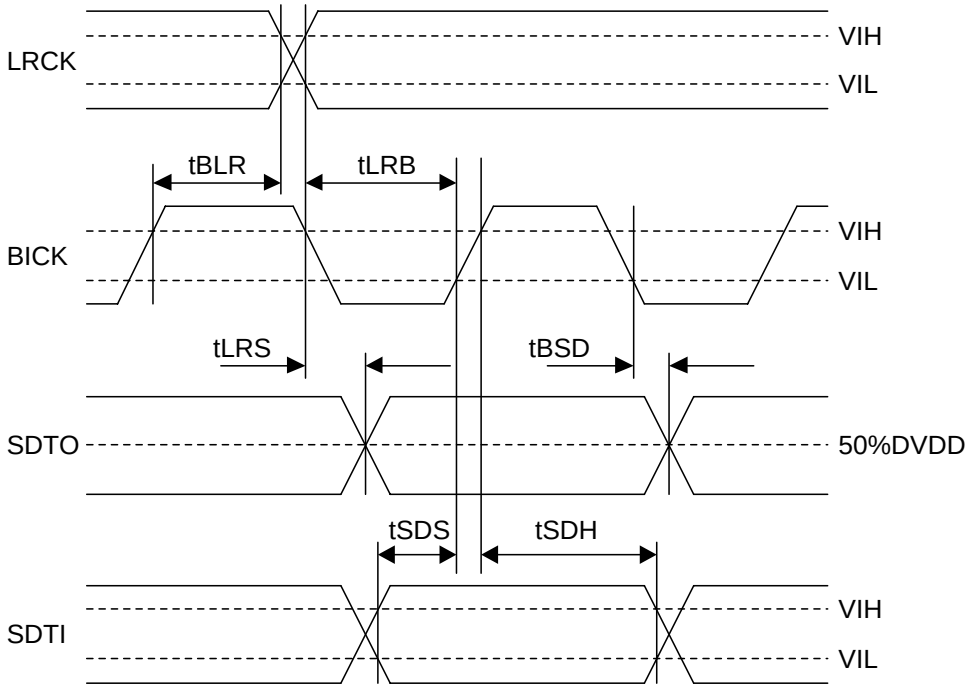
Parameter	Symbol	min	typ	max	Units
LRCK for Input data (ILRCK)					
Frequency	fs	8		192	kHz
Duty Cycle	Duty	48	50	52	%
LRCK for Output data (OLRCK)					
Frequency	fs	8		192	kHz
Duty Cycle	Duty	48	50	52	%
Audio Interface Timing					
Input PORT					
IBICK Period	tBCK	1/64fs			ns
IBICK Pulse Width Low	tBCKL	27			ns
Pulse Width High	tBCKH	27			ns
ILRCK Edge to IBICK "↑" (Note 9)	tLRB	15			ns
IBICK "↑" to ILRCK Edge (Note 9)	tBLR	15			ns
SDTI Hold Time from IBICK "↑"	tSDH	15			ns
SDTI Setup Time to IBICK "↑"	tSDS	15			ns
Output PORT					
OBICK Period	tBCK	1/64fs			ns
OBICK Pulse Width Low	tBCKL	27			ns
Pulse Width High	tBCKH	27			ns
OLRCK Edge to OBICK "↑" (Note 9)	tLRB	20			ns
OBICK "↑" to OLRCK Edge (Note 9)	tBLR	20			ns
OLRCK to SDTO (MSB) (Except I^2S mode)	tLRS			20	ns
OBICK "↓" to SDTO	tBSD			20	ns
Reset Timing					
PDN Pulse Width (Note 10)	tPD	150			ns

Note 9. BICK rising edge must not occur at the same time as LRCK edge.
Note 10. The AK4126 can be reset by bringing the PDN pin = "L".

■ Timing Diagram

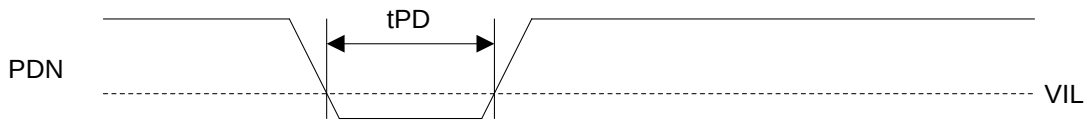


Clock Timing



Audio Interface Timing

Note: BICK shows IBICK and OBICK. LRCK shows ILRCK and OLRCK. SDTI shows SDTI1, SDTI2 and SDTI2. SDTO shows SDTO1, SDTO2 and SDTO3.



Power Down & Reset Timing

OPERATION OVERVIEW

■ System Clock & Audio Interface Format for Input PORT

The input port works in slave mode. The clocks supply ILRCK and IBICK externally. An internal system clock is created by the internal PLL using ILRCK (Mode 0 ~ 2 of Table 2) or IBICK (Mode 4, 5, 7of Table 2). The PLL2-0 pins and IDIF2-0 pins select the PLL mode. The PLL2-0 pins and IDIF2-0 pins should be controlled when PDN pin = "L".

The IDIF2-0 pins select the audio interface format for the input port. The audio data is MSB first, 2's complement format. The SDTI is latched on the rising edge of IBICK. Select the audio interface format when PDN pin = "L". The audio interface format of SDTI1, SDTI2 and SDTI3 becomes the same setting. The maximum input frequency of IBICK is 64fsi.

Mode	IDIF2	IDIF1	IDIF0	SDTI Format	IBICK Frequency
0	L	L	L	16bit, LSB justified	≥ 32fsi
1	L	L	H	20bit, LSB justified	≥ 40fsi
2	L	H	L	24/20bit, MSB justified	≥ 48fsi
3	L	H	H	24/16bit, I^2S Compatible	≥ 48fsi or 32fsi
4	H	L	L	24bit, LSB justified	≥ 48fsi
5	H	L	H	Reserved	
6	H	H	L	Reserved	
7	H	H	H	Reserved	

Table 1. Input Audio Interface Format (Input PORT)

Mode	PLL2	PLL1	PLL0	ILRCK Freq	IBICK Freq	SMUTE (Note 14)
0	L	L	L	8k ~ 96kHz	Depending on IDIF2-0 (Note 12)	Manual
1	L	L	H	8k ~ 192kHz		
2	L	H	L	16k ~ 192kHz (Note 11)		Semi-Auto
3	L	H	H	Reserved		
4	H	L	L	8k ~ 192kHz (Note 12)	32fsi (Note 13)	Manual
5	H	L	H		64fsi	
6	H	H	L	Reserved		
7	H	H	H	8k ~ 192kHz (Note 12)	64fsi	Semi-Auto

Note 11. PLL lock rage is changed by the value of R and C connected FILT pin. Refer to "PLL Loop Filter".
Note 12. The IBCIK must be continuous except when the clocks are changed.
Note 13. IBCIK = 32fsi is supported only 16bit LSB justified and I^2S Compatible.
Note 14. Refer to "Soft Mute Operation" for Manual mode and Semi-Auto mode.

Table 2. PLL Setting (Input PORT)

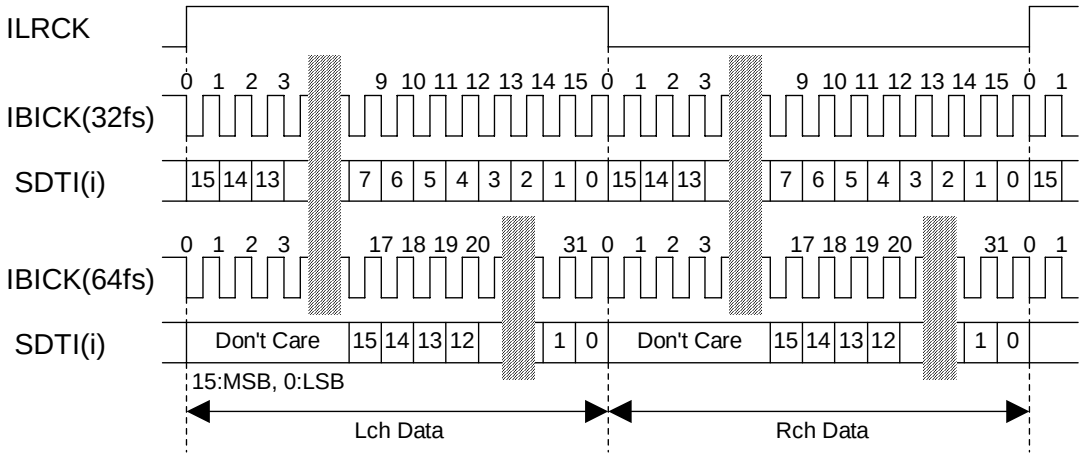


Figure 2. Mode 0 Timing

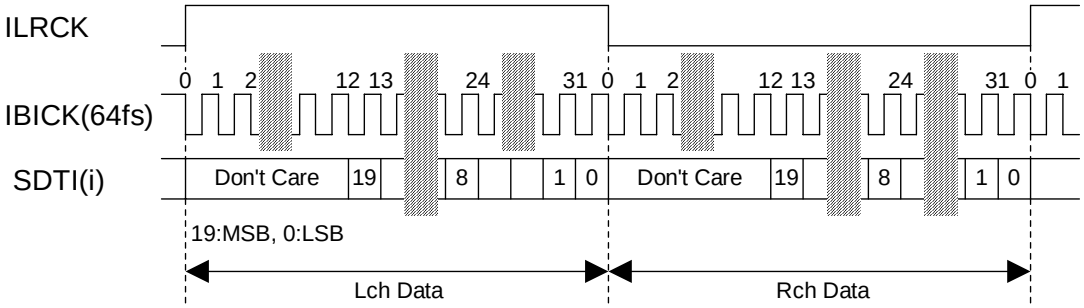


Figure 3. Mode 1 Timing

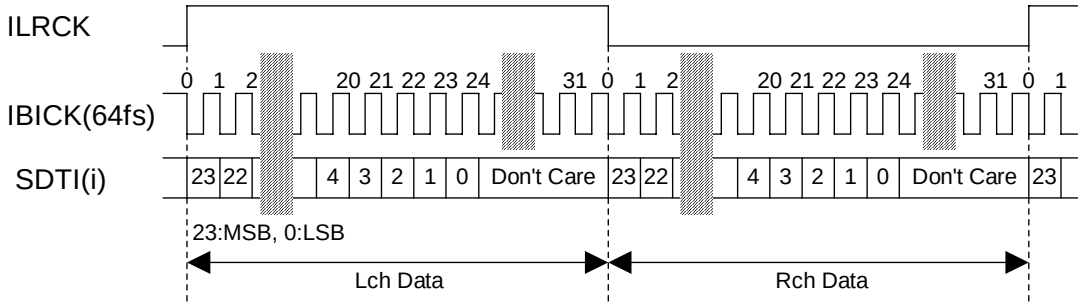


Figure 4. Mode 2 Timing (24bit MSB)

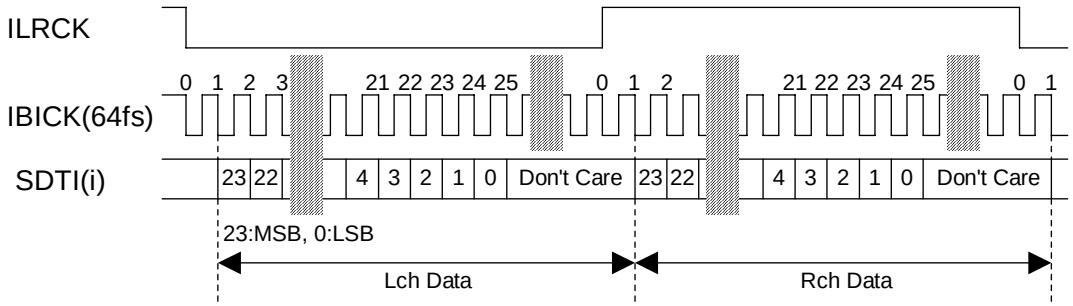


Figure 5. Mode 3 Timing (24bit I^2S)

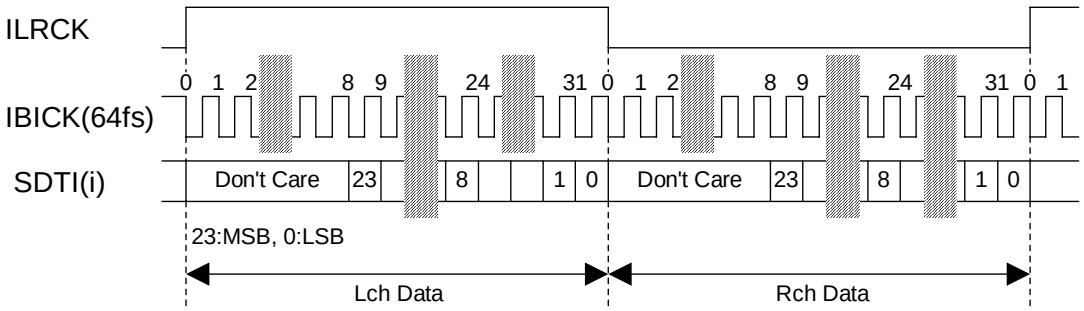


Figure 6. Mode 4 Timing

Note: SDTI shows SDTI1, SDTI2 and SDTI3.

■ System Clock & Audio Interface Format for Output PORT

The output port works in slave mode. The clocks supply OLRCK and OBICK externally. The ODIF1-0 pins and OBIT1-0 pins select the audio interface format for the output port. The audio data is MSB first, 2's complement format. The SDTO is clocked out on the falling edge of OBICK. Select the audio interface format when PDN pin = "L". The audio interface format of SDTO1, SDTO2 and SDTO3 becomes the same setting. The maximum input frequency of OBICK is 64fso.

Mode	ODIF1	ODIF0	SDTO Format
0	L	L	LSB justified
1	L	H	(Reserved)
2	H	L	MSB justified
3	H	H	I^2S Compatible

Table 3. Output Audio Interface Format 1 (Output PORT)

Mode	OBIT1	OBIT0	SDTO	OBICK Frequency	
				MSB justified, I^2S	LSB justified
0	L	L	16bit	≥ 32fso	64fso
1	L	H	18bit	≥ 36fso	
2	H	L	20bit	≥ 40fso	
3	H	H	24bit	≥ 48fso	

Table 4. Output Audio Interface Format 2 (Output PORT)

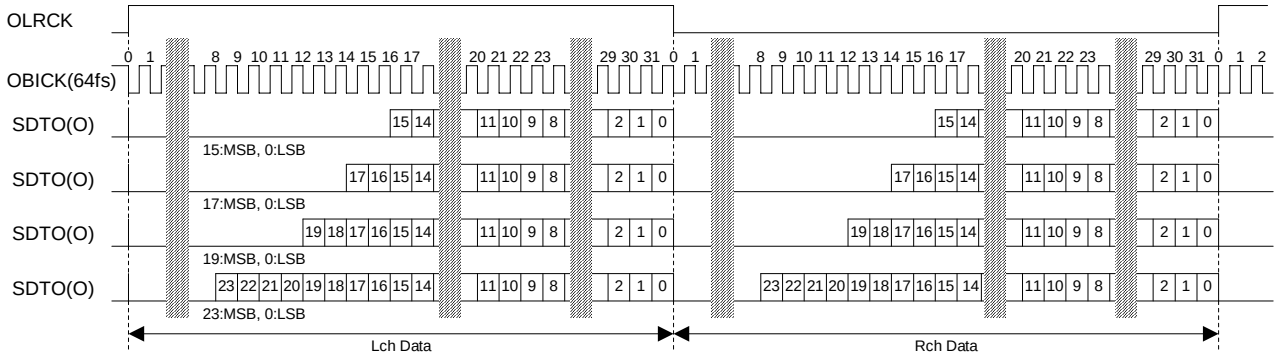


Figure 7. LSB Timing

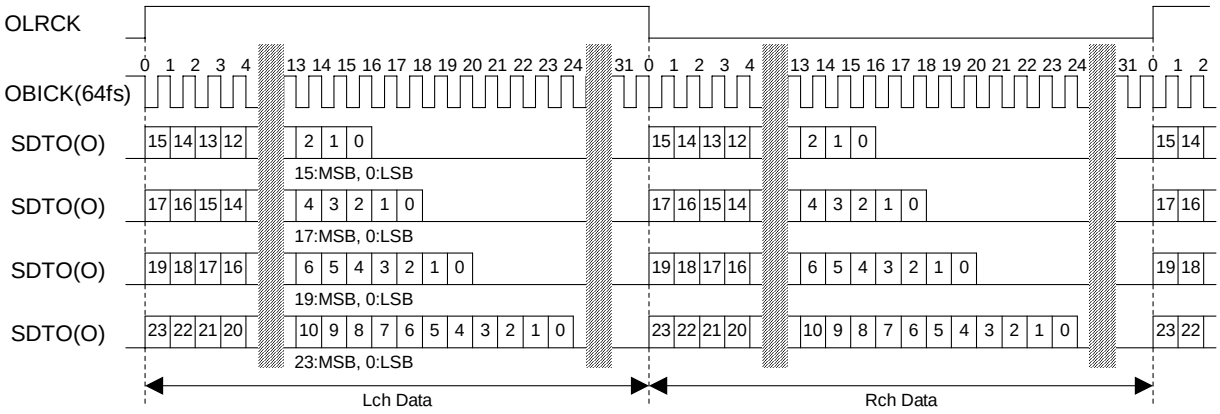


Figure 8. MSB Timing

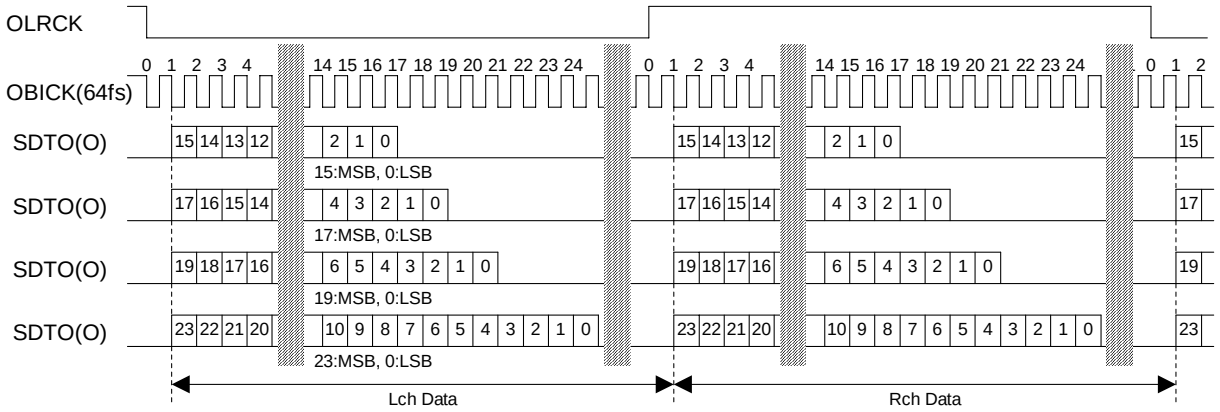


Figure 9. I^2S Compatible Timing

Note: SDTO shows SDTO1, SDTO2 and SDTO3.

■ 4-channel Mode

The AK4126 has 4-channel mode to reduce power supply current when using four channels in six channels. When PM pin is set to "H", four channels (SDTI1→ SDTO1 and SDTI2 → SDTO2) in six channels work, and other 2 channels (SDTI3 → SDTO3) are powered-down (SDTO3 outputs "L".).

PM pin	Mode
L	6-channel mode
H	4-channel mode

Table 5. Channel Mode Setting

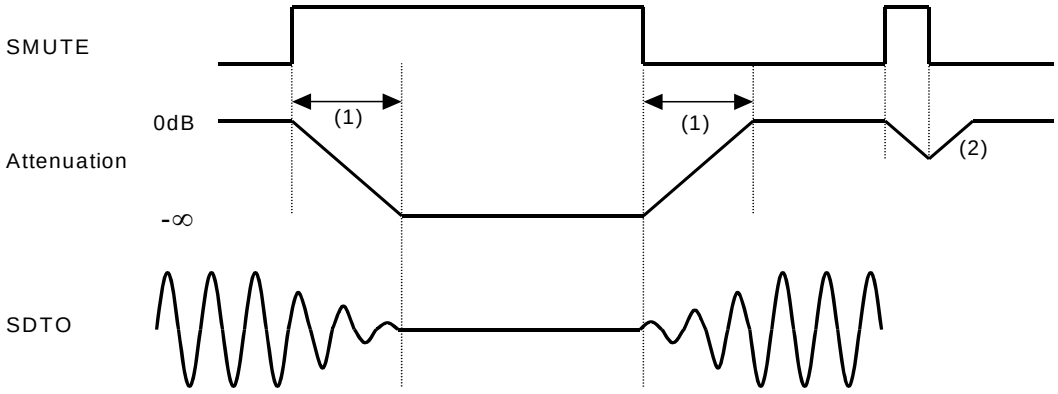
■ Soft Mute Operation

1. Manual mode

The soft mute operation is performed in the digital domain of the SRC output. The soft mute can be controlled by SMUTE pin. When SMUTE pin goes "H", all the SRC output data are attenuated by –∞ during 1024 OLRCK cycles (@ SMT1 pin = "L" and SMT0 pin = "L"). When the SMUTE pin goes "L" the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 OLRCK cycles (@ SMT1 pin = "L" and SMT0 pin = "L"). If the soft mute is cancelled before mute state after starting of the operation, the attenuation is discontinued and returned to 0dB by the same cycles. The soft mute is effective for changing the signal source. Soft mute cycle is selected by SMT1-0 pins. SMT1-0 pins must not be changed during soft mute transition.

SMT1pin	SMT0 pin	Period	fso=48kHz	fso=96kHz	fso=192kHz
L	L	1024/fso	21.3ms	10.7ms	5.3ms
L	H	2048/fso	42.7ms	21.3ms	10.7ms
H	L	4096/fso	85.3ms	42.7ms	21.3ms
H	H	8192/fso	170.7ms	85.3ms	42.7ms

Table 6. Soft Mute Cycle Setting



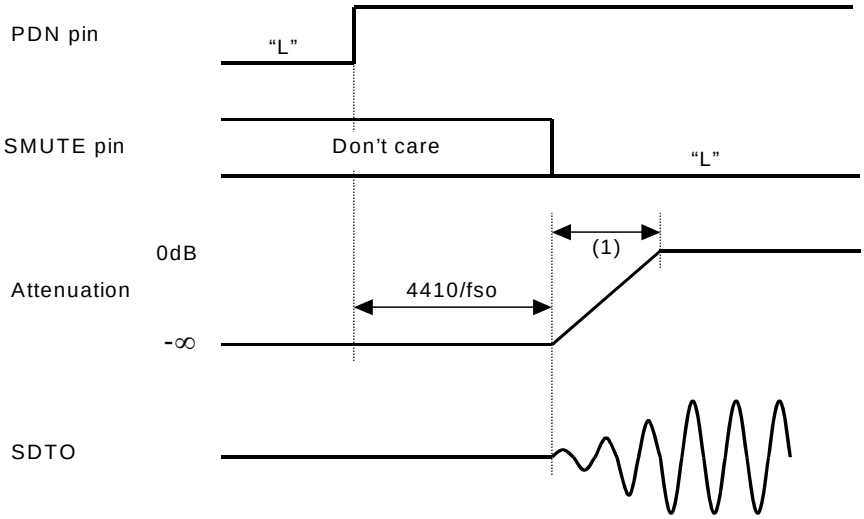
Note: SDTO shows SDTO1, SDTO2 and SDTO3.

(1) The soft mute cycle is selected by SMT1-0 pins. (See Table 6) The output data is attenuated by –∞ during the soft mute cycle.
(2) If the soft mute is cancelled before attenuating to –∞ after starting the operation, the attenuation is discontinued and returned to 0dB by the same number of clock cycles.

Figure 10. Soft Mute Function (Manual Mode)

2. Semi-Auto mode

The soft mute is cancelled automatically by the setting of PLL2-0 pins (refer to Table 2), after the AK4126 detects the rising edge (PDN pin = "L" → "H") and the mute is continued during 4410/fso=100ms@fso=44.1kHz. After PDN pin = "L" → "H" and when SMUTE pin is "H", the mute is not cancelled.



Note: SDTO shows SDTO1, SDTO2 and SDTO3.

(1) The output data is attenuated by –∞ during the soft mute cycle (See Table 6)

Figure 11. Soft Mute Function (Semi-Auto Mode)

■ Dither

The AK4126 includes the dither circuit. The dither circuit adds the dither to the LSB of all the output data set with the OBIT1-0 pins by DITHER pin = "H".

■ De-emphasis Filter

The AK4126 includes a digital de-emphasis filter (tc = 50/15μs) via an IIR filter. This filter corresponds to three frequencies (32kHz, 44.1kHz and 48kHz). This setting is done via DEM1-0 pins (See Table 7), and it is applied to all input data.

DEM1pin	DEM0 pin	Mode
L	L	44.1kHz
L	H	OFF
H	L	48kHz
H	H	32kHz

Table 7. De-emphasis Filter Setting

■ System Reset

Bringing the PDN pin = “L” sets the AK4126 power-down mode and initializes the digital filter. The AK4126 should be reset once by bringing PDN pin = “L” upon power-up. When PDN pin = “L”, the SDTO output is “L”. The SDTO valid time is 100ms. Until then, the SDTO outputs “L”. (SDTO shows SDTO1, SDTO2 and SDTO3. SDTI shows SDTI1, SDTI2 and SDTI3.)

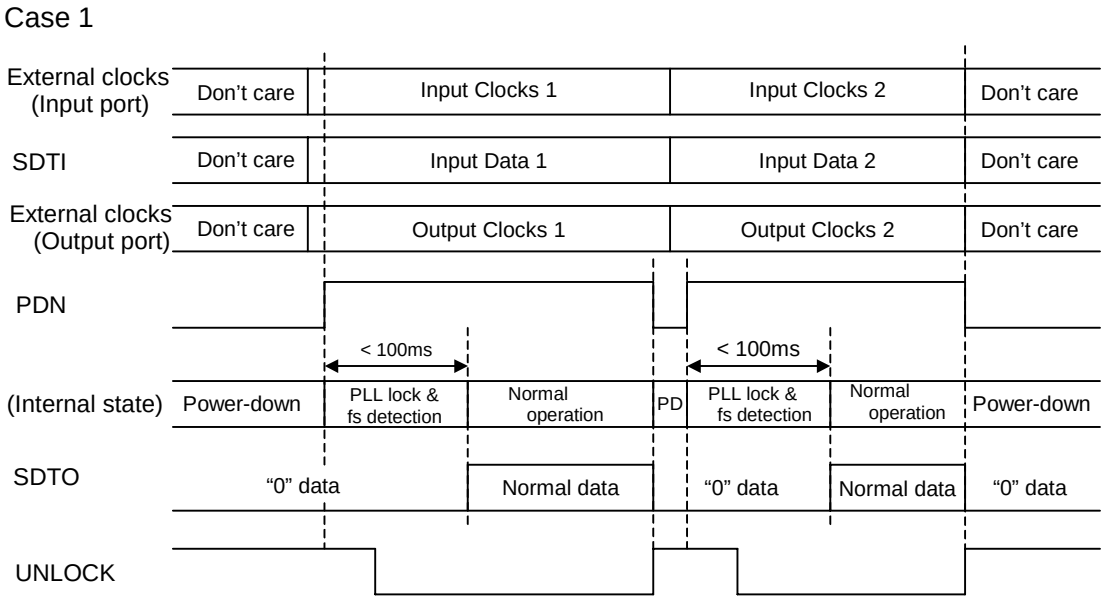


Figure 12. System Reset

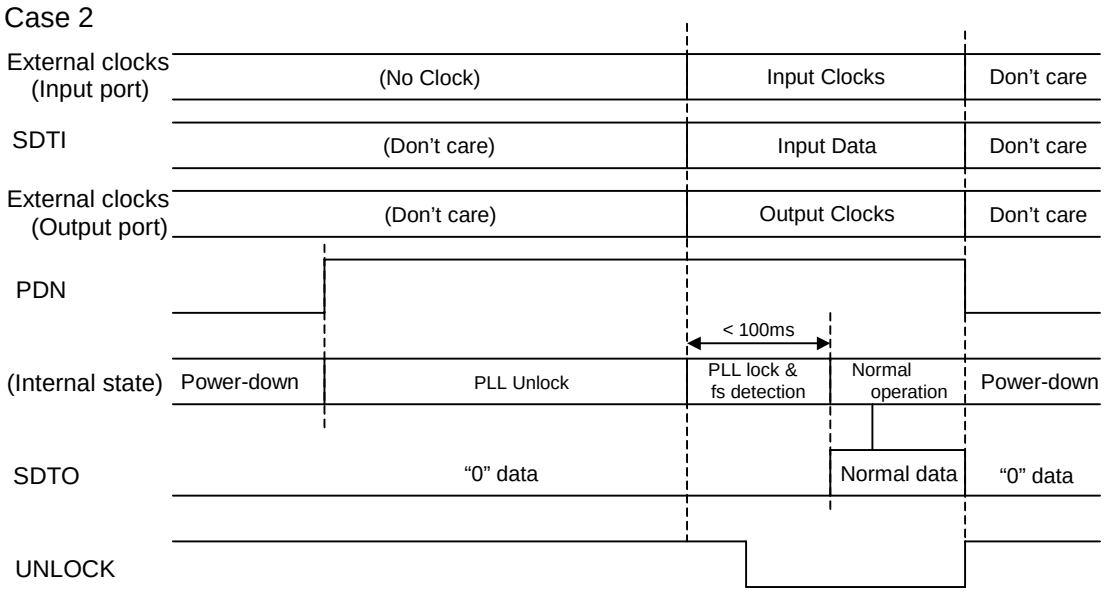
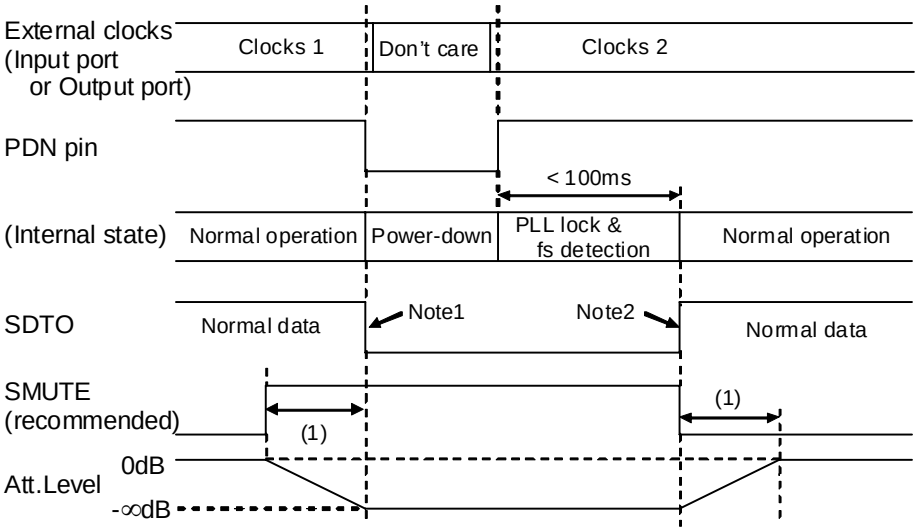


Figure 13. System Reset 2

■ Internal Reset Function for Clock Change

The change of the clock supplied to the AK4126 is shown in Figure 14. SDTO shows SDTO1, SDTO2 and SDTO3.



(1) Soft mute cycle. (See Table 6)
E.g. SMT1 pin = "L", SMT0 pin = "L", fso = 48kHz
Soft mute cycle: 1024/fso = 21.3ms

Note 1. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" from GD before PDN pin goes "L", which will cause the data on SDTO to remain "0". SMUTE can also remove this clicking noise.

Note 2. The data on SDTO may cause a clicking noise. To prevent this, set SDTI to "0" for 1024/fso+100ms or more from the timing PDN pin changes to "H" while the SMUTE pin = "H".

Note 3. When the PDN pin is not used for this clock change, a distorted signal may output for about 10ms ~ 100ms (typ) after changing clocks.

Figure 14. Sequence of Changing Clocks

■ UNLOCK pin

The UNLOCK pin outputs "L" when the internal PLL is locked. When the internal PLL is unlocked, the UNLOCK pin outputs "H". When PDN pin = "L", the UNLOCK pin outputs "H".

■ PLL Loop Filter

The C1 and R should be connected in series and attached between FILT pin and AVSS in parallel with C2. (See Figure 15, Table 8 and Table 9) Please be careful the noise onto the FILT pin. When using IBICK, the value of an external element doesn't depend on the IBICK input frequency.

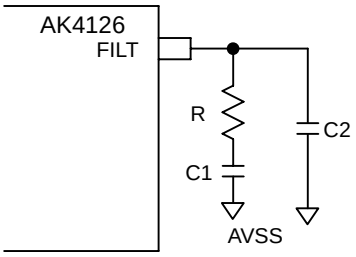


Figure 15. PLL Loop Filter

1. When using ILRCK

PLL2	PLL1	PLL0	ILRCK	R [Ω]	C1 [μF]	C2 [nF]
L	L	L	8k ~ 96kHz	1.8k ± 5%	0.68 ± 30%	0.68 ± 30%
L	L	H	8k ~ 192kHz	1k ± 5%	1.0 ± 30%	2.2 ± 30%
			16k ~ 192kHz	1.5k ± 5%	0.68 ± 30%	0.68 ± 30%
L	H	L	8k ~ 192kHz	1k ± 5%	1.0 ± 30%	2.2 ± 30%
			16k ~ 192kHz	1.5k ± 5%	0.68 ± 30%	0.68 ± 30%

Table 8. PLL Loop Filter (ILRCK Mode)

- Note. Smaller value can be selected for the capacitors (C1, C2) in case of ILRCK range from 16kHz to 192kHz.
- Note. Tolerance of R, C1, and C2 includes the temperature characteristics.

2. When using IBICK

PLL2	PLL1	PLL0	ILRCK	R [Ω]	C1 [μF]	C2 [nF]
H	x	x	8k ~ 192kHz	470 ± 5%	0.22 ± 30%	1.0 ± 30%

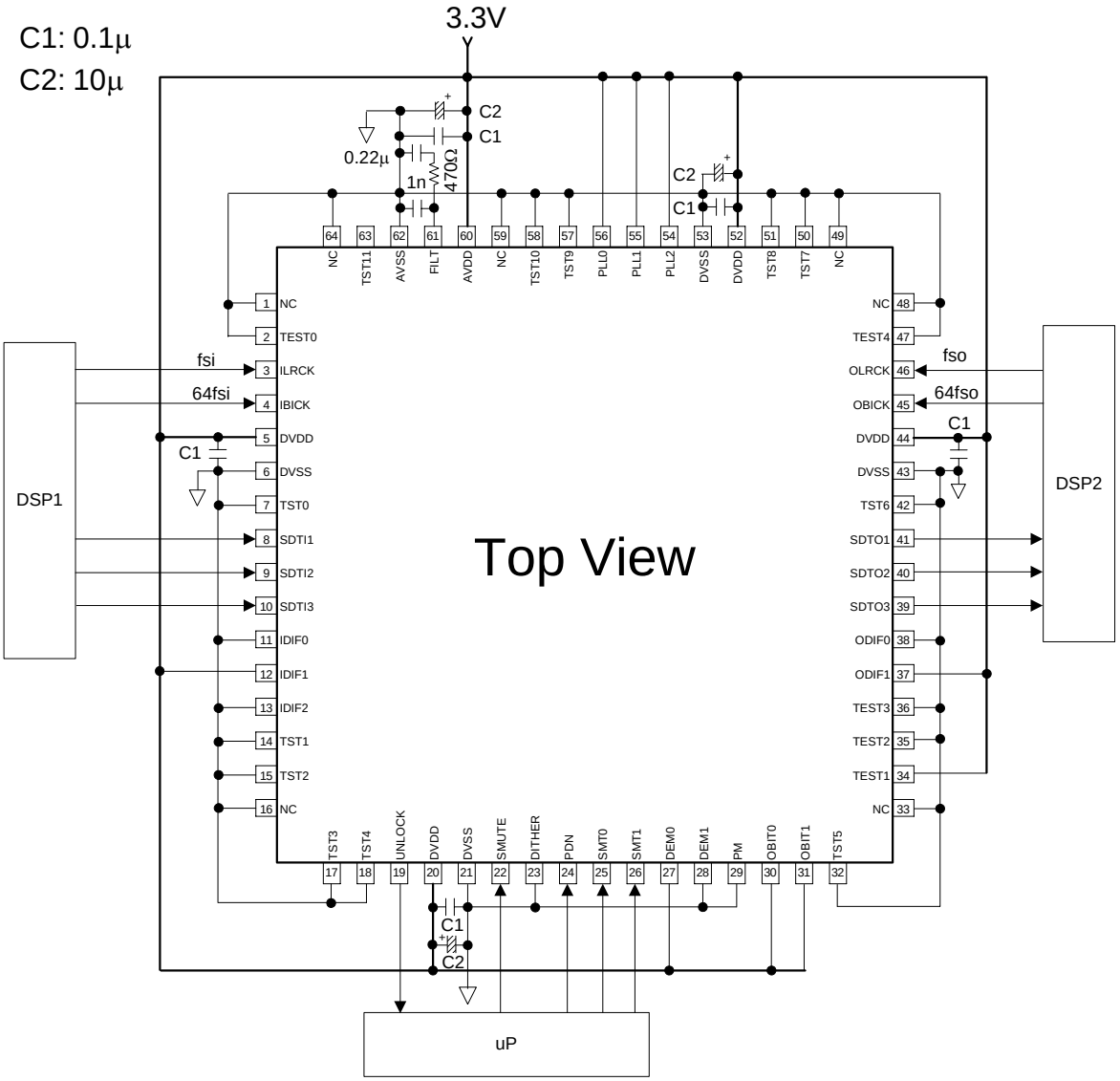
Table 9. PLL Loop Filter (IBICK Mode, “x”: Don’t care)

- Note. The IBCIK must be continuous except when the clocks are changed.
- Note. IBCIK = 32fsi is supported only 16bit LSB justified and I^2S Compatible.
- Note. Tolerance of R, C1, and C2 includes the temperature characteristics.

SYSTEM DESIGN

Figure 16 shows the system connection diagram. An evaluation board is available which demonstrates application circuits, the optimum layout, power supply arrangements and measurement results.

- Input PORT: Slave mode, IBICK lock mode (64fsi), 24 bit MSB justified
- Output PORT: Slave mode, 24 bit MSB justified
- Dither = OFF, De-emphasis = OFF, PM = 6ch mode



Notes:

- All digital input pins should be not left floating.
- AVSS and DVSS must be connected to the same ground plane.

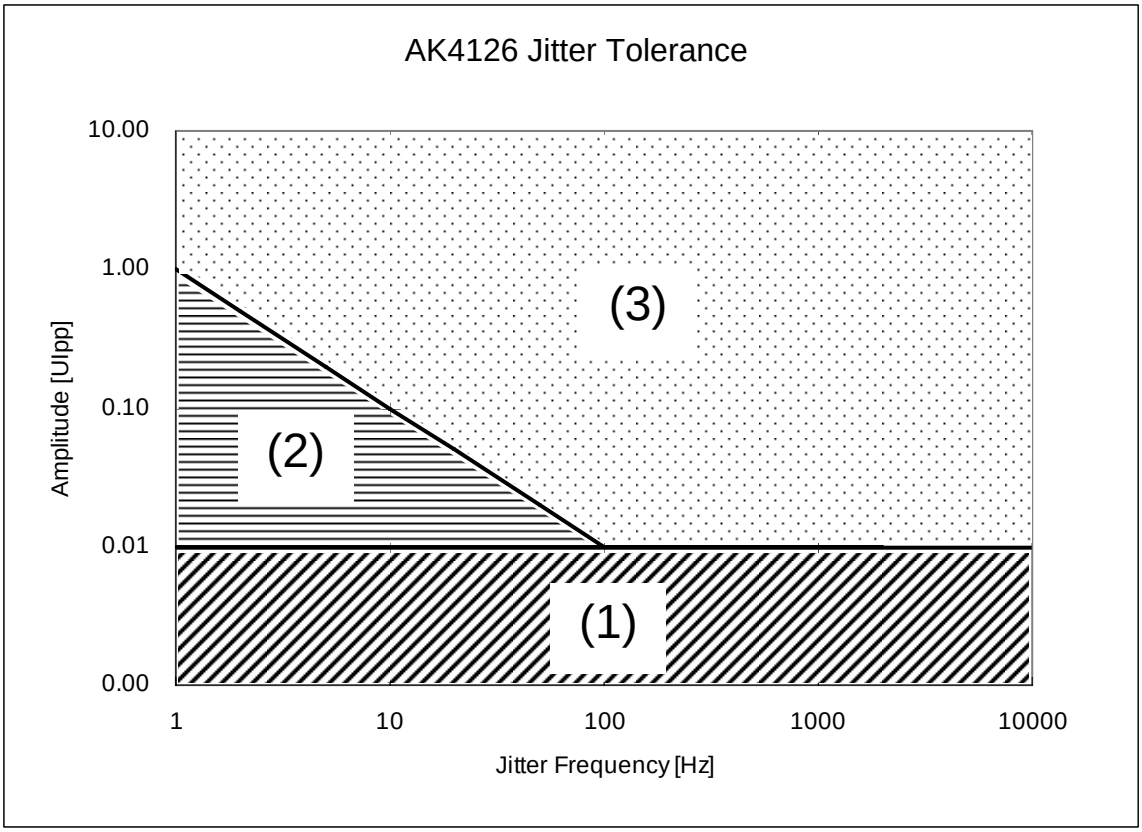
Figure 16. Typical Connection Diagram

1. Grounding and Power Supply Decoupling

The AK4126 requires careful attention to power supply and grounding arrangements. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical**. AVSS and DVSS must be connected to the same ground plane.** Decoupling capacitors should be as near to the AK4126 as possible, with the small value ceramic capacitor being the nearest.

2. Jitter Tolerance

Figure 17 shows the jitter tolerance to ILRCK and IBICK for AK4126. The jitter frequency and the jitter amplitude shown in Figure 17 define the jitter quantity. When the jitter amplitude is 0.01Uipp or less, the AK4126 operate normally regardless of the jitter frequency.



(1) Normal operation
(2) There is a possibility that the distortion degrades. (It may degrade up to about −50dB.)
(3) There is a possibility that the output data is lost.

Note:
- When PLL2-0 = “L/L/L”, “L/L/H”, “L/H/L”, the jitter amplitude is for ILRCK and 1UI (Unit Interval) is one cycle of ILRCK. When FSI = 48kHz, 1UI is 1/48kHz = 20.8μs.
- When PLL2-0 = “H/*/*” (*: Don’t care), the jitter amplitude is for IBICK and 1UI (Unit Interval) is one cycle of IBICK. When FSI = 48kHz, 1UI is 1/(64 x 48kHz) = 326ns.

Figure 17. Jitter Tolerance

Tracking to the Input Sampling Frequency

When the ILRCK is generated by an external PLL, it may take a time to settle after changing the input sampling frequency because the response of an external PLL to the frequency change is slow. AK4126 operates normally up to 23%/sec speed and the output data becomes incorrect at the speed of the frequency change over 23%/sec.

3. Digital Filter Response Example

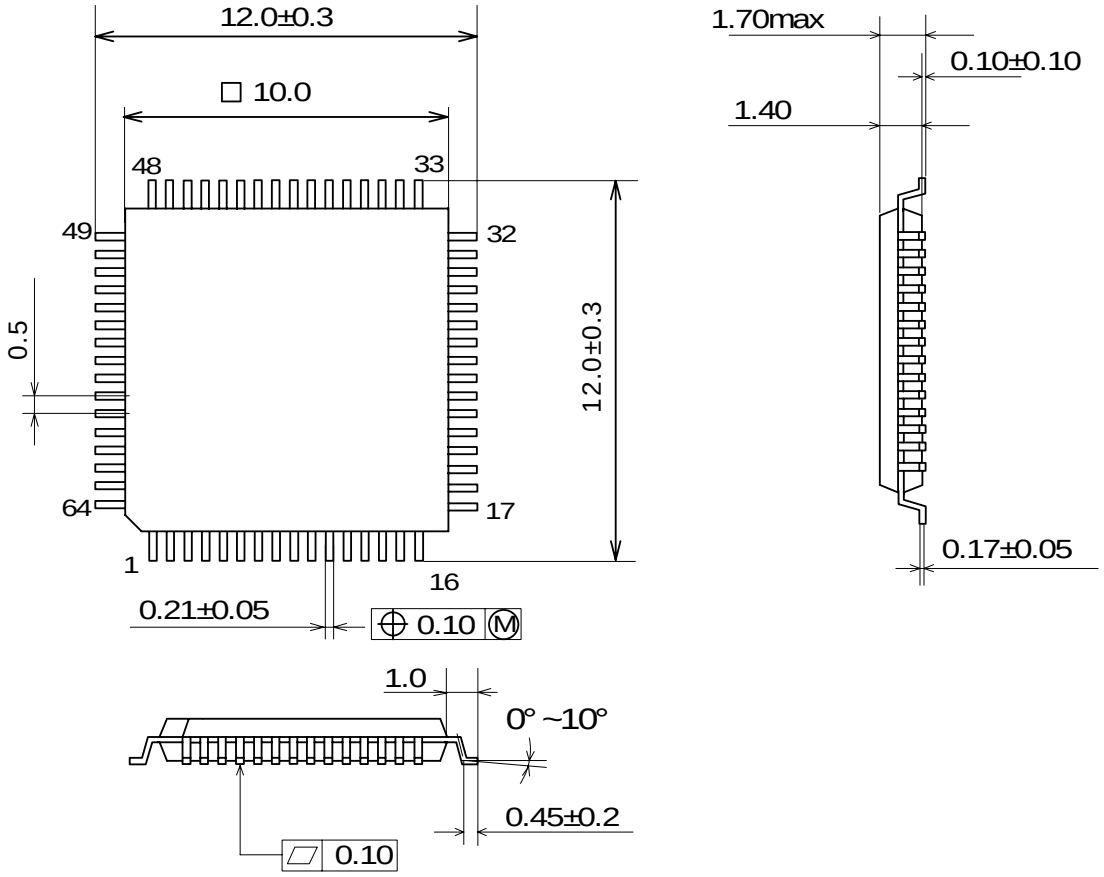
Table 10 shows the examples of digital filter response performed by the AK4126.

Ratio	FSO/FSI [kHz]	Passband [kHz]	Stopband [kHz]	Stopband Attenuation [dB]	Gain [dB]
4.000	192/48.0	22.000	26.000	–121.2	–0.01@ 20k
1.000	48.0/48.0	22.000	26.000	–121.2	–0.01@ 20k
0.919	44.1/48.0	20.000	24.100	–121.4	–0.01@ 20k
0.725	32.0/44.1	14.088	17.487	–115.3	–0.01@ 14.5k
0.667	32.0/48.0	13.688	17.488	–116.9	–0.19@ 14.5k
0.544	48.0/88.2	19.250	26.232	–114.6	–0.03@ 20k
0.500	48.0/96.0	20.900	27.000	–100.2	–0.01@ 20k
0.500	44.1/88.2	19.202	24.806	–100.2	–0.08@ 20k
0.459	44.1/96.0	18.700	25.000	–103.3	–0.23@ 20k
0.363	32.0/88.2	12.863	18.665	–102.0	–0.75@ 14.5k
0.333	32.0/96.0	12.500	18.900	–103.6	–1.07@ 14.5k
0.250	48.0/192.0	17.600	30.200	–104.0	–0.18@ 20k
0.250	44.1/176.4	16.170	27.746	–104.0	–1.34@ 20k
0.230	44.1/192.0	15.860	28.240	–103.3	–1.40@ 20k
0.167	32.0/192.0	11.200	19.600	–73.2	–2.97@ 14.5k
0.181	32.0/176.4	10.278	17.987	–73.2	–7.88@ 14.5k
0.167	8/48.0	2.800	4.900	–73.2	–2.97@ 3.625k
0.181	8/44.1	2.5695	4.4968	–73.2	–7.88@ 3.625k

Table 10. Digital Filter Example

PACKAGE

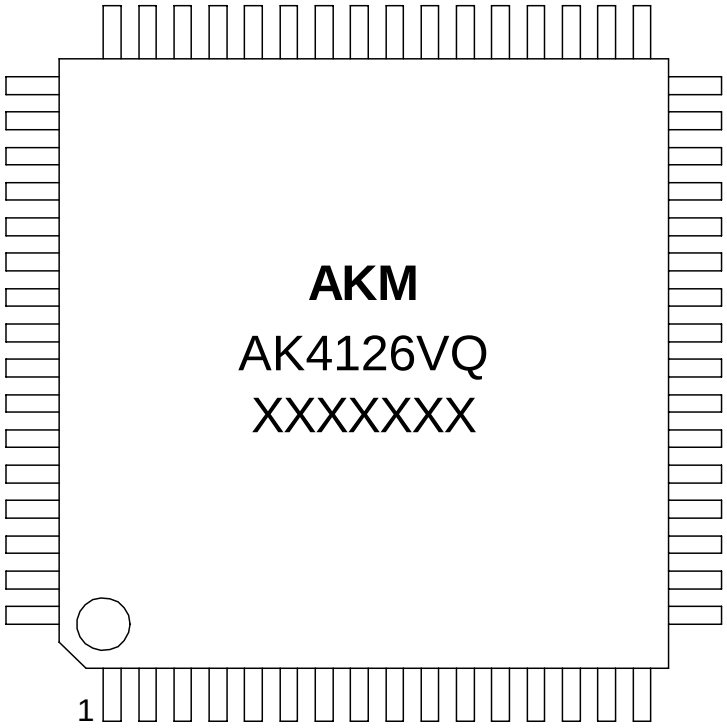
64pin LQFP(Unit:mm)



■ Material & Lead finish

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



XXXXXXX: Date code identifier

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
06/09/20	00	First Edition		
10/05/17	01	Description Addition	20	■ **Sequence of changing clocks** Description is added in notes.

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