# AK8814

## NTSC/PAL Digital Video Encoder

## Notice

AKM does not ship this product (the AK8814) to customers who are not licensed by ROVI corp.

## GENERAL DESCRIPTION

The AK8814 is low voltage, low power and small packaged Digital Video Encoder. It is suitable for a STB or Digital TV. It converts ITU-R.BT601/656 standard 8- bit parallel data into analog composite video signal, S-video in NTSC and PAL formats.

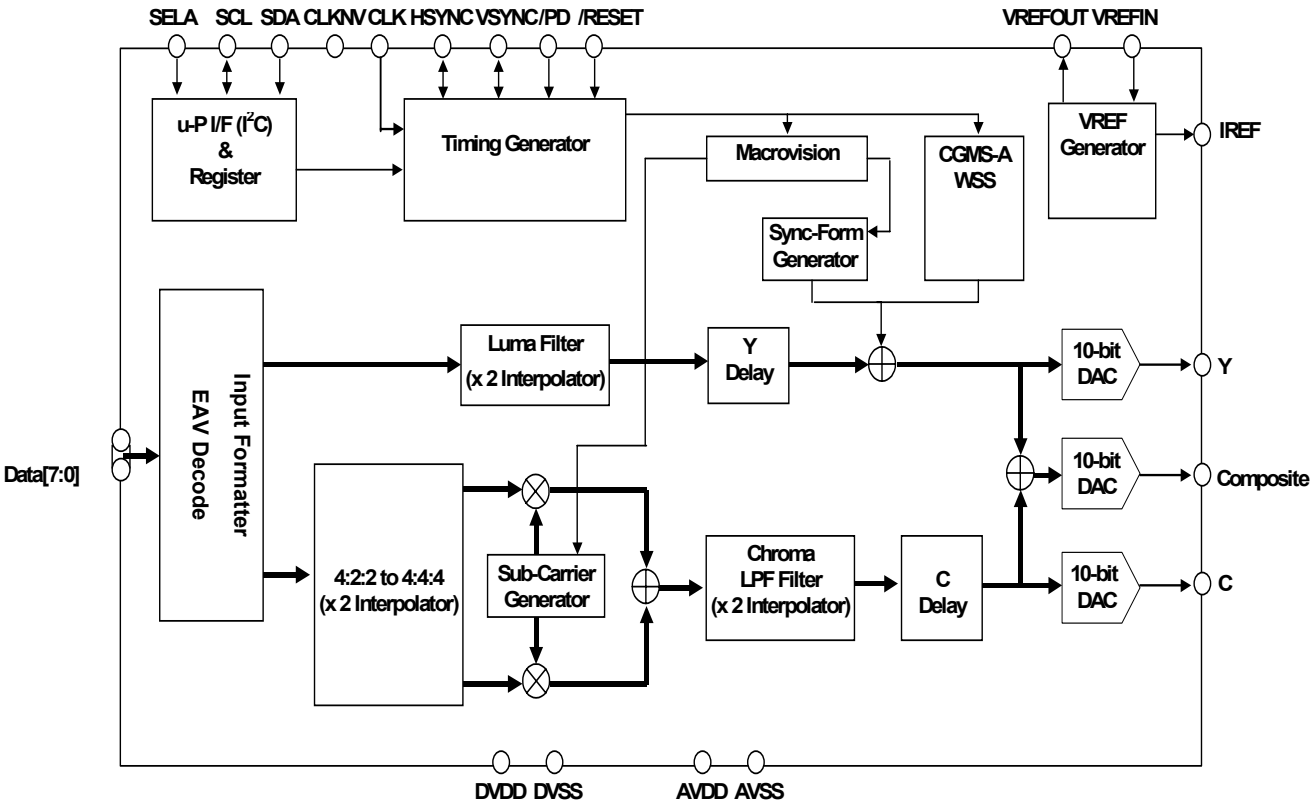
AK8814 supports Macrovision Copy Protection Rev.7.1, Closed Captioning and Video Blanking ID(CGMS-A) and WSS. These functions are controlled by high-speed $I^2C$ Bus interface.

## FEATURES

- NTSC-M, PAL-B,D,G,H,I,M,N encoding.
- Simultaneous composite video signal and S-video signal outputs
- ITU-R BT.656 4:2:2 8-bit Parallel Input
  - EAV Decoding
- Master/Slave Operation
  - Digital Field Sync I/O
  - Digital Vertical/Horizontal Sync I/O
- Y filtering 2 x over-sampling
- C filtering 4 x over-sampling
- Single 27MHz Clock (The polarity could be inverted by SYSINV pin)
- Triple 10-bit DACs
- $I^2C$ Bus Interface (400kHz)
- Closed Caption encoding (NTSC: line 21,284-SMPTE PAL: line 22,335-CCIR)
- Macrovision Copy Protection Rev. 7.1*
- VBID, CGMS-A(EIAJ CPR-1024)
- WSS
- On-chip color bar generator
- Low power consumption
- 2.8V to 3.3V operation CMOS Monolithic
- 57pin FBGA Package

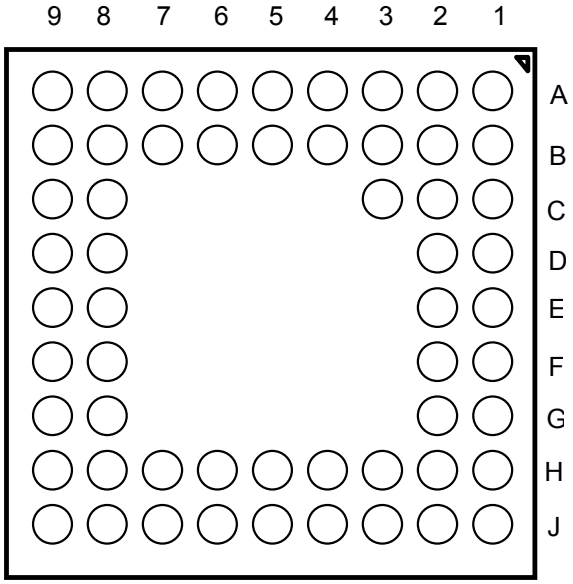
* This device is protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098, and other intellectual rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per -view use only, unless otherwise authorized in written by Macrovision. Reverse engineering or disassembly is prohibited.

## Block Diagram



## PIN LAYOUT

57pin FBGA



## PIN/FUNCTION

| No. | Pin Name | I/O | Description |
|---|---|---|---|
| A1 | NC | - | Open for normal operation |
| B1 | AVSS | G | Analog Ground |
| C1 | AVDD | P | Analog Power supply |
| C2 | VREFOUT | O | Output of the Internal Vref. Terminate with 0.1uF or more capacitor. |
| D1 | VREFIN | I | Input of the Reference Voltage |
| D2 | IREF | O | The currents flow this pin adjusts the full-scale output current of the DAC.<br>Connect this pin to Analog ground via a 6.8kohm resistor ( better than +/- 1% accuracy ). |
| E1 | DVSS | G | Digital Ground |
| E2 | DVDD | P | Digital Power supply |
| F2 | UD0 | I/O | Test pin. Open for normal operation |
| F1 | UD1 | I/O | Test pin. Open for normal operation |
| G2 | UD2 | I/O | Test pin. Open for normal operation |
| G1 | UD3 | I/O | Test pin. Open for normal operation |
| H1 | UD4 | I/O | Test pin. Open for normal operation |
| J1 | NC | - | Open for normal operation |
| J2 | UD5 | I/O | Test pin. Open for normal operation |
| H2 | UD6 | I/O | Test pin. Open for normal operation |
| H3 | UD7 | I/O | Test pin. Open for normal operation |
| J3 | DVSS | G | Digital Ground |
| H4 | SYSCLK | I | 27MHz Clock Input. The polarity could be inverted by SYSINV. |
| J4 | DVDD | P | Digital Power supply |
| H5 | UD8 | I/O | Test pin. Open for normal operation |
| J5 | DVDD | P | Digital Power supply |
| J6 | FID/VSYNC | I/O | Either of FID or VSYNC selected by the register.<br>Rec.656 decode mode :Output<br>Master mode : Output<br>Slave mode : Input<br>FID shows that “L” is odd field and ”H” is even field. |
| H6 | HSYNC | I/O | Rec.656 decode mode : Output<br>Master mode : Output<br>Slave mode : Input |
| H7 | DVSS | G | Digital Ground |
| J7 | SYSINV | I | “L “ : data is latched with rising edge.<br>“H” : data is latched with falling edge. |
| H8 | UD9 | I/O | Test pin. Open for normal operation |
| J9 | NC | - | Open for normal operation |
| J8 | D7 | I | Video data input (MSB) |
| G8 | D6 | I | Video data input |
| H9 | D5 | I | Video data input |

| | | | |
|---|---|---|---|
| G9 | D4 | I | Video data input |
| F8 | DVDD | P | Digital Power supply |
| F9 | DVSS | G | Digital Ground |
| E8 | NC | - | Open for normal operation |
| E9 | D3 | I | Video data input |
| D8 | D2 | I | Video data input |
| D9 | D1 | I | Video data input |
| C8 | D0 | I | Video data input |
| C9 | TEST | I | Open for normal operation |
| B9 | TEST | I | Open for normal operation |
| A9 | NC | - | Open for normal operation |
| A8 | SELA | I | The slave address is set with this pin.<br>“L”:40H “H”:42H |
| B8 | SCL | I | Serial interface clock |
| B7 | SDA | I/O | Serial interface data |
| A7 | PD | I | Power Down Pin. After returning from PD mode to normal operation, RESET Sequence should be done to AK8813. |
| A6 | /RESET | I | After this pin becomes “L”, AK8813 starts the internal initializing sequence. After initializing sequence, AK8813 is set NTSC mode, Rec.656 decoding mode. All DACs Off condition.<br>After power up, AK8813 must be initialized with this pin.<br>(27MHz Clock is necessary for reset sequence.) |
| B6 | AVSS | G | Analog Ground |
| A5 | NC | - | Open for normal operation |
| B5 | Y | O | Output of Luminance Signal. |
| B4 | AVDD | P | Analog power supply |
| A4 | C | O | Output of the Chrominance signal |
| B3 | AVSS | G | Analog Ground |
| A3 | CVBS | O | Output of Composite Video signal |
| B2 | NC | - | Open for normal operation |
| A2 | NC | - | Open for normal operation |
| C3 | NC | - | Open for normal operation |

(Note1) At ITU-R.BT656 I/F mode operation, FID/VSYNC, HSYNC pins should be pulled up to VDD with 100k-ohm Resistor

(Note2) This device requires reset operation. Before resetting the state of the pin of I/O are unknown state. After reset sequence, I/O pins (FID/VSYNC, HSYNC) turns Hi-Z states.

# ELECTRICAL CHARACTERISTICS

## Absolute Maximum Ratings

| Parameter | Min | Max | Units |
|---|---|---|---|
| Supply Voltage (VDD)<br>DVDD, AVDD | -0.3 | 4.6V | V |
| Input Pin Voltage (Vin) | -0.3 | VDD+0.3 | V |
| Input Pin Current (Iin) | - | ±10 | mA |
| Analog Reference Current (IREF) | - | 0.21 | mA |
| Analog Output Current | - | 6.5 | mA |
| Storage Temperature | -40 | 125 | °C |

(Note)When all Ground pins(DVSS, AVSS) are set to 0V.

## Recommended Operating Conditions

| Parameter | Min | Typ. | Max | Units |
|---|---|---|---|---|
| Supply Voltage (VDD) | 2.8 | 3.3 | 3.6 | V |
| Operating Temperature | -40 | | 85 | °C |

## DC Characteristics

[Power Supply:2.8 ~ 3.6V Temperature:-40 ~ 85°C]

| Parameter | Symbol | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| Digital Input High Voltage | VIH1 | 0.7VDD | | V | Note1) |
| Digital Input Low Voltage | VIL1 | | 0.3VDD | V | Note1) |
| Digital Input leak Current | IL | | ±10 | uA | Note1) |
| Digital Output High Voltage | VOH | 2.2 | | V | IOH =-1mA Note 2) |
| Digital Output Low Voltage | VOL1 | | 0.4 | V | IOL = 2mA Note 2) |
| $I^2C$ Input High Voltage $I^2C$(SDA,SCL) | VIH2 | 0.7VDD | | V | |
| $I^2C$ Input Low Voltage $I^2C$(SDA,SCL) | VIL2 | | 0.3VDD | V | |
| $I^2C$(SDA) Output Voltage | VOL2 | | 0.4 | V | IOL = 3mA |

Note 1) D[9:0],FID/VSYNC, HSYNC, SYSCLK, /RESET pin

Note 2) FID/VSYNC, HSYNC pin

Note ) Connected Test Pin to Ground, SELA and SYSINV Pin are desired polarity.

## Analog Characteristics and Dissipation Current

[Power Supply:3.3V Temperature:25°C]

| Parameter | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| DAC Resolution | | 10 | | bit | |
| DAC Integral linearity error | | ±0.6 | ± 2 | LSB | |
| DAC Differential linearity error | | ±0.4 | ± 1 | LSB | |
| DAC Output Full Scale Voltage | 1.21 | 1.28 | 1.35 | V | Note1) |
| DAC Output offset Voltage | | | 5.0 | mV | Note2) |
| Unbalances between DACs | | ±1 | ±5 | % | Note3) |
| Isolation between DACs | | 50 | | dB | 1MHz Full Scale |
| DAC Load Capacitance | | | 30 | pF | Note4) |
| Internal Reference Voltage | 1.17 | 1.235 | 1.30 | V | |
| Internal Reference Drift | | -50 | | ppm/°C | |
| DAC Current (Active mode) | | 24 | | mA | Note5) |
| DAC Current (Sleep mode) | | 10 | | uA | Note6) |
| Total Current | | 50 | 65 | mA | Note7) |
| Power Down Current | | 10 | 100 | uA | |

Note 1) Under the condition of output load 220Ω, IREF pin with 6.8kΩ, using internal reference. The output full-scale current IOUT is calculated as Full scale output voltage (typ. 1.28V) /220Ω=typ. 5.82mA.

Note 2) DAC output when feeding code of 0 (Decimal).

Note 3) Deviation between the DAC output when feeding 1V generating code of 800(Decimal).

Note 4) The value is a design target. This value is not tested.

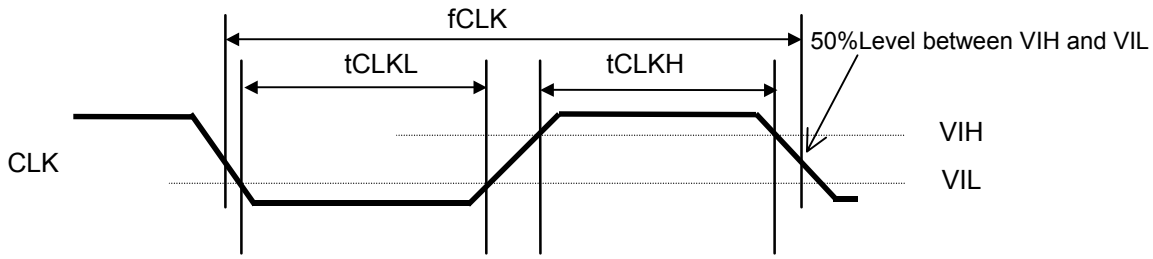
Note 5) All DACs are operating.

Note 6) All DACs are turned off with no system clock.

Note 7) NTSC internal color bar with 3ch DACs operation and slave mode operation. DAC output pins is connected with only 220Ω load.

## AC Characteristics (2.8V - 3.6V Temperature –40 ~ 85°C)

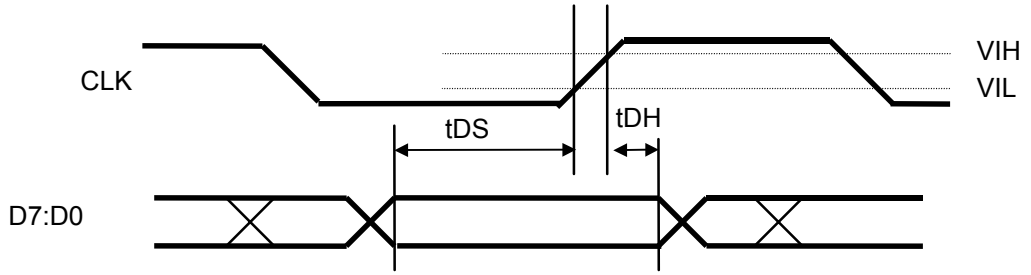
1. SYSCLK



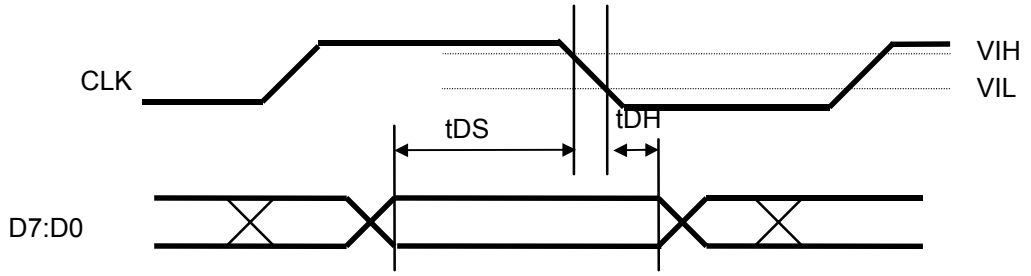

| Parameter | Symbol | Min. | Typ. | Max | Unit |
|---|---|---|---|---|---|
| SYSCLK | fSYSCLK | | 27 | | MHz |
| SYSCLK Pulse width H | tCLKH | 15 | | | nsec |
| SYSCLK Pulse width L | tCLKL | 15 | | | nsec |

## (2). Pixel Data Input Timing

### (2-1) SYSINV = Low




### (2-2) SYSINV = High

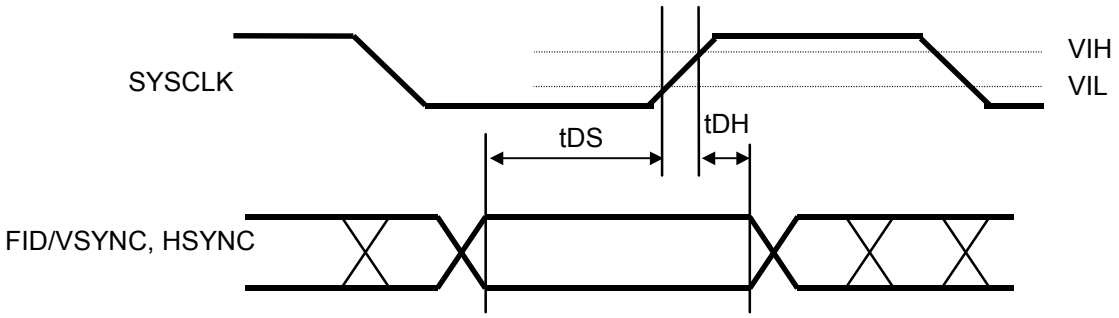



| Parameter | Symbol | Min | Typ | Max | Units |
|---|---|---|---|---|---|
| Data Setup Time | tDS | 5 | | | nsec |
| Data Hold Time | tDH | 8 | | | nsec |

## (3). Synchronizing Signal ( FID/VSYNC, HSYNC )

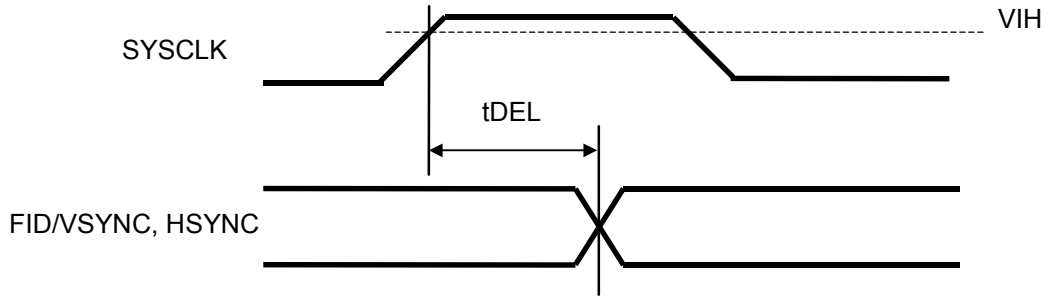
### (3-1) SYSINV=Low

#### (3-1-1) Input Timing




| Parameter | Symbol | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Data Setup Time | tDS | 5 | | | nsec |
| Data Hold Time | tDH | 8 | | | nsec |

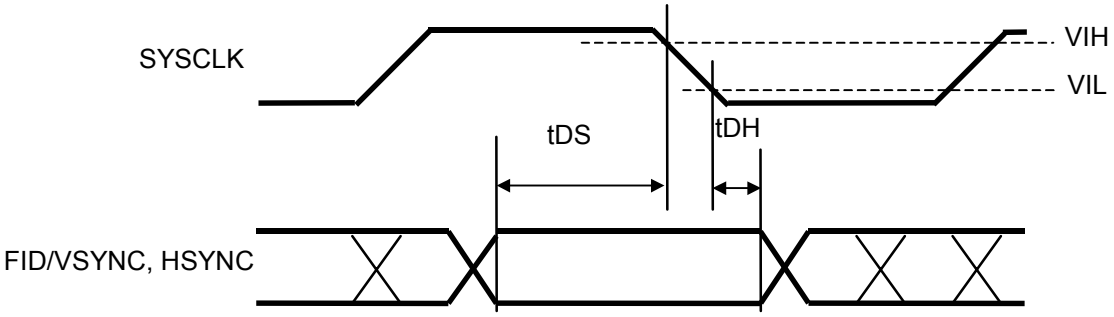
#### (3-1-2) Output Timing




| Parameter | Symbol | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Delay from SYSCLK | tDEL | | | 27 | nsec |

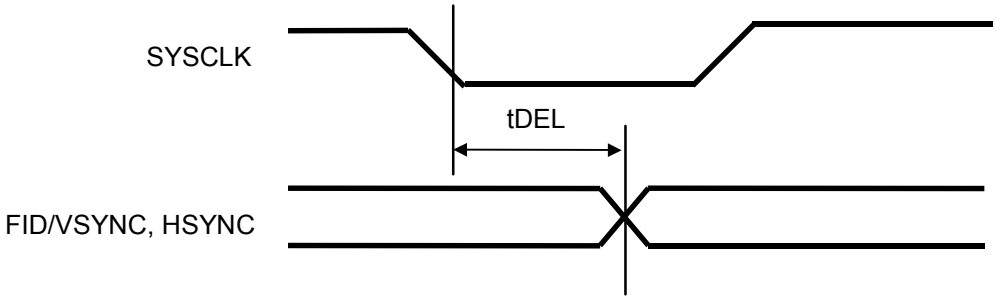
(3-2) SYSINV = High

(3-2-1) Input Timing




| Parameter | Symbol | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Data Setup Time | tDS | 5 | | | nsec |
| Data Hold Time | tDH | 8 | | | nsec |

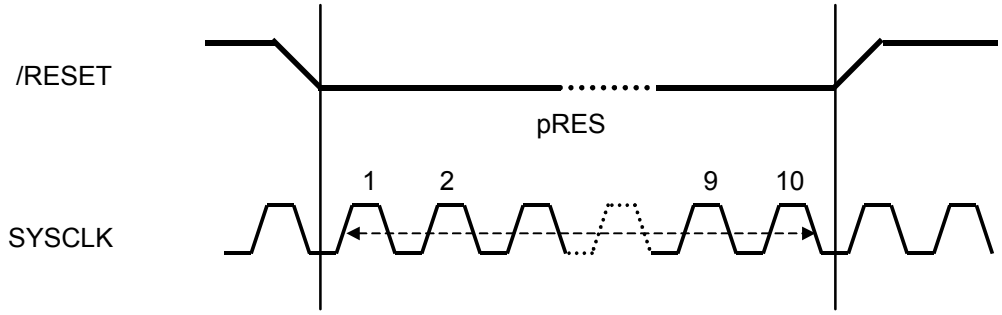
(3-2-2) Output Timing




| Parameter | Symbol | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| Delay from SYSCLK | tDEL | | | 27 | nsec |

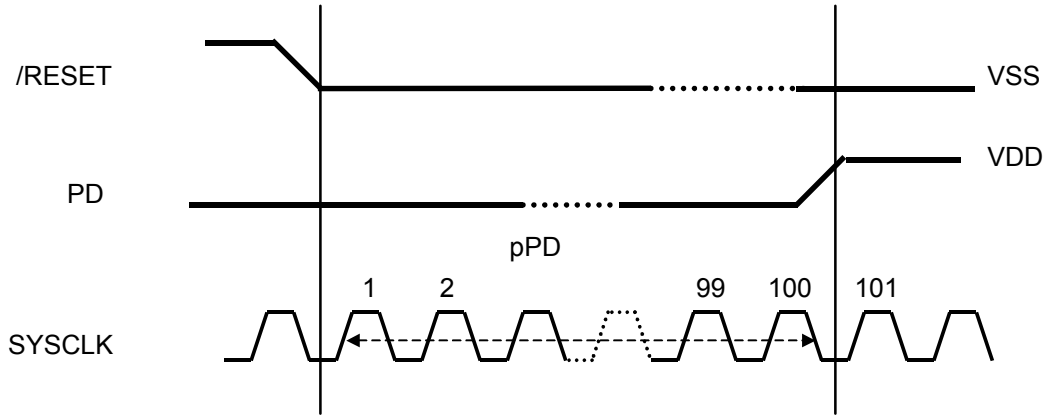
(4). Reset (Initialize)

Reset Timing




| Parameter | Symbol | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| /RESET Pulse Width | pRES | 10 | | | SYSCLK |

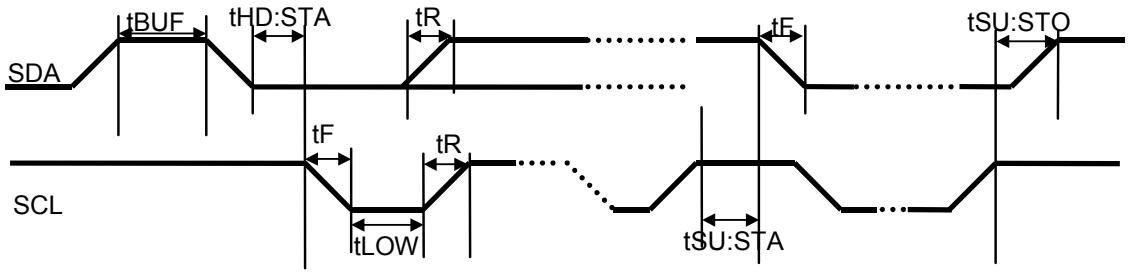
(5) Power Down Sequence




| Parameter | Symbol | Min | Typ. | Max | Units |
|---|---|---|---|---|---|
| /RESET Pulse Width | pSTOP | 100 | | | SYSCLK |

## (4). $I^2C$ Bus (SCL 400kHz cycle mode)

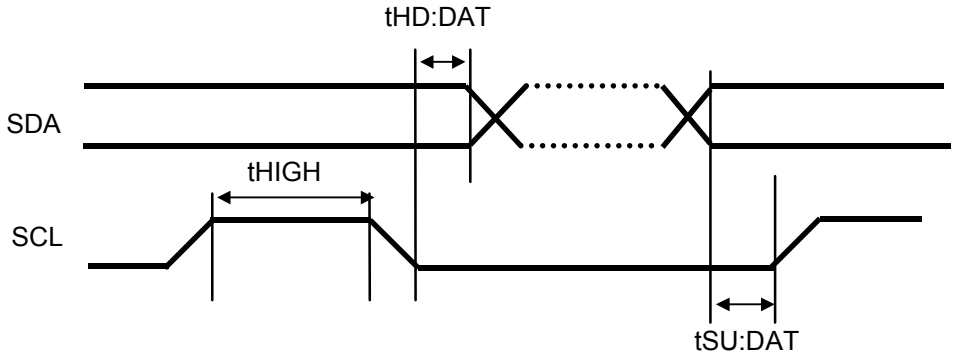
### (4-1) I/O Timing 1




| Parameter | Symbol | Min | Max | Units |
|---|---|---|---|---|
| Bus Free Time | tBUF | 1.3 | | usec |
| Hold Time (Start Condition) | tHD:STA | 0.6 | | usec |
| Clock Pulse Low Time | tLOW | 1.3 | | usec |
| Bus Signal Rise Time | tR | | 300 | nsec |
| Bus Signal Fall Time | tF | | 300 | nsec |
| Setup Time(Start Condition) | tSU:STA | 0.6 | | usec |
| Setup Time(Stop Condition) | tSU:STO | 0.6 | | usec |

All the figures shown above list are not restricted by AK8814 but are restricted by $I^2C$ Bus standard.
Please see the $I^2C$ Bus standard for further details.

### (4-2) I/O Timing 2




| Parameter | Symbol | Min. | Max. | Unit. |
|---|---|---|---|---|
| Data Setup Time | tSU:DAT | 100 (1) | | nsec |
| Data Hold Time | tHD:DAT | 0.0 | 0.9 (2) | usec |
| Clock Pulse High Time | tHIGH | 0.6 | | usec |

(1) In case of normal $I^2C$ bus mode tSU:DAT ≥250nsec
(2) Using under minimum tLOW, this value must be satisfied.

## FUNCTIONAL DESCRIPTION

### ♦ Reset

When the reset pin [ /RESET ] set to “L”, AK8814 is in reset state. AK8814 starts in the internal initializing sequence at the trailing edge of the first SYSCLK after the reset pin is “L”. All internal registers are set to be default value by this initializing sequence. AK8814 needs at least 10 clock counts of SYSCLK for this reset operation. After the reset operation, the video output pins are in high-impedance. AK8814 requires SYSCLK for the reset operation.

### ♦ Master Clock

AK8814 requires 27MHz clock at SYSCLK pin for operation. Video input data (ITU-R BT.656) is sampled at the trailing edge of this 27MHz. SYSINV decides the edge direction.

SYSINV = L Data is sampled at rising edge of SYSCLK.
SYSINV = H Data is sampled at falling edge of SYSCLK.

### ♦ Video Signal Interface

AK8814 can interface with the video input data by the following 3 modes. The mode is set by the register [ Interface mode register(00H) ].

#### 1. ITU-R BT.656 Format

AK8814 decodes EAV in stream data and manages an internal synchronization.
In this case, AK8814 outputs FID (odd : “L” even : “H”)/ VSYNC and HSYNC.
CCIR-bit of [ Interface mode register (00H) ] should be set “1” .

#### 2. ITU-R BT.656 like Format (4:2:2 Y/Cb/Cr)

There are Master and Slave modes, for ITU-R BT.656 like Format which does not include EAV. In this mode, CCIR-bit of [ Interface mode register(00H) ] should be set “0” .

<Master Mode>

AK8814 provides FID/VSYNC and HSYNC to an external device according to the AK8814 internal timing counter. AK8814 starts to sample the input data at the fixed value on the internal pixel counter.
In this mode, following setting should be done to [Interface mode register(00H)].
CCIR-bit = 0
MAS-bit = 1

<Slave Mode>

FID/VSYNC and HSYNC are supplied by an external device. AK8814 samples the data as same manner of Master mode.
In this mode, following setting should be done to [Interface mode register(00H)].
CCIR-bit = 0
MAS-bit = 0

## ♦ Video Signal Conversion

Video reconstruction module converts the multiplexed data (ITU-R. BT601 Y/Cb/Cr) to the interlace format of NTSC-M, PAL-M, PAL-B,D,G,H,I,N and other formats (ex. NTSC-4.43 and PAL60). The video reconstruction format, the line number, the color encode way(NTSC or PAL) and the frequency of Color Sub-carrier is specified by [Video Process 1 register(01H)]. (cf. Burst Signal Table) The frequency and the phase of Color Sub-carrier are also adjustable by [Sub C. Freq. register(06H)] and [Sub C. Phase register(07H)]. The Sub-carrier has a free-running mode and a reset-mode. In the reset-mode, the Sub-carrier is reset automatically to the initial phase for every 4 fields (NTSC) or 8 fields (PAL).

## ♦ Luminance Filter

Luminance signal passes through the 2x Low Pass filter with sin(x)/x compensation. Fig.1 is the characteristic of Luminance Filter.

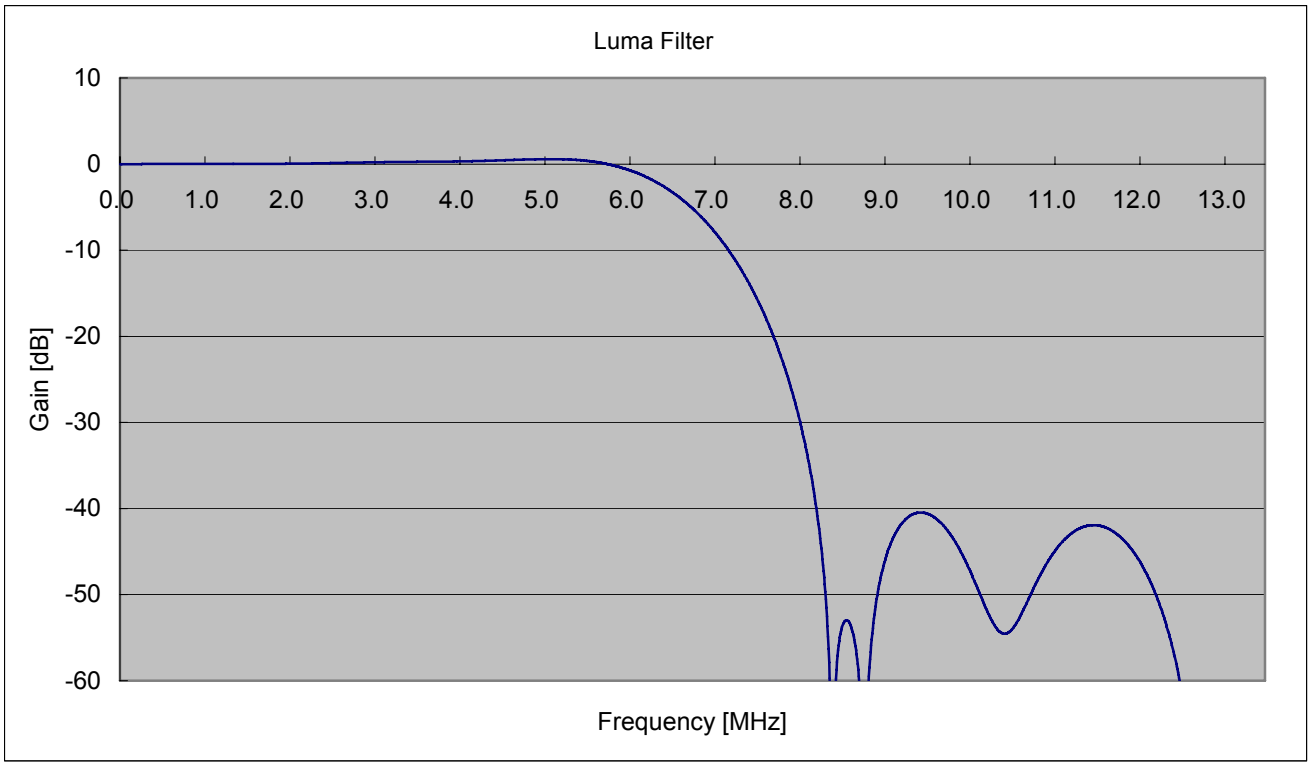



Fig. 1 Luminance Filter

## ♦ Chrominance Filter

Chrominance signals (Cb,Cr) before Sub-carrier modulation pass through the 1.3 MHz Low pass filter shown in Fig.2. Chrominance signal modulated by Sub-carrier passes through the filter shown in Fig.3.

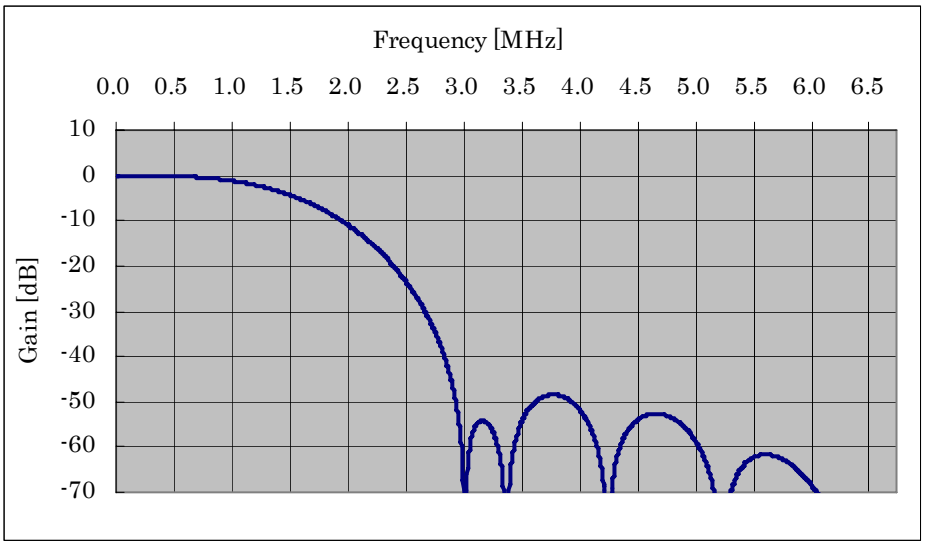



Fig. 2 Chroma-1 LPF

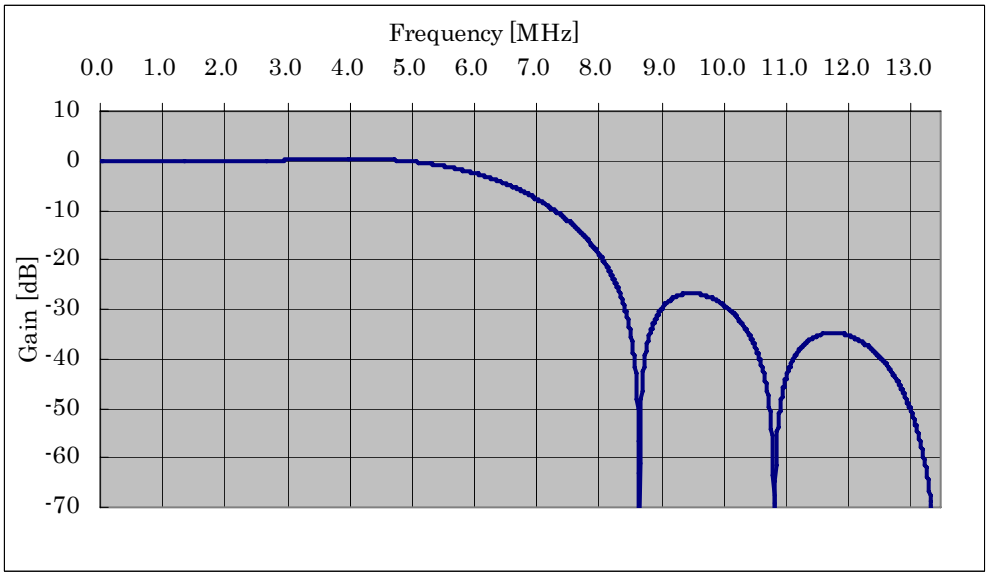



Fig. 3 Chroma-2 LPF

## ♦ Color burst signal

Color burst signal is generated by 32bits-length Digital Frequency Synthesizer. The Default frequency of the color burst is selected by [Video Process 1 Register(0x01)].

| Standard | Sub-carrier Freq. [MHz] | Video Process 1 [VM1,VM0] |
|---|---|---|
| NTSC-M | 3.57954545 | [0,0] |
| PAL-M | 3.57561188 | [0,1] |
| PAL-B,D,G,H,I | 4.43361875 | [1,1] |
| PAL-N(Arg.) | 3.5820558 | [1,0] |
| PAL-N(non-Arg.) | 4.43361875 | [1,1] |
| PAL60 | 4.43361875 | [1,1] |
| NTSC-4.43 | 4.43361875 | [1,1] |

Burst Signal Table

Sub-carrier frequency 3.57561188MHz is allowed when PAL-M mode is selected.

The burst frequency and initial phase resolution are as follows.

| | |
|---|---|
| Frequency resolution | 0.8046Hz |
| SCH Phase resolution | 360°/256 |

## ♦ Video DAC

AK8814 has the three current driven 10bits-DACs at 27MHz operation. The full scale voltage of DAC is determined by the current output from IREF pin. Typical output voltage is 1.28Vo-p under the condition of VREFIN 1.235V, 6.8KΩ between IREF pin and Ground(AVSS) and DAC load resistance of 220Ω. This full-scale voltage should be set in the range of 1.17V to 1.33V by adjusting the resistor which terminates IREF pin. Each DAC output can be set to “active state” or to “inactive state” individually by [DAC Mode register(05H)]. When DAC is in “inactive state”, the output is Hi-impedance. When all DACs are set to “inactive state”, the analog part of AK8814 goes into sleep mode. In this case AK8814 stops outputing the reference voltage(VREF) output. When any DAC is switched over in “active state” from sleep mode, AK8814 starts outputing reference voltage. In this case AK8814 needs several milisecond for VREF wake-up time.

Using internal VREF as the reference voltage, connect [VREF OUT] pin with [VREF IN] pin and [VREF OUT] pin is terminated with more than 0.1uF capacitor.

## ♦ Use external Reference Voltage

In order to improve the accuracy of DAC output, external reference voltage may be used. In this case, VREFOUT pin still needs to be terminated with more than 0.1uF capacitor.

## ♦ Copy Protection

Macrovision Copy Protection Rev.7.1

Information about the Macrovision encoding functions of the AK8814 is available to Macrovision licensees. Macrovision may be contacted at:

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Main Telehone (switchboard): +1 408 743-8600
Main Fax: +1 408 743-8610
Technical Support Group Fax: +1 408 743-8617

Macrovision Register is same as AK8812

| Register | | bit-7 | bit-6 | bit-5 | bit-4 | bit-3 | bit-2 | bit-1 | bit-0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0A | :CSP32 | - | - | - | - | CPS32[3] | CPS32[2] | CPS32[1] | CPS32[0] |
| 0x0B | CPS31:CPS30 | CPS31[3] | CPS31[2] | CPS31[1] | CPS31[0] | CPS30[3] | CPS30[2] | CPS30[1] | CPS30[0] |
| 0x0C | CPS29:CPS28 | CPS29[3] | CPS29[2] | CPS29[1] | CPS29[0] | CPS28[3] | CPS28[2] | CPS28[1] | CPS28[0] |
| 0x0D | CPS27:CPS26 | CPS27[3] | CPS27[2] | CPS27[1] | CPS27[0] | CPS26[3] | CPS26[2] | CPS26[1] | CPS26[0] |
| 0x0E | CPS25:CPS24 | CPS25[3] | CPS25[2] | CPS25[1] | CPS25[0] | CPS24[3] | CPS24[2] | CPS24[1] | CPS24[0] |
| 0x0F | CPS23:CPS22 | CPS23[3] | CPS23[2] | CPS23[1] | CPS23[0] | CPS22[3] | CPS22[2] | CPS22[1] | CPS22[0] |
| 0x10 | CPS21:CPS20 | CPS21[3] | CPS21[2] | CPS21[1] | CPS21[0] | CPS20[3] | CPS20[2] | CPS20[1] | CPS20[0] |
| 0x11 | CPS19:CPS18 | CPS19[3] | CPS19[2] | CPS19[1] | CPS19[0] | CPS18[3] | CPS18[2] | CPS18[1] | CPS18[0] |
| 0x12 | CPS17:CPS16 | CPS17[3] | CPS17[2] | CPS17[1] | CPS17[0] | CPS16[3] | CPS16[2] | CPS16[1] | CPS16[0] |
| 0x13 | CPS15:CPS14 | CPS15[3] | CPS15[2] | CPS15[1] | CPS15[0] | CPS14[3] | CPS14[2] | CPS14[1] | CPS14[0] |
| 0x14 | CPS13:CPS12 | CPS13[3] | CPS13[2] | CPS13[1] | CPS13[0] | CPS12[3] | CPS12[2] | CPS12[1] | CPS12[0] |
| | | | | | | | | | |
| 0x1D | CPC1:CPC0 | CPC1[3] | CPC1[2] | CPC1[1] | CPC1[0] | CPC0[3] | CPC0[2] | CPC0[1] | CPC0[0] |
| 0x1E | CPS11:CPS10 | CPS11[3] | CPS11[2] | CPS11[1] | CPS11[0] | CPS10[3] | CPS10[2] | CPS10[1] | CPS10[0] |
| 0x1F | CPS9:CPS8 | CPS9[3] | CPS9[2] | CPS9[1] | CPS9[0] | CPS8[3] | CPS8[2] | CPS8[1] | CPS8[0] |
| 0x20 | CPS7:CPS6 | CPS7[3] | CPS7[2] | CPS7[1] | CPS7[0] | CPS6[3] | CPS6[2] | CPS6[1] | CPS6[0] |
| 0x21 | CPS5:CPS4 | CPS5[3] | CPS5[2] | CPS5[1] | CPS5[0] | CPS4[3] | CPS4[2] | CPS4[1] | CPS4[0] |
| 0x22 | CPS3:CPS2 | CPS3[3] | CPS3[2] | CPS3[1] | CPS3[0] | CPS2[3] | CPS2[2] | CPS2[1] | CPS2[0] |
| 0x23 | CPS1:CPS0 | CPS1[3] | CPS1[2] | CPS1[1] | CPS1[0] | CPS0[3] | CPS0[2] | CPS0[1] | CPS0[0] |

## ♦ Closed Caption and Extended Data

AK8814 supports both Closed Captioning and Extended Data. They are controlled “ON” or ”OFF” respectively by [ Video Process 2 Register(02H) ]. Each data consists of 2 continuous bytes register( Closed Caption R (16H,17H) ), and it is recognized as the data is renewed when the second byte(17H register) is written in the register. After the data is renewed, AK8814 encodes Closed Captioning and Extended Data at the designated line. If the data isn’t renewed, AK8814 outputs “ASCII-NULL” code. The data is supposed as Odd Parity and 7 bit US-ASCII code. Host should provide a parity bit.

*In PAL encoding mode, AK8814 outputs them at the same timing and same pattern as NTSC.

*The line where Closed Captioning data is encoded is as follows.

| | 525/60 System (SMPTE) | 625/50 System (CCIR) |
|---|---|---|
| Closed Caption | 21 Line default | 22 Line default |
| Extended Data | 284 Line default | 335 Line default |

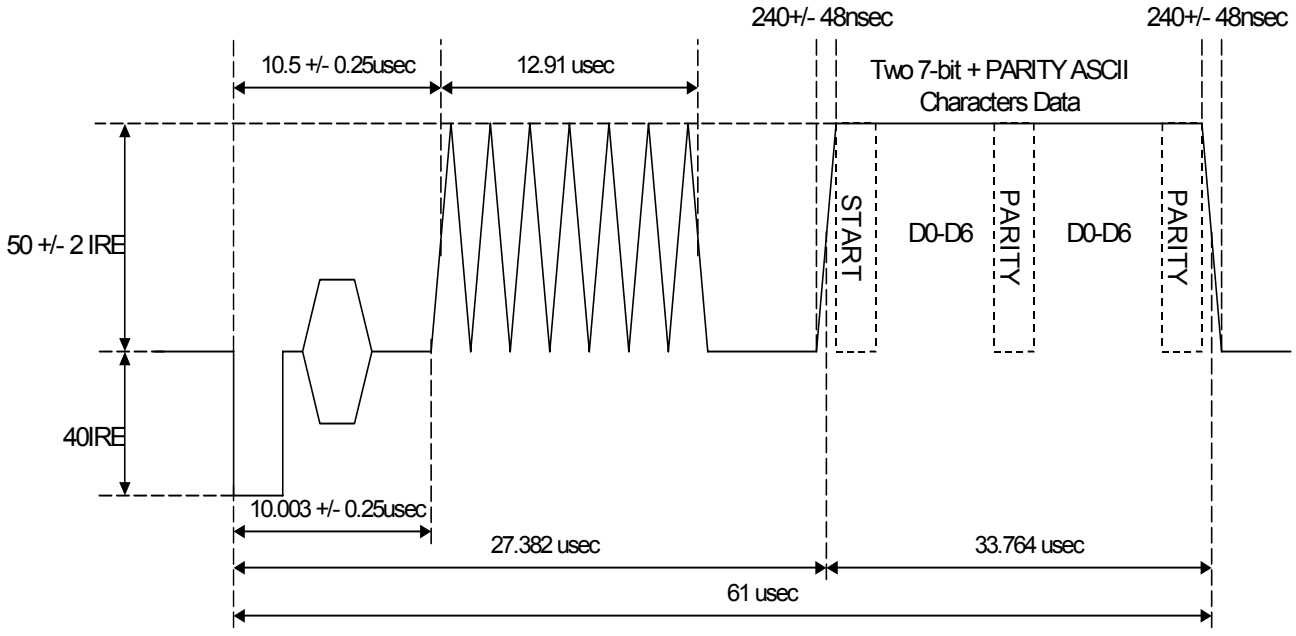



Fig. 4 Closed Captioning Wave form

## ♦ Video ID

AK8814 supports Video ID (EIAJ standard, CPR-1204) encoding for the distinction of an aspect ratio or CGMS-A etc. Setting or Resetting the VBID-bit of [ Video Process 2 Register(02H) ], this function is switched On/Off. The data is set by using [ Video ID Data Register(1AH, 1BH) ].

### VBID Data Renewal Timing.

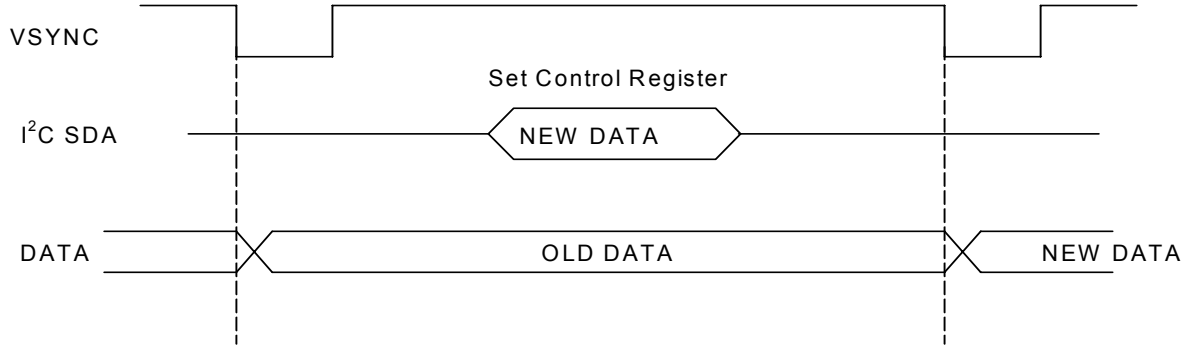



Fig. 5 VBID Data renewal Timing

### VBID Data Layout

VBID is consists of 20 bits and its format is shown as follows.

AK8814 generates CRC code automatically and appends it to the data. Initial value of the Polynomial is 1.

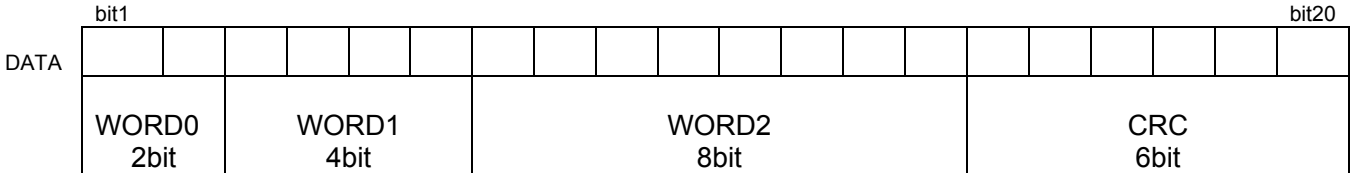



Fig. 6 VBID code assignment

## VBID Waveform

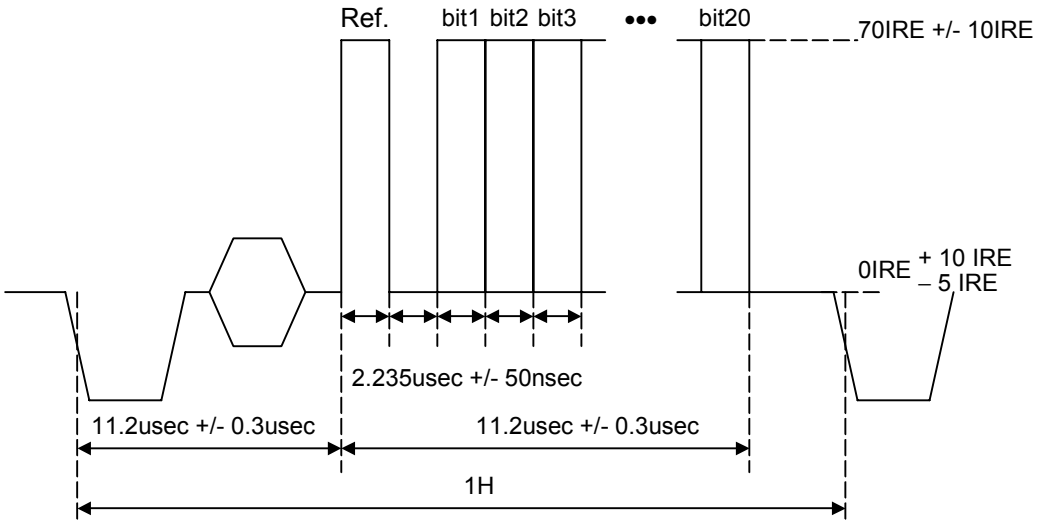



Fig. 7 VBID Wave Form

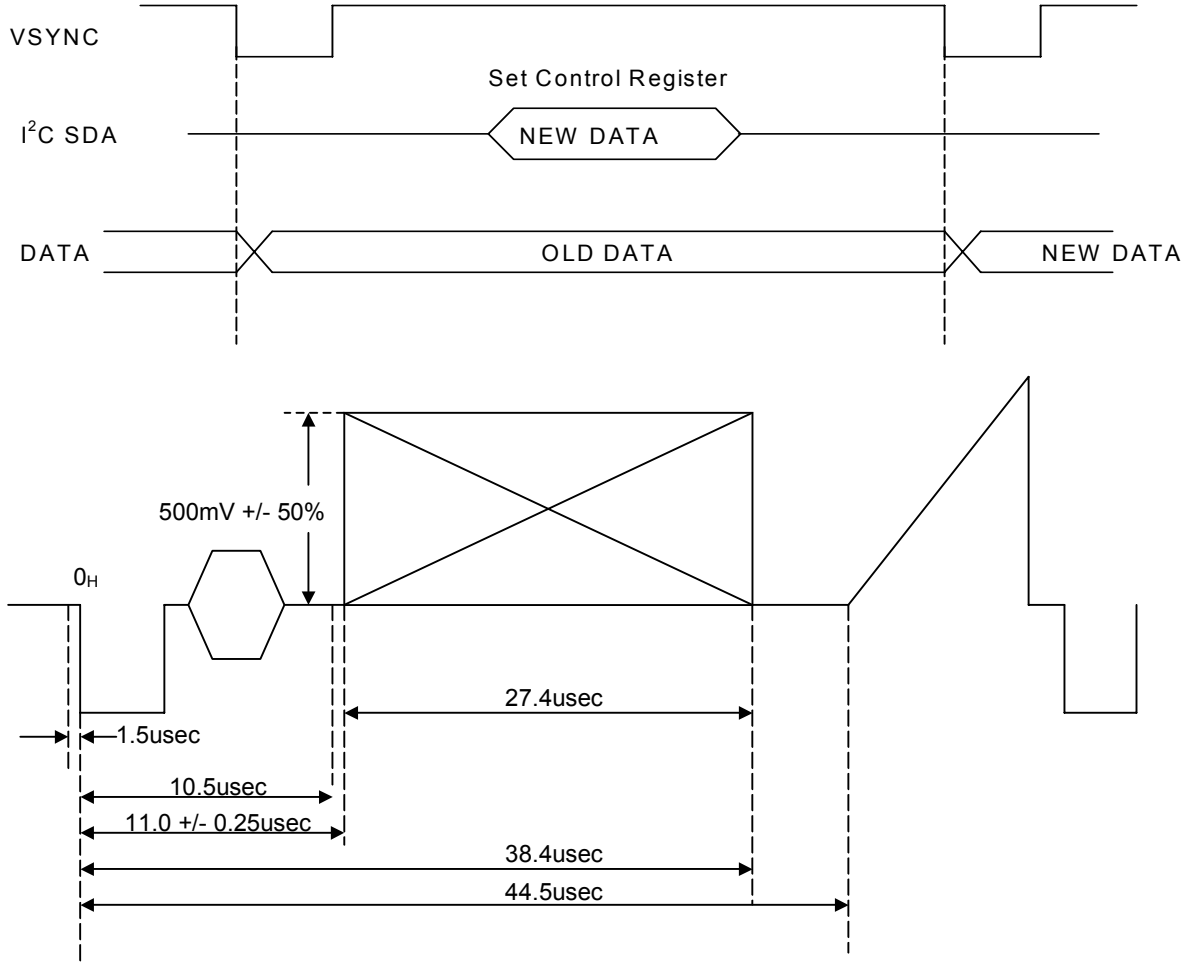
| | 525/60 system | 625/50 system |
|---|---|---|
| Amplitude | 70 IRE | 490 mV |
| Encode Line | 20/283 | 20/333 |

VBID parameter table

## ♦ WSS

AK8814 supports WSS(ITU-R.Bt.1119) encoding for the distinction of an aspect ratio etc. Setting or Resetting the WSS-bit of [ Video Process 2 Register(02H) ], this function is switched On/Off. The data is set by using [ WSS Data Register(08H, 09H) ].

### WSS Data Renewal Timing




Encode Line: Line 23
Coding: bi-phase modulation coding
Clock: 5MHz (Ts = 200ns)

| Run-in | Start code | Group 1<br>Aspect ratio | Group 2<br>Enhanced Services | Group 3<br>Subtitles | Group4<br>Reserved |
|---|---|---|---|---|---|
| 29 elements | 24 elements | 24 elements | 24 elements | 18 elements | 18 elements |
| | | Bit numbering<br>0 1 2 3<br>LSB MSB<br>0 : 000111<br>1 : 111000 | Bit numbering<br>4 5 6 7<br>LSB MSB<br>0 : 000111<br>1 : 111000 | Bit numbering<br>8 9 10<br>LSB MSB<br>0 : 000111<br>1 : 111000 | Bit numbering<br>11 12 13<br>LSB MSB<br>0 : 000111<br>1 : 111000 |
| 0x1F1C71C7 | 0x1E3C1F | | | | |

## ♦ AK8814 Interface Timing (Part 1) Master mode & ITU-R BT. 656 mode

On ITU-R BT.656 decoding mode or master mode operation, AK8814 outputs HSYNC and FID or VSYNC (selected by register).

When AK8814 receives ITU-R BT. 656 signal, AK8814 decodes [EAV] code in the data for synchronization then outputs the HSYNC. AK8814 outputs HSYNC at the rising edge of SYSCLK in the timing of the 32nd/24th(NTSC/PAL) data slot, which is counted from the [EAV] starting point as below. (See also AC Characteristics 2-2[Input Synchronizing Signal])

On master mode operation, the front device connected with AK8814 (ex. MPEG Decoder) starts to set Cb on the 276th/288th(NTSC/PAL) slot, after starting to count HSYNC falling edge as 32nd/24th(NTSC/PAL) slot.

FID/VSYNC is output synchronously with HSYNC at the timing of solid line as in Fig. 10 Video Field.

| | EAV | | | | | | | | | | SAV | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Y/Cb/Cr | Cb | Y | Cr | Y | Cb | Y | Cr | Y | | | Cb | Y | Cr | | | Y | Cb | Y | Cr | Y | Cb | Y | Cr | Y | Cb |
| Data# 525system | 360 | 720 | 360 | 721 | 361 | 722 | 361 | 723 | | | 368 | 736 | 368 | | | 855 | 428 | 856 | 428 | 857 | 0 | 0 | 0 | 1 | 1 |
| Data# 625system | 360 | 720 | 360 | 721 | 361 | 722 | 361 | 723 | | | 366 | 732 | 366 | | | 861 | 431 | 862 | 431 | 863 | 0 | 0 | 0 | 1 | 1 |

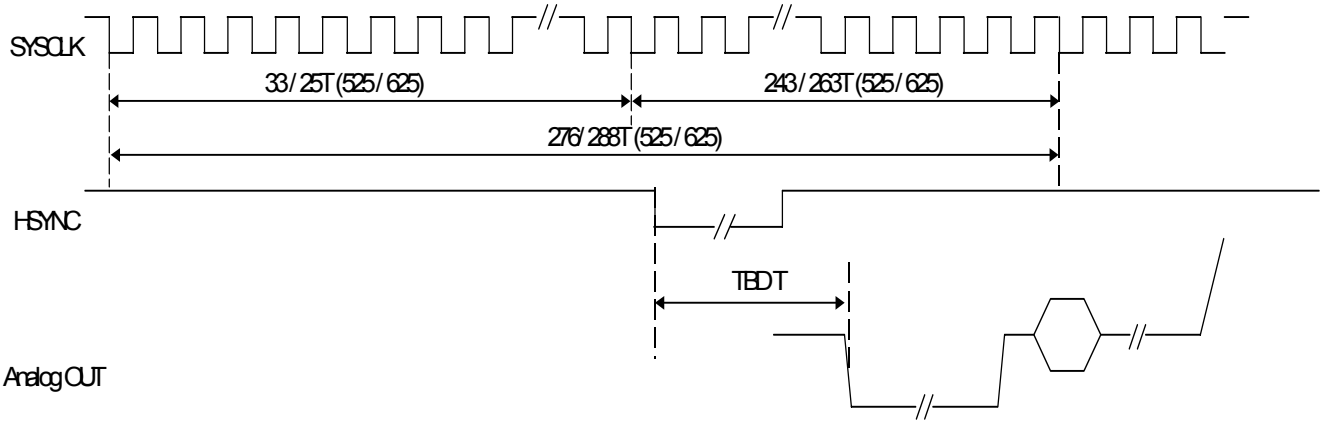



Fig. 8 Interface Timing (ITU-R BT.656 or Master mode)

## ♦ AK8814 Interface Timing (Part 2) Slave mode

On slave mode operation, HSYNC and FID or VSYNC (Selected by register) are input to AK8814.

AK8814 monitors the transition of HSYNC at the timing of the rising edge of SYSCLK. (Refer to AC Characteristic 2-1. [Input Synchronizing Signal]) After AK8814 recognizes HSYNC is Low-logic, AK8814 sets the slot number to the 32nd/24th(NTSC/PAL), internally, then AK8814 starts to sample the data as Cb on 276th/288th(NTSC/PAL) slot.

Video field is recognized the transition timing between FID/VSYNC and HSYNC. (Fig.10. Video Field) As in the figure, there is a toreralnce of ±1/4H.

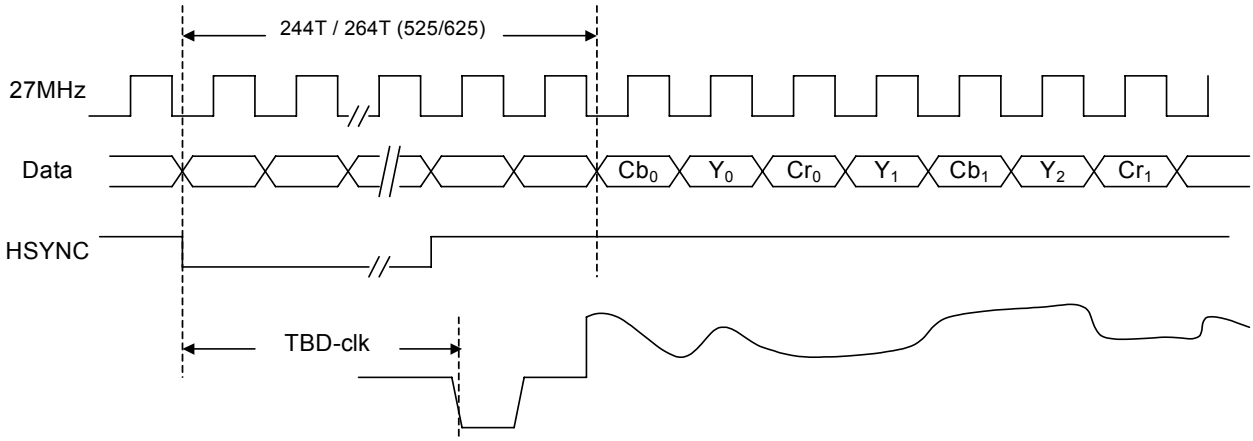
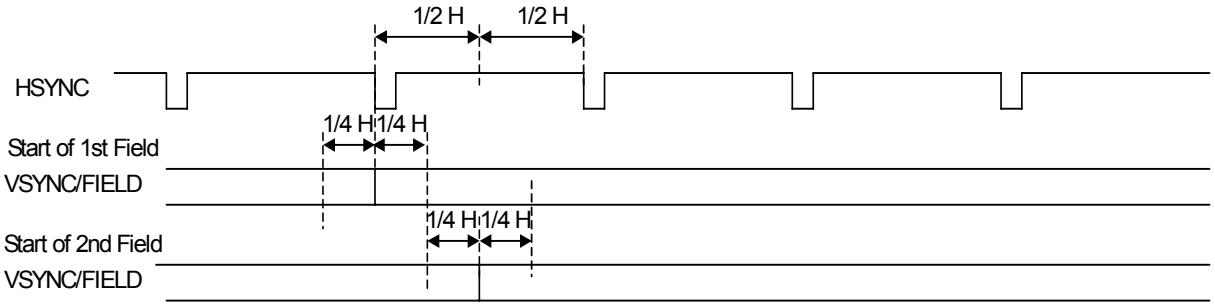



Fig. 9. Interfacing timing (Slave mode)

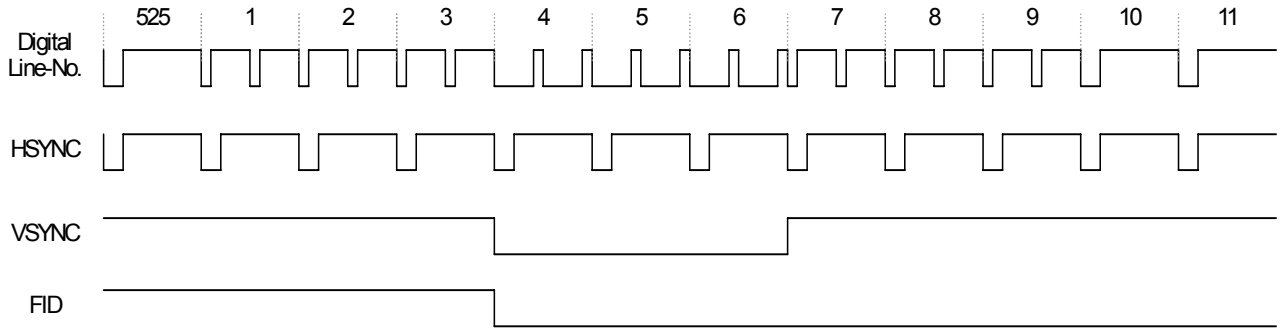


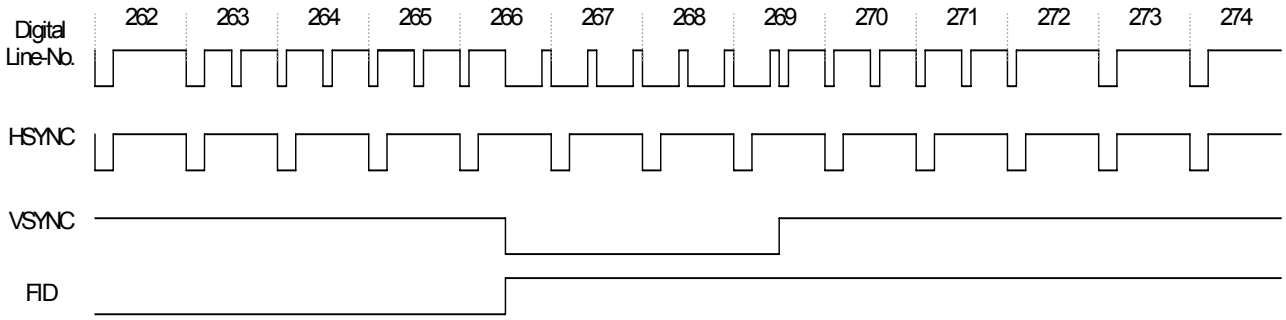

F

ig. 10. Video Field

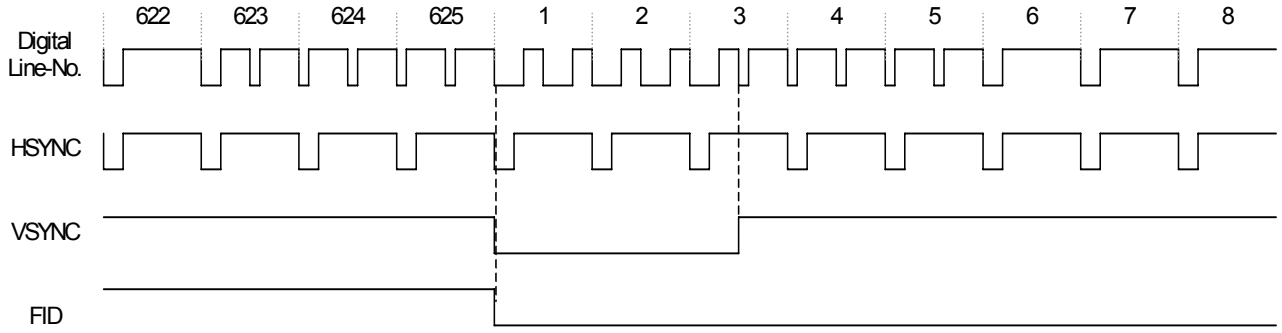
## ♦ HSYNC FID/VSYNC Timing

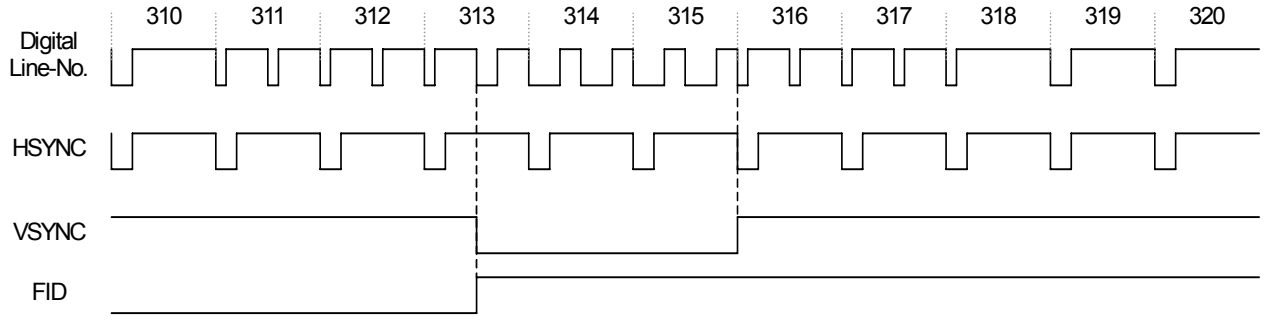
525 System



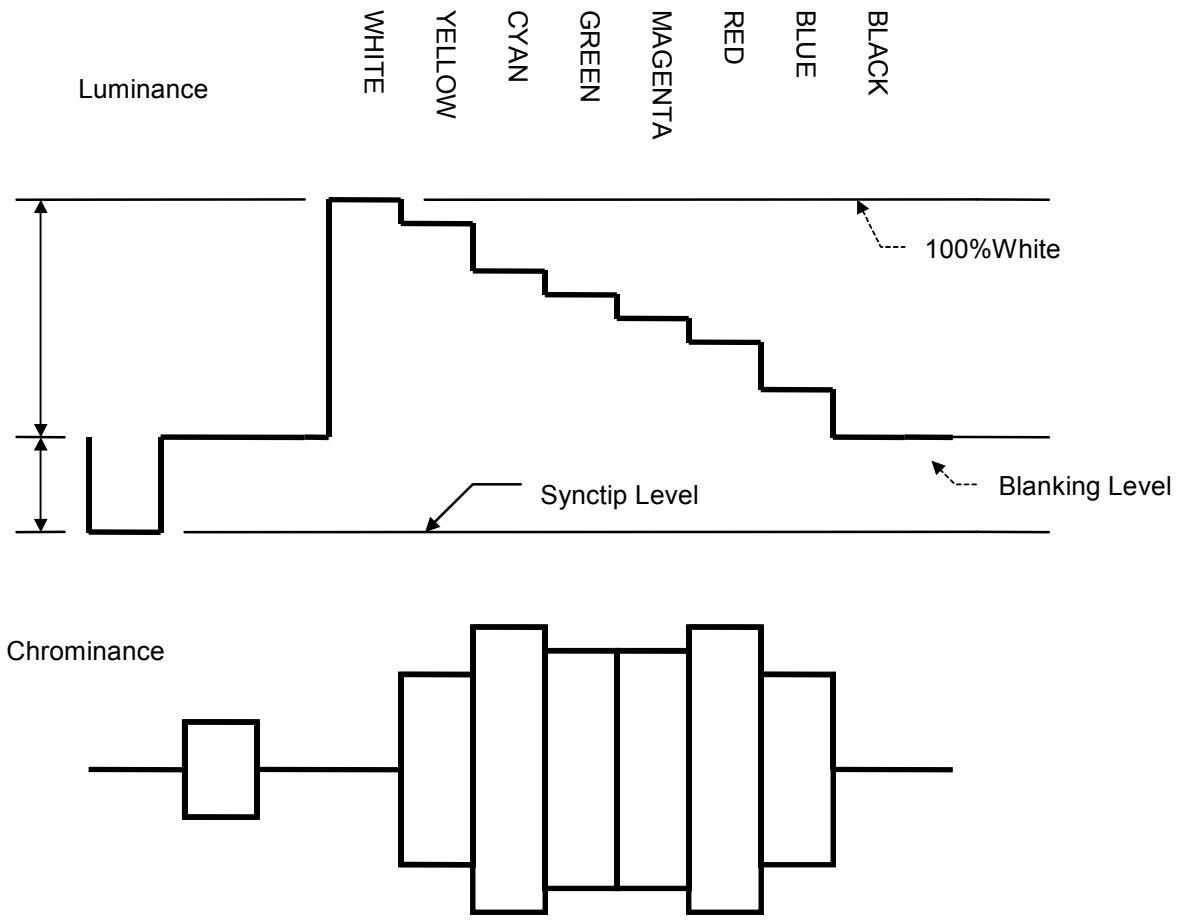

625 System



## ♦ Internal Color Bars Generator

AK8814 generates the Common Color Bar signal for NTSC and PAL internally. The generated Color Bar is “100% Amplitude, 100% Saturation”. When AK8814 is set to Black Burst output mode, AK8814 does not output Color bar even Color bar output register is set.




The following values are code for ITU-R. BT601

| | WHITE | YELLOW | CYAN | GREEN | MAGENTA | RED | BLUE | BLACK |
|---|---|---|---|---|---|---|---|---|
| Cb | 128 | 16 | 166 | 54 | 202 | 90 | 240 | 128 |
| Y | 235 | 210 | 170 | 145 | 106 | 81 | 41 | 16 |
| Cr | 128 | 146 | 16 | 34 | 222 | 240 | 110 | 128 |

## ♦ Internal Black Burst Generator

AK8814 generates Black burst signal for NTSC and PAL internally. When AK8814 is set to Black burst output mode, AK8814 works same operation as that the input Y/Cb/Cr data is 16/128/128. In this mode, AK8814 does not output Color bar even Color bar output register is set.

## ♦ I²C Control Sequence

AK8814 is controlled by I²C bus. The slave address can be selected as 40H or 42H by selecting SELA pin.

| SELA | SLAVE Address |
|---|---|
| PULL Down [Low] | 0x40 |
| PULL UP [High] | 0x42 |

Operation :

*Write Sequence:*

(a)1byte Write Sequence

| S | Slave Address | w | A | Sub Address | A | Data | A | Stp |
|---|---|---|---|---|---|---|---|---|
| | 8-bits | | 1-bit | 8-bits | 1-bit | 8-bits | 1-bit | |

(b) Sequential Write Operation

| S | Slave Address | w | A | Sub Address(n) | A | Data(n) | A | Data(n+1) | A | ••• | Data(n+m) | A | stp |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 8-bits | | 1-bit | 8-bits | 1-bit | 8-bits | 1-bit | 8-bits | 1-bit | | 8-bits | 1-bit | |

*Read Sequence:*

| S | Slave Address | w | A | Sub Address(n) | A | rS | Slave Address | R | A | Data1 | A | Data2 | A | Data3 | A | ••• | Data n | Ā | stp |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 8-bits | | 1 | 8-bits | 1 | | 8-bits | | 1 | 8-bits | 1 | 8-bits | 1 | 8-bits | 1 | | 8-bits | 1 | |

S, rS : Start Condition
A : Acknowledge (SDA Low )
Ā : Not Acknowledge (SDA High)
stp : Stop Condition
R/W 1 : Read 0 : Write

: Master device (Host)

: Slave device (AK8814)

| Sub Address | Name | R/W | Explanation |
|---|---|---|---|
| 00H | Interface Mode | R/W | Setting Interface mode |
| 01H | Video Process 1 | R/W | Setting Standard (NTSC, PAL etc.) |
| 02H | Video Process 2 | R/W | Setting Closed Caption/Extended Data/VBID |
| 03H | Video Process 3 | R/W | Setting Composite signal or Component Signal<br>Adjusting Chrominance/Luminance Delay |
| 04H | RESERVED | | |
| 05H | DAC Mode | R/W | Each DAC On/Off Switch |
| 06H | Sub C. Freq. | R/W | Adjusting Sub-carrier frequency |
| 07H | Sub C. Phase | R/W | Adjusting Sub-carrier phase |
| 08H | WSS Data 1 | R/W | WSS Data Register |
| 09H | WSS Data 2 | R/W | WSS Data Register |
| 1AH-15H | RESERVED | R/W | |
| 16H | Closed Caption R | R/W | Closed Caption Lower byte Data |
| 17H | Closed Caption R | R/W | Closed Caption Upper byte Data |
| 18H | Closed Caption R | R/W | Extended Lower byte Data |
| 19H | Closed Caption R | R/W | Extended Upper byte Data |
| 1AH | Video ID Data | R/W | Video ID Lower byte Data |
| 1BH | Video ID Data | R/W | Video ID Upper byte Data |
| 1CH-23H | RESERVED | | |
| 24H | STS Data | R | Status |
| 25H | Device ID | R | Device ID |
| 26H | Device REV | R | Revision |
| 27H-29H | RESERVED | | |

## Interface Mode Register (R/W only default A4H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 00H | BLN4 | BLN3 | BLN2 | BLN1 | BLN0 | FID | MAS | CCIR |

| Symbol | Value | Description | |
|---|---|---|---|
| BLN4 - BLN0 | ***** | Line Blanking No. | default 10100 |
| FID | 0<br>1 | Select VSYNC<br>Select FID | <br>default |
| MAS | 0<br>1 | Slave mode<br>Master mode When CCIR=0,it's valid | default |
| CCIR | 0<br>1 | CCIR656 non-decode<br>CCIR656 decode | default |

## Video Process 1 Register (R/W only default 18H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 01H | Reserved | CBG | SETUP | SCR | VM3 | VM2 | VM1 | VM0 |

| Symbol | Value | Description | |
|---|---|---|---|
| CBG | 0<br>1 | Video Encode<br>Generates color bar | default |
| SETUP | 0<br>1 | No Set-up<br>7.5 IRE Set-up | <br>default |
| SCR | 0<br>1 | Sub C. Phase Reset off<br>Standard Field Reset | <br>default |
| VM3 – VM2 | 00<br>01<br>10<br>11 | 525/60<br>525/60 PAL (PAL-M etc.)<br>Reserved<br>PAL | default |
| VM1-VM0 | 00<br>01<br>10<br>11 | 3.57954545 MHz<br>3.57561188 MHz (PAL-M only)<br>3.5820558 MHz<br>4.43361875 MHz | default |

Register Setting of each standard is showend as following ;

| | VM3-VM0 |
|---|---|
| NTSC-M | 0000 |
| PAL-B,D,G,H,I | 1111 |
| PAL-M | 0101 |
| PAL-60 | 0111 |
| NTSC4.43 | 0011 |

- When SCR is "ON", the Subcarrier Phase is reset every 4 fields for NTSC, every 8 fields for PAL.
- Even when SETUP is "ON", there is no Set-up (Pedestal) during the blanking lines.

## Video Process 2 Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 02H | Reserved | Reserved | Reserved | Reserved | WSS | CC284 | CC21 | VBID |

| Symbol | Value | Description | |
|---|---|---|---|
| CC284 | 0<br>1 | Extended Data OFF<br>ON | default |
| CC21 | 0<br>1 | Closed Caption OFF<br>ON | default |
| VBID | 0<br>1 | Video ID OFF<br>ON | default |
| WSS | 0<br>1 | WSS OFF<br>ON | default |

## Video Process 3 Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 03H | Reserved | VS | SYD2 | SYD1 | SYD0 | CYD2 | CYD1 | CYD0 |

| Symbol | Value | Description | |
|---|---|---|---|
| SYD2 - SYD0 | | S-Video Y Component<br>delay no. from Chroma: 2's comp. | default<br>000 |
| CYD2 - CYD0 | | Composite Y Component<br>delay no. from Chroma: 2's comp. | default<br>000 |

- S-video and Y component of the composite signal can be shifted for the chroma signal independently at ±3-system clock (27MHz).

## DAC Mode Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 05H | Reserved | Reserved | Reserved | Reserved | Reserved | OUTCP | OUTC | OUTY |

| Symbol | Value | Description | |
|---|---|---|---|
| OUTCP | 0 | Composite video signal or U signal output : OFF | default |
| | 1 | Composite video singal or U signal output : ON | |
| OUTC | 0 | Chroma signal or V signal output : OFF | default |
| | 1 | Chroma signal or V signal output : ON | |
| OUTY | 0 | Y signal output : OFF | default |
| | 1 | Y signal output : ON | |

- Video output of AK8814 (DAC) can be forced “OFF” independently.

  The output of DAC that is forced “OFF” is Hi-impedance. When three DACs are forced “OFF”, then the internal VREF is also forced “OFF”. In this case, it takes several miliseconds before the internal VREF reaches the proper voltage after any DAC becomes “ON”.

## SubC Freq. Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 06H | SUBF7 | SUBF6 | SUBF5 | SUBF4 | SUBF3 | SUBF2 | SUBF1 | SUBF0 |

| Symbol | Value | Description | |
|---|---|---|---|
| SUBF7-SUBF0 | | Adjustment of frequency between +127 and –128 step of 0.8Hz | default 0 |

- AK8814 generates the necessary sub-carrier frequency from a system clock by DFS (Digital Frequency Synthesizer)
- Frequency of default is adjustable by specifying this bit. This bit adjusts the default frequency.

## SubC Phase Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 07H | SUBP7 | SUBP6 | SUBP5 | SUBP4 | SUBP3 | SUBP2 | SUBP1 | SUBP0 |

| Symbol | Value | description | |
|---|---|---|---|
| SUBP7 – SUBP0 | | Step: (360° /256) | default 0 |

- Sub- carrier phase is adjustable by (360° /256) step.

## WSS Data Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 08H | G2-7 | G2-6 | G2-5 | G2-4 | G1-3 | G1-2 | G1-1 | G1-0 |
| 09H | Reserved | Reserved | G4-13 | G412 | G4-11 | G3-10 | G3-9 | G3-8 |

- Please write value 0 at Reserved bit.

## Closed Caption Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 16H | CC1[7] | CC1[6] | CC1[5] | CC1[4] | CC1[3] | CC1[2] | CC1[1] | CC1[0] |
| 17H | CC2[7] | CC2[6] | CC2[5] | CC2[4] | CC2[3] | CC2[2] | CC2[1] | CC2[0] |
| 18H | CC3[7] | CC3[6] | CC3[5] | CC3[4] | CC3[3] | CC3[2] | CC3[1] | CC3[0] |
| 19H | CC4[7] | CC4[6] | CC4[5] | CC4[4] | CC4[3] | CC4[2] | CC4[1] | CC4[0] |

| Symbol | Description | |
|---|---|---|
| CC1[7] – CC1[0]<br>CC2[7] – CC2[0] | Line 21 –1<br>Line 21 –2 | Closed Caption |
| CC3[7] – CC3[0]<br>CC4[7] – CC4[0] | Line 284 -1<br>Line 284 -2 | Extended Data |

- When the 2nd byte of Closed Caption Data and Extended Data is written in, AK8814 recognizes the renewed data and encodes it in the video line. When the data is not renewed AK8814 outputs NULL code.

## Video ID Data Register (R/W only default 00H)

| Sub Add | bit 7 | bit 6 | bit 5 | bit 4 | bit 3 | bit 2 | bit 1 | bit 0 |
|---|---|---|---|---|---|---|---|---|
| 1AH | Reserved | Reserved | bit 1 | bit 2 | bit 3 | bit 4 | bit 5 | bit 6 |
| 1BH | bit 7 | bit 8 | bit 9 | bit 10 | bit 11 | bit 12 | bit 13 | bit 14 |

- Please write value 0 at Reserved bit.
- Bit numbers correspond to Fig. 5 VBID code assignment.
- AK8814 generates CRC 6 bit data automatically.

Followings are read only register

## STATUS REGISTER (R only)

| Sub Add | bit7 | bit6 | bit5 | bit4 | bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|
| 24H | Reserved | Reserved | EN284 | EN21 | SYNC | STS2 | STS1 | STS 0 |

| Symbol | Value | Description |
|---|---|---|
| EN284 | 0<br>1 | Wait for the appointed video line to encode.<br>Ready for the C.C. data input to the register. |
| EN21 | 0<br>1 | Wait for the appointed video line to encode.<br>Ready for the C.C. data input to the register. |
| SYNC | 0<br>1 | Missing synchronization in slave mode.<br>Synchronization was achieved. |
| STS2 - STS 0 | *** | Shows the processing field No. |

- Status Register becomes effective when SYNC bit turns to “1”. When in master mode operation, this bit is ”1”.
- STS2-STS2 holds the field number of processing. Some time lag is inevitable for the $I^2C$ acquisition.
- Closed caption data should be renewed after firm that the EN* flag is “1”. EN* flag bit is cleared after the second byte( Sub address 17H,19H) was accessed.
- Reserved-bit is always value 0.

| Sub Add | bit7 | bit6 | bit5 | bit4 | Bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|
| 25H | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |

- Represents device ID. 14H is assigned for AK8814.

## Device REV (R only default 01H)

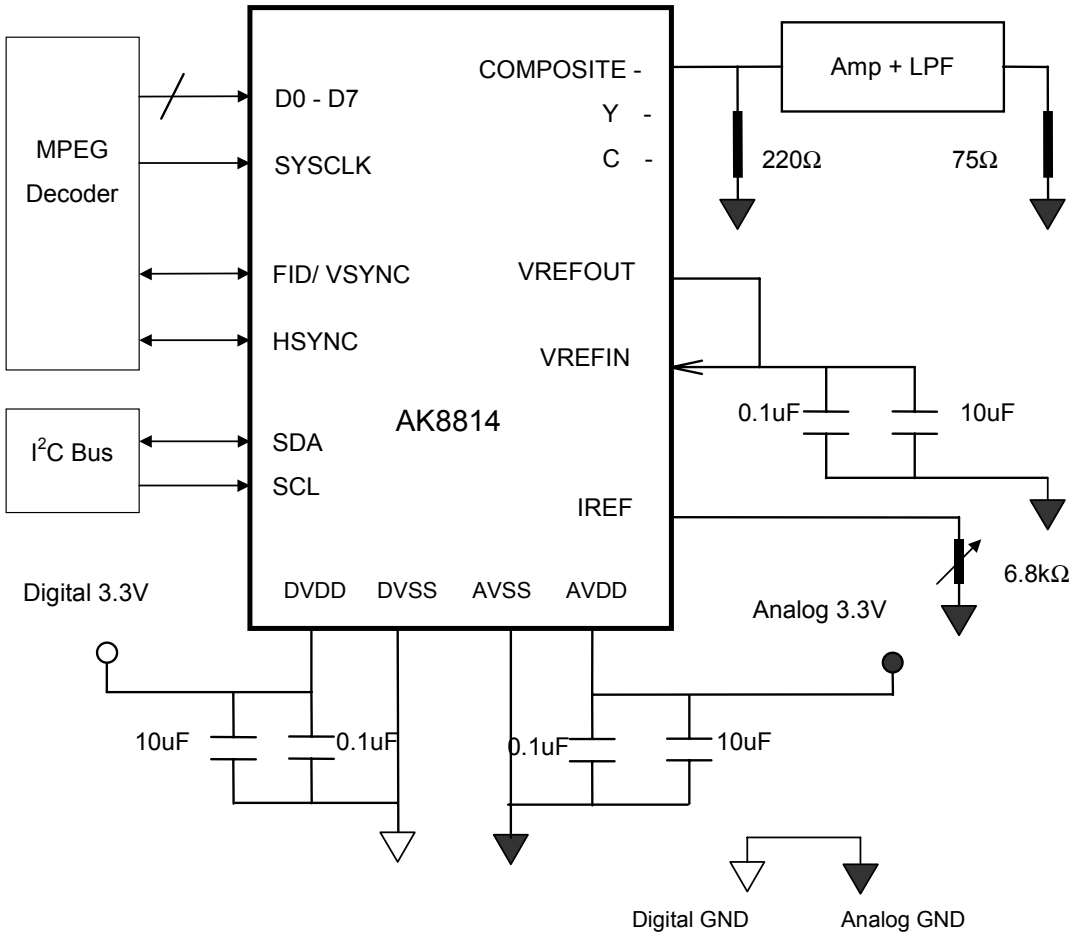
| Sub Add | bit7 | bit6 | bit5 | bit4 | Bit3 | bit2 | bit1 | bit0 |
|---|---|---|---|---|---|---|---|---|
| 26H | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

- Represents device revision. Initial is 01H.

Macrovision Register Map

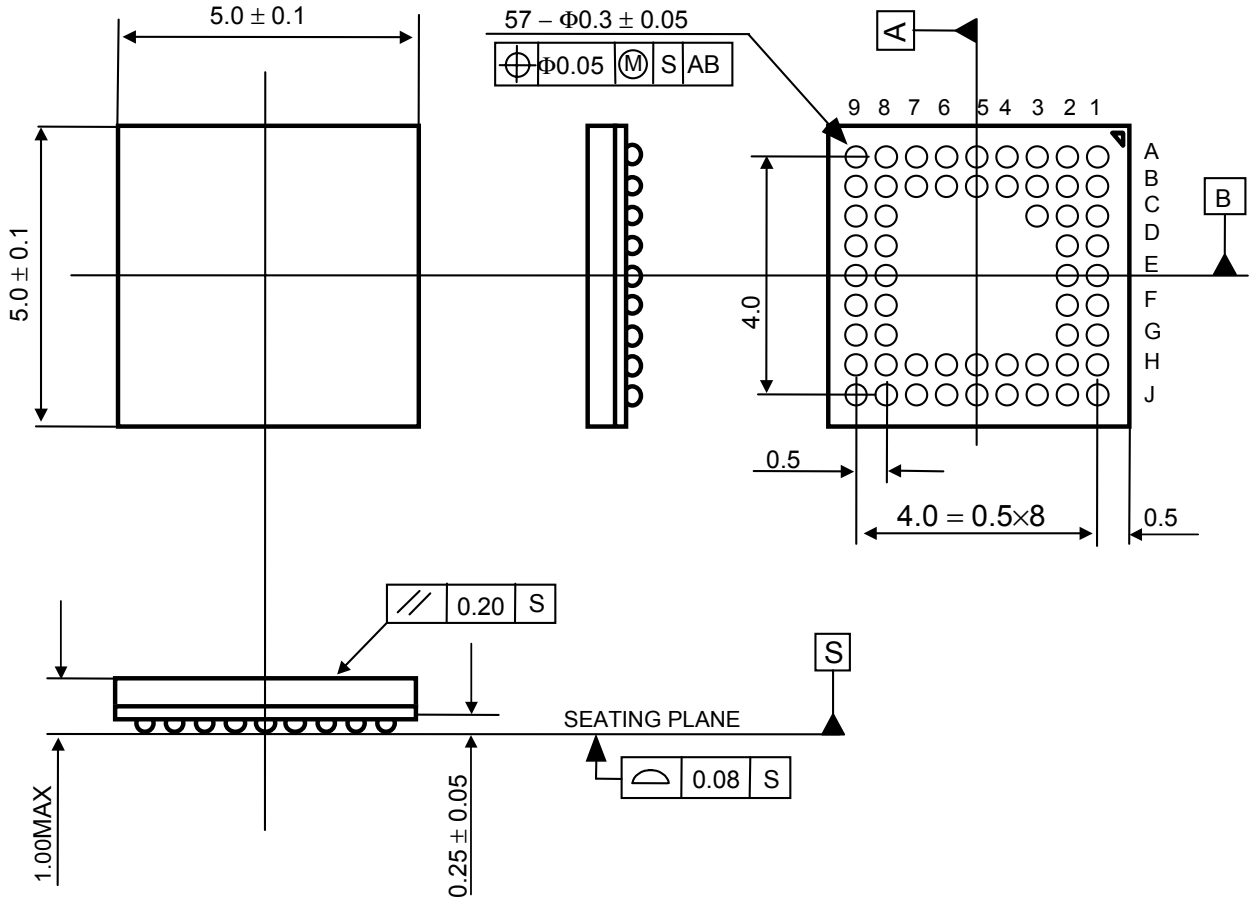
| Register | | bit-7 | bit-6 | bit-5 | bit-4 | bit-3 | bit-2 | bit-1 | bit-0 |
|---|---|---|---|---|---|---|---|---|---|
| 0x0A | :CSP32 | - | - | - | - | CPS32[3] | CPS32[2] | CPS32[1] | CPS32[0] |
| 0x0B | CPS31:CPS30 | CPS31[3] | CPS31[2] | CPS31[1] | CPS31[0] | CPS30[3] | CPS30[2] | CPS30[1] | CPS30[0] |
| 0x0C | CPS29:CPS28 | CPS29[3] | CPS29[2] | CPS29[1] | CPS29[0] | CPS28[3] | CPS28[2] | CPS28[1] | CPS28[0] |
| 0x0D | CPS27:CPS26 | CPS27[3] | CPS27[2] | CPS27[1] | CPS27[0] | CPS26[3] | CPS26[2] | CPS26[1] | CPS26[0] |
| 0x0E | CPS25:CPS24 | CPS25[3] | CPS25[2] | CPS25[1] | CPS25[0] | CPS24[3] | CPS24[2] | CPS24[1] | CPS24[0] |
| 0x0F | CPS23:CPS22 | CPS23[3] | CPS23[2] | CPS23[1] | CPS23[0] | CPS22[3] | CPS22[2] | CPS22[1] | CPS22[0] |
| 0x10 | CPS21:CPS20 | CPS21[3] | CPS21[2] | CPS21[1] | CPS21[0] | CPS20[3] | CPS20[2] | CPS20[1] | CPS20[0] |
| 0x11 | CPS19:CPS18 | CPS19[3] | CPS19[2] | CPS19[1] | CPS19[0] | CPS18[3] | CPS18[2] | CPS18[1] | CPS18[0] |
| 0x12 | CPS17:CPS16 | CPS17[3] | CPS17[2] | CPS17[1] | CPS17[0] | CPS16[3] | CPS16[2] | CPS16[1] | CPS16[0] |
| 0x13 | CPS15:CPS14 | CPS15[3] | CPS15[2] | CPS15[1] | CPS15[0] | CPS14[3] | CPS14[2] | CPS14[1] | CPS14[0] |
| 0x14 | CPS13:CPS12 | CPS13[3] | CPS13[2] | CPS13[1] | CPS13[0] | CPS12[3] | CPS12[2] | CPS12[1] | CPS12[0] |
| | | | | | | | | | |
| 0x1D | CPC1:CPC0 | CPC1[3] | CPC1[2] | CPC1[1] | CPC1[0] | CPC0[3] | CPC0[2] | CPC0[1] | CPC0[0] |
| 0x1E | CPS11:CPS10 | CPS11[3] | CPS11[2] | CPS11[1] | CPS11[0] | CPS10[3] | CPS10[2] | CPS10[1] | CPS10[0] |
| 0x1F | CPS9:CPS8 | CPS9[3] | CPS9[2] | CPS9[1] | CPS9[0] | CPS8[3] | CPS8[2] | CPS8[1] | CPS8[0] |
| 0x20 | CPS7:CPS6 | CPS7[3] | CPS7[2] | CPS7[1] | CPS7[0] | CPS6[3] | CPS6[2] | CPS6[1] | CPS6[0] |
| 0x21 | CPS5:CPS4 | CPS5[3] | CPS5[2] | CPS5[1] | CPS5[0] | CPS4[3] | CPS4[2] | CPS4[1] | CPS4[0] |
| 0x22 | CPS3:CPS2 | CPS3[3] | CPS3[2] | CPS3[1] | CPS3[0] | CPS2[3] | CPS2[2] | CPS2[1] | CPS2[0] |
| 0x23 | CPS1:CPS0 | CPS1[3] | CPS1[2] | CPS1[1] | CPS1[0] | CPS0[3] | CPS0[2] | CPS0[1] | CPS0[0] |

## SYSTEM CONNECTION EXAMPLE



# PACKAGE

57Pin FBGA

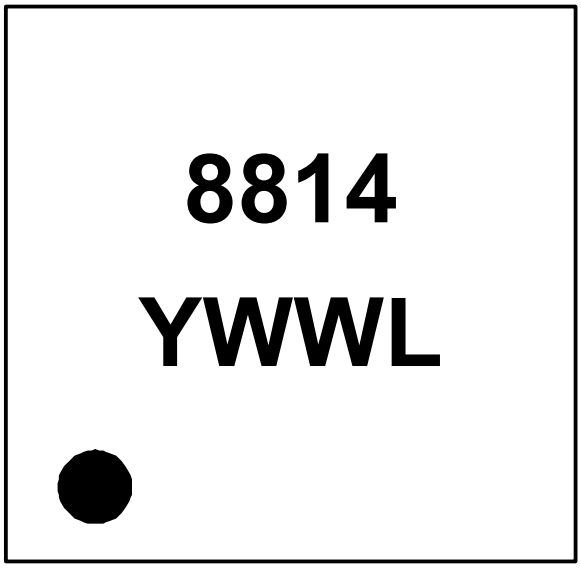



Package & Lead frame material

Package molding compound: Epoxy

Interposer material: BT resin

## MARKING




1) Pin #1 indication
2) Marketing Code : 8813
3) Date Code : YWWL (4 digits)
   Y: Year
   WW: week
   L: Lot

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