

AsahiKASEI

ASAHI KASEI EMD

Preliminary**AK8825****HD/SD Multi Format Video Encoder with 3ch DAC****Notice**

AKM does not ship this product (the AK8825) to customers who are not licensed by ROVI corp.

General Description

The AK8825 is a HD/SD TV Video Encoder with onchip 3-channel 10bit DAC.

As input data, in SDTV encoder mode, SMTE-125M / ITUR-R.BT601, 656 compatible Y/Cb/Cr 4:2:2 formats (8bit) are accepted and in HDTV encoder mode, SMPTE-274M (1080i), SMPTE296M (720p) compatible Y/Cb/Cr 4:2:2 formats (8bit x 2) are accepted.

As input data capture method, either a Synchronous mode to be made by detecting encoded EAV signal or a mode to synchronize with externally-fed H/V SYNC signal is selectable.

Outputs of CVBS / SDY / SDC and HDY / HDPB / HDPR and R / G / B analog signal can be output exclusively.

VBI signal and Macrovision signal can be also superimposed on output in addition to Video signals by register setting.

AK8825 supports I2C compatible interface as Micro-Processor interface.

Features**Component Video Encoder**

- Compatible Input Data
 - SMPTE125M-1995 / ITU-R BT601 (525i/625i)
 - SMPTE293M-1996 / ITU-R BT1358 (525p/625p)
 - SMPTE274M-1998 (1080i)
 - SMPTE296M-2001 (720p)
- Input Signal Format (525i / 625i, 525p / 625p, 1080i, 720P)
 - Y/Cb/Cr 4:2:2 (8bit x 1: 525i/625i)
 - Y/Cb/Cr 4:2:2 (8bit x 2: 525p/625p/1080i/720p)
 - RGB 6:6:6
 - RGB 5:6:5
- Input Clock
 - 27MHz (525i / 625i / 525p / 625p) / 74.25MHz (1080i/720p)
- Output Signals
 - Y/Pb/Pr Interlace
 - Y/Pb/Pr Progressive
 - (EIA 770.2, EAI 770.3)
- Input Signal Synchronization
 - ITU-R.BT 656 I/F (EAV Decode)
 - Slave operation by HSYNC / VSYNC
 - (525i: ITU-R. BT601 Compatible 625i / 525p / 625p / 1080i / 720p; CEA-861-D Compatible)
- VBID (CGMS-A), CC/XDS, WSS, CEA-805-B (Type A/B)
- Macrovision 525i / 625i Rev.7.1.1L, 525p/625p Macrovision Progressive 1.2
- Internal Color bar Generator
- Internal Black Burst Generator
- Adjustable Y / Pb / Pr Delay Function

NTSC / PAL Composite Video Encoder

- NTSC-M, PAL-B, D, G, H, I, M, N Encoding
- Composite Video Output / S-Video Output
- Compatible Input Data
 - SMPTE125M-1995 / ITU-R BT601(525i/625i) Y/Cb/Cr 4:2:2 (8bit x 1)
 - RGB 6:6:6
 - RGB 5:6:5
- Input Signal Synchronization
 - ITU-R.BT 656 I/F (EAV Decode)
 - Slave operation by HSYNC / VSYNC
 - (525i / 625i: ITU-R. BT601 Compatible)
- Input Clock
 - 27MHz
- VBID(CGMS-A), CC/XDS, WSS
- Macrovision Rev. 7.1.L



RGB Video DAC

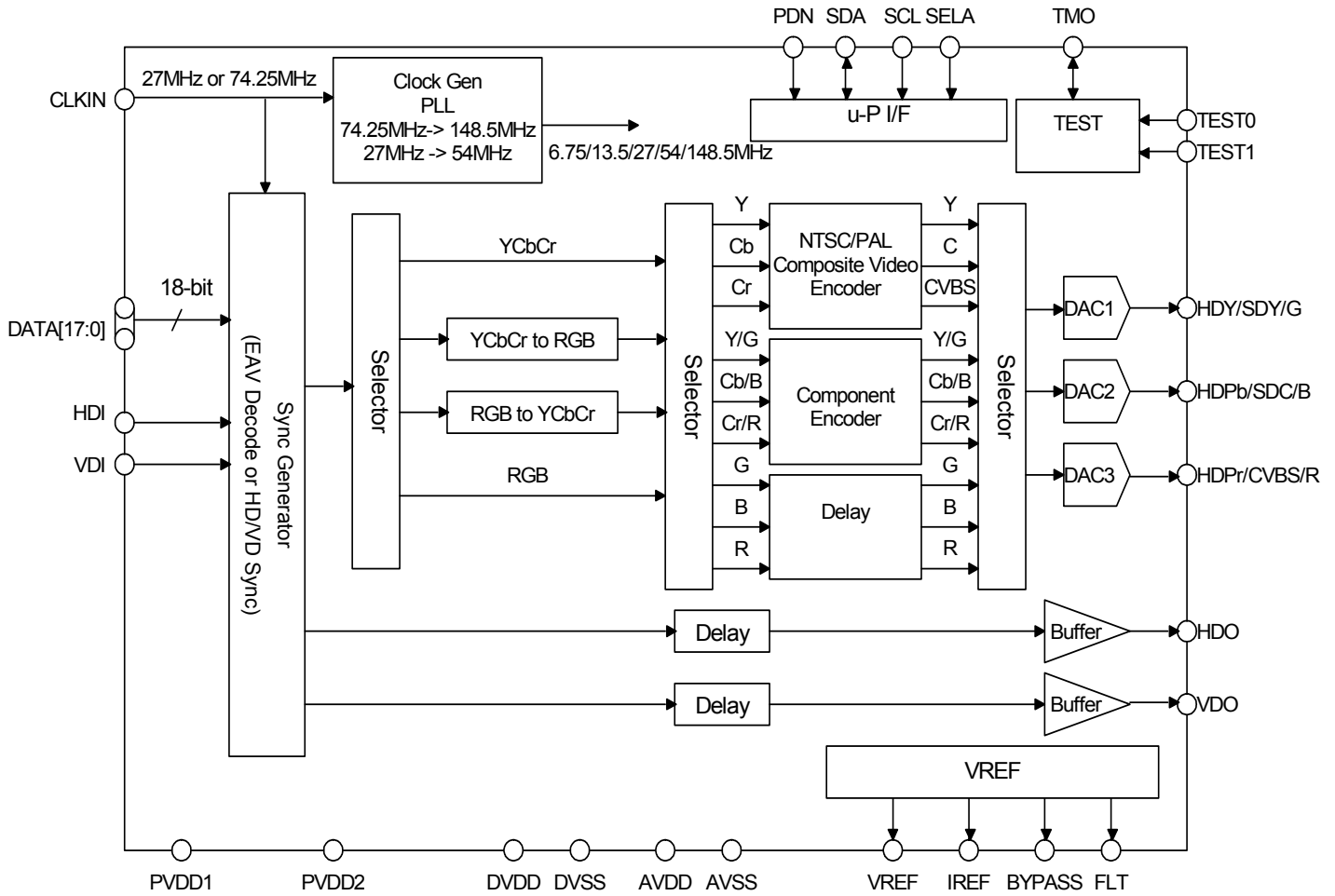
- RGB output
- Input Data Format
 - RGB 6:6:6
 - RGB 5:6:5
- Input Clock
 - 54MHz (max)

Common Specification

- 10bit DAC x 3ch (max operating speed 150MHz)
- I²C BUS I/F (400kHz) compatible
- Power Down mode
- Internal VREF Circuit
- 3.0V / 1.8V VCC
- 57pin FBGA (5mm x 5mm)

* This device is protected by U.S. patent numbers 4,631,603, 4,577,216, and 4,819,098, and other intellectual rights. The use of Macrovision's copy protection technology in the device must be authorized by Macrovision and is intended for home and other limited pay-per-view use only, unless otherwise authorized in written by Macrovision. Reverse engineering or disassembly is prohibited.

1. Block Diagram


Fig. 1 Block Diagram

With Register setting, AK8825 works as

- Multi-Format Component Video Encoder (Component Video Encoder)
- NTSC/PAL Composite Video Encoder (Composite Video Encoder)
- High Speed Video DAC

1-1. Component Video Encoder Block

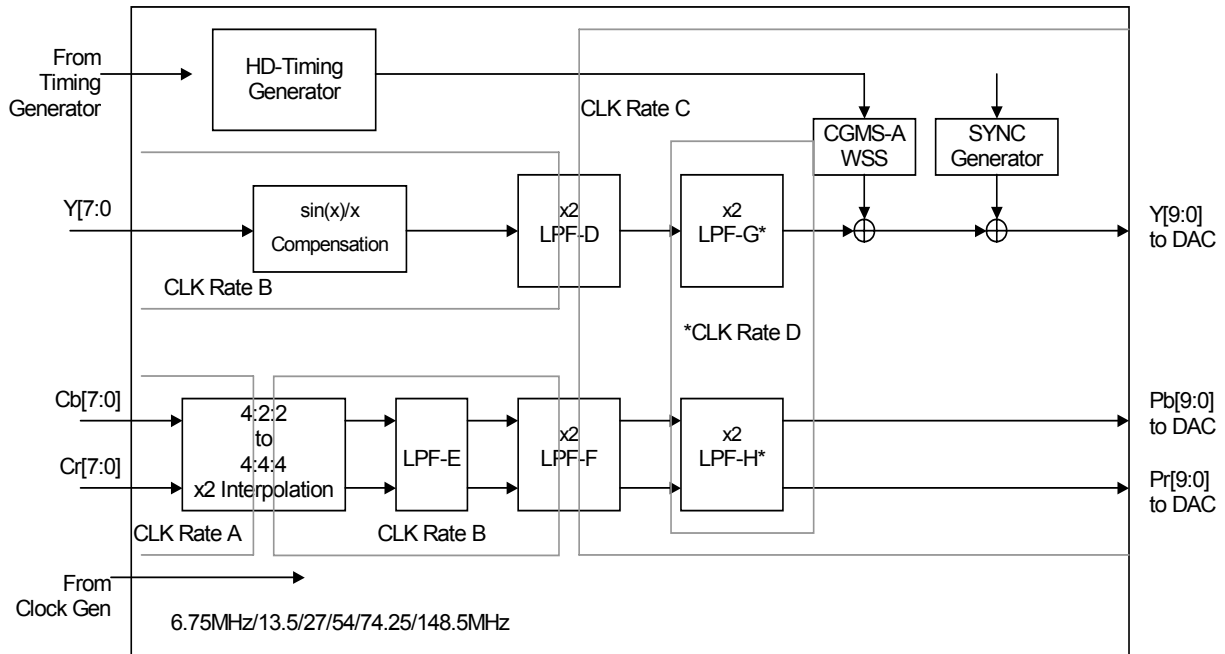


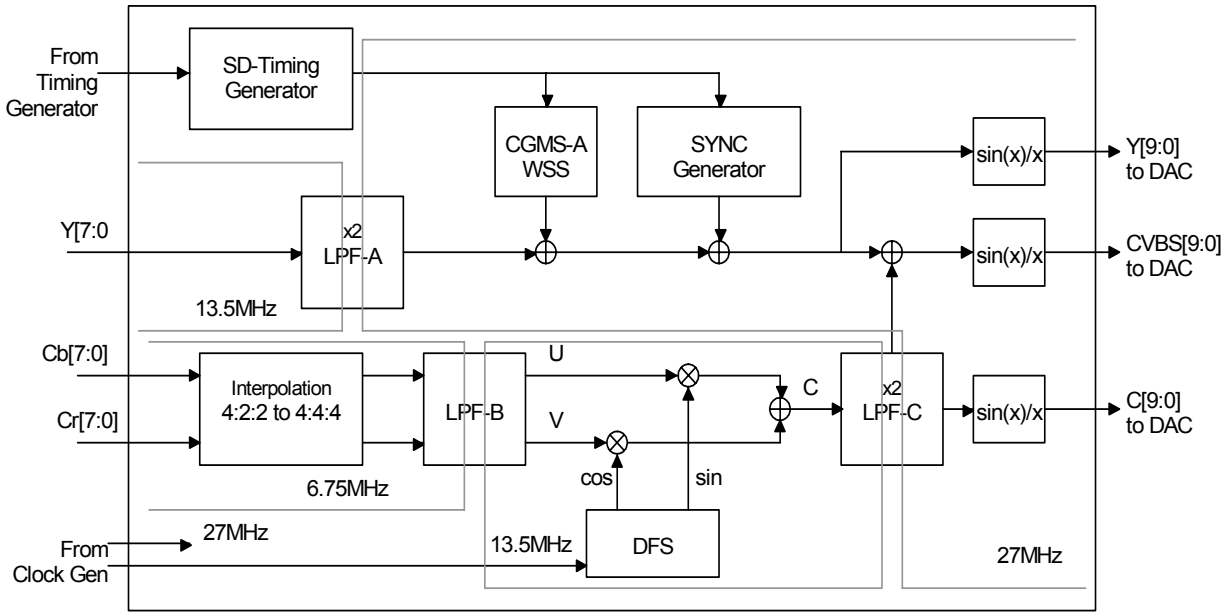
Fig. 2 Component Video Encoder Block

This Block described as Component Video Encoder Block in this datasheet.
CLK Rate D is only a case of D1(525i/625i) mode.

Clock Rate

	D1(525i /625i)	D2(525P / 625P)	D3/D4(1080i/720P)
CLK Rate A	6.75MHz	13.5MHz	37.125MHz
CLK Rate B	13.5MHz	27MHz	74.25MHz
CLK Rate C	27MHz	54MHz	148.5MHz
CLK Rate D	54MHz	-	-

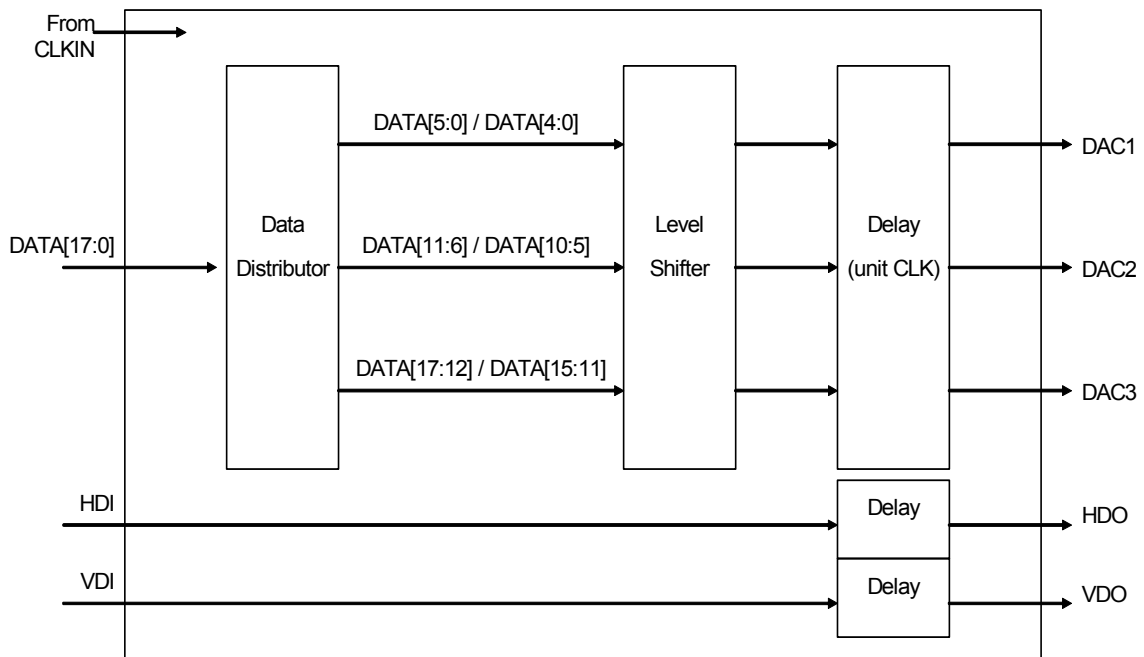
1-2. NTSC/PAL Composite Video Encoder Block


Fig. 3 Composite Video Encoder Block

This Block described as Composite Video Encoder Block in this datasheet.

1-3 High Speed Video DAC mode

AK8825 can be used as High Speed Video DAC. This mode is described as Video DAC mode in this datasheet.


Fig. 4 High Speed Video ADC Block