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AK8854VQ
Multi-Format Digital Video Decoder

Overview

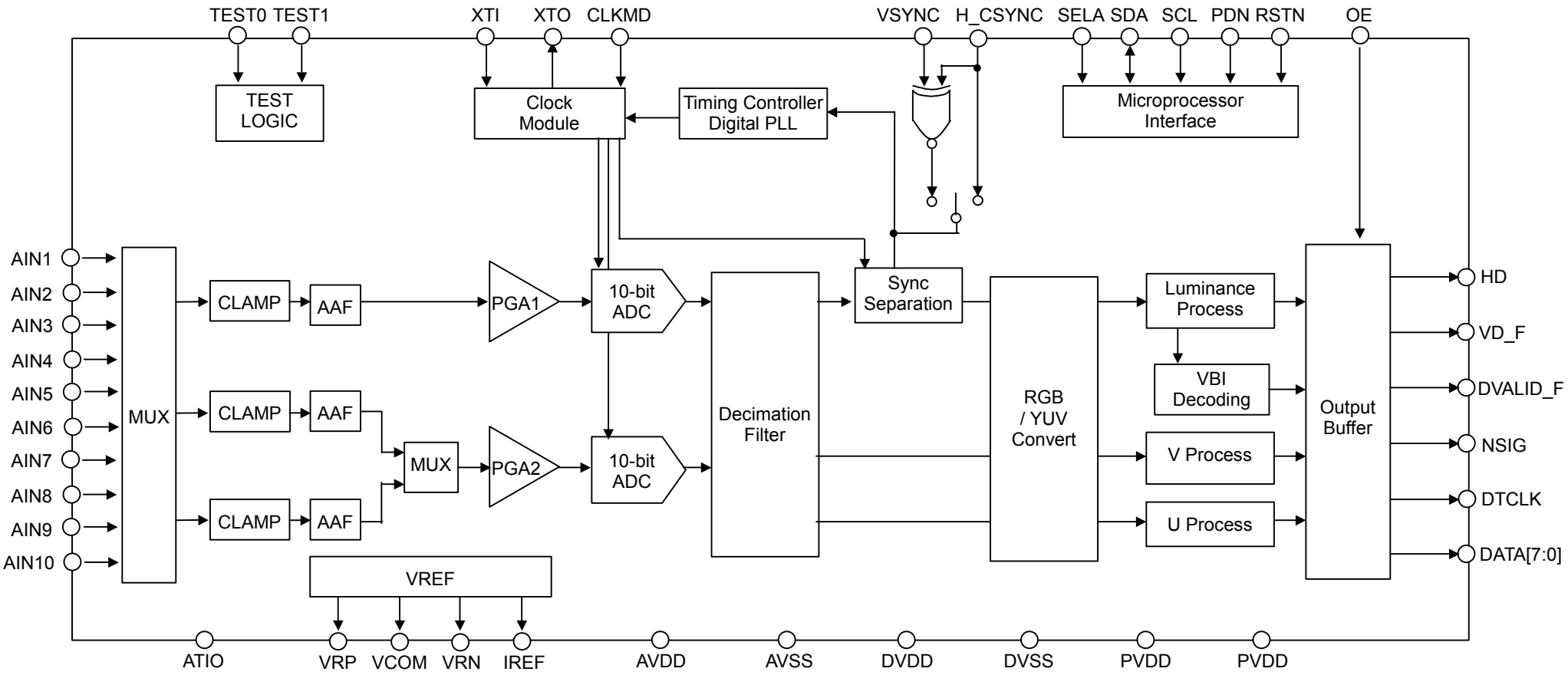
The AK8854VQ is a single-chip digital video decoder for composite, s-video, component YPbPr and RGB video signals. In case of RGB, AK8854VQ support Sync on Green,CSYNC and H/VSYNC as sync signal. Its output data is in YCbCr format, compliant with ITU-R BT.601. Its pixel clock, with a generated clock rate of 27 MHz, synchronizes with the input signal. Its output interface is ITU-R BT.656 compliant. Microprocessor access is via a I^2C interface. The operating temperature range is −40°C to 85°C. The package is 64-terminal LQFP.

Features

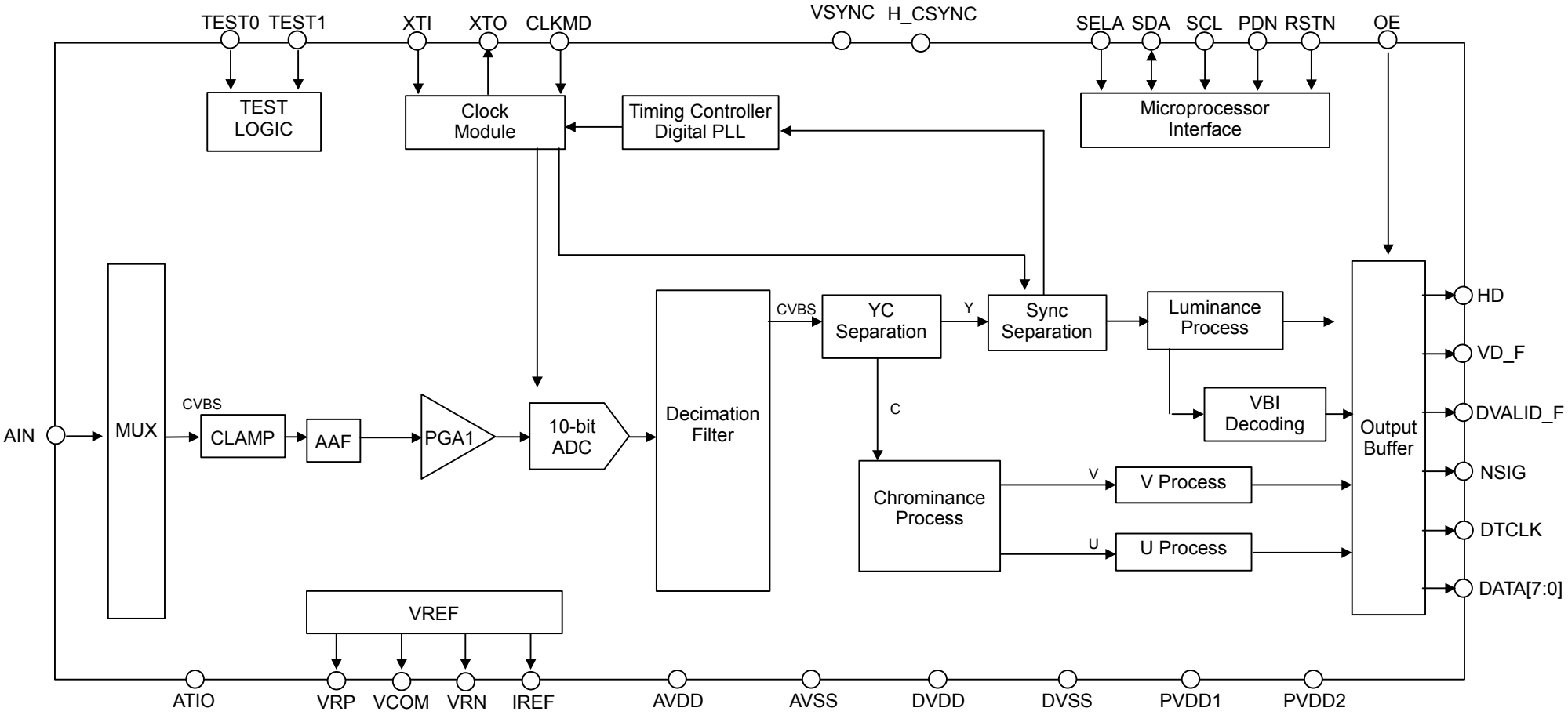
- Decodes composite video signals NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60), SECAM.
- Decodes S-video video signals NTSC (J, M, 4.43), PAL (B, D, G, H, I, M, N, Nc, 60), SECAM.
- Decodes component YPbPr video signals 525i, 625i.
- Decodes component RGB video signals 525i, 625i and Non interlace.
- Ten input channels, with internal video switch.
- 10-bit ADC 2 channel.
- Internal line-locked and frame-locked PLLs for generation of clock synchronized with input signal.
- Internal PGA (-6 dB to 6 dB).
- Adaptive automatic gain control (AGC).
- Auto color control (ACC).
- Image adjustment (contrast, saturation, brightness, hue, sharpness).
- Automatic input signal detection.
- Adaptive 2-D Y/C separation.
- PAL decoding phase correction.
- ITU-R BT.656 and ITU-R BT.601 format output (with 4:2:2_8 bit parallel_EAV/SAV)
- Closed-caption signal decoding (output via register).
- WSS signal decoding (output via register).
- Macrovision signal detection (Macrovision certification).
- Power down function.
- I^2C control.
- 1.70~2.00 V core power supply.
- 1.70~3.60 V interface power supply.
- Operating temperature range: −40°C to 85°C.
- 64-pin LQFP package.

1. Functional block diagram

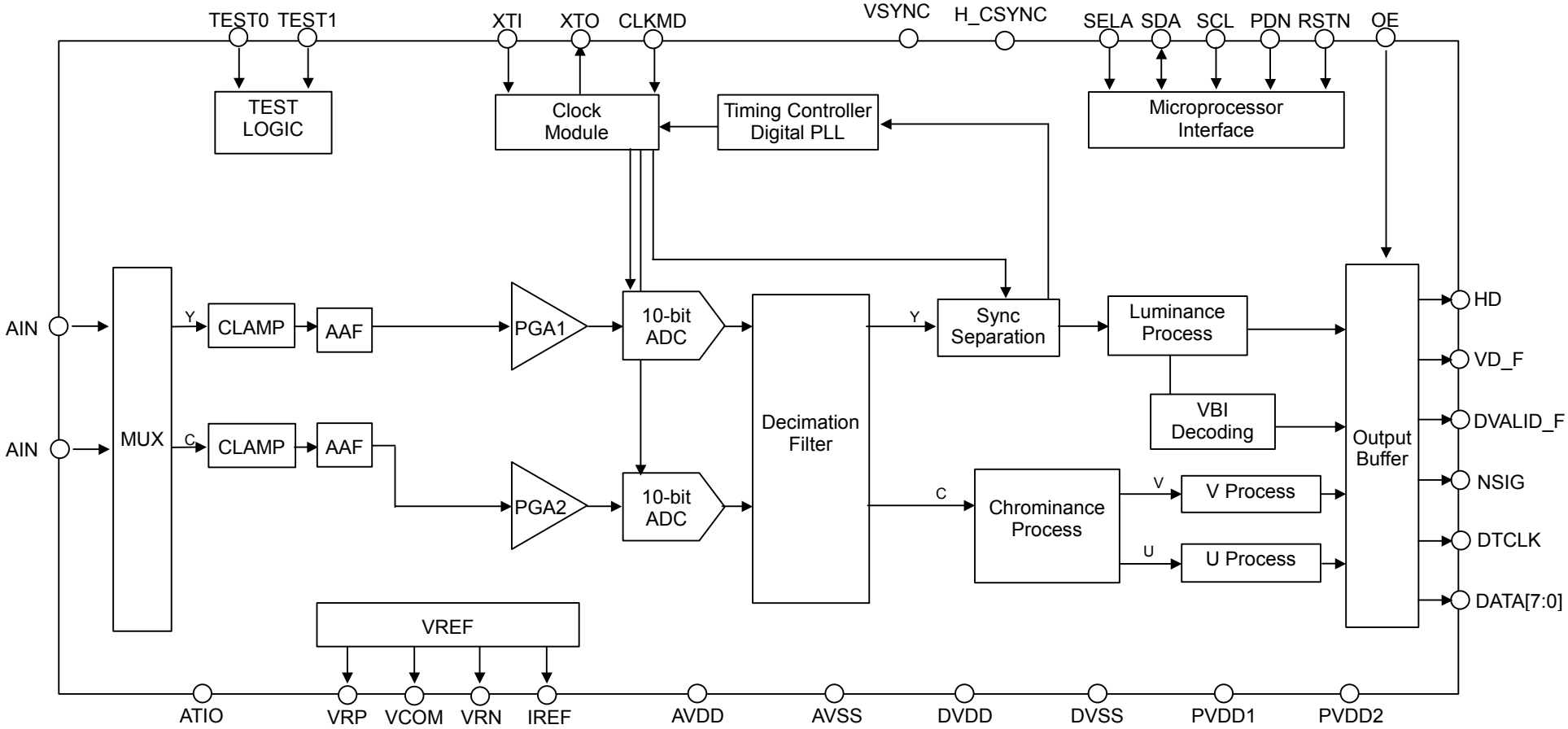
[General block diagram]



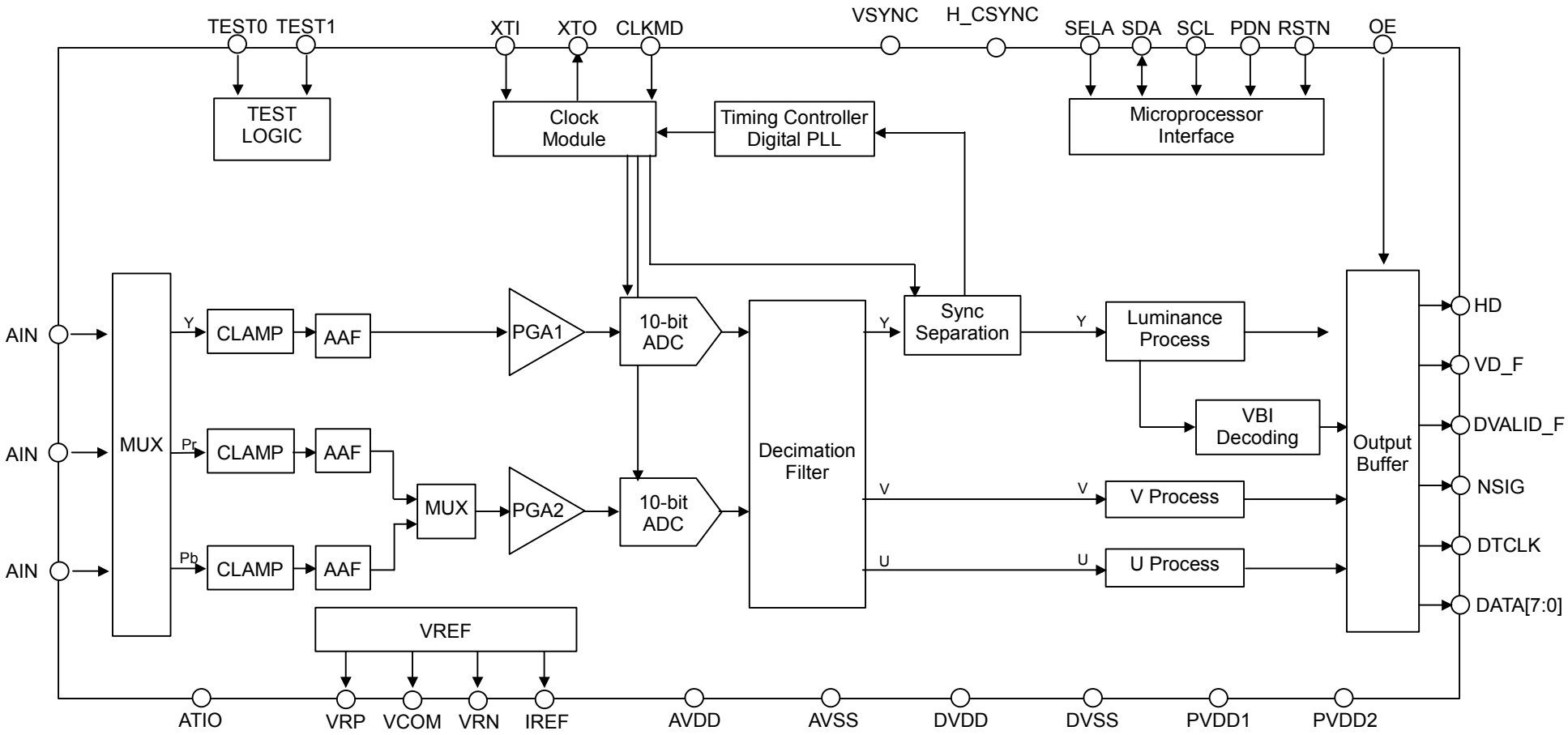
[CVBS decode block diagram]



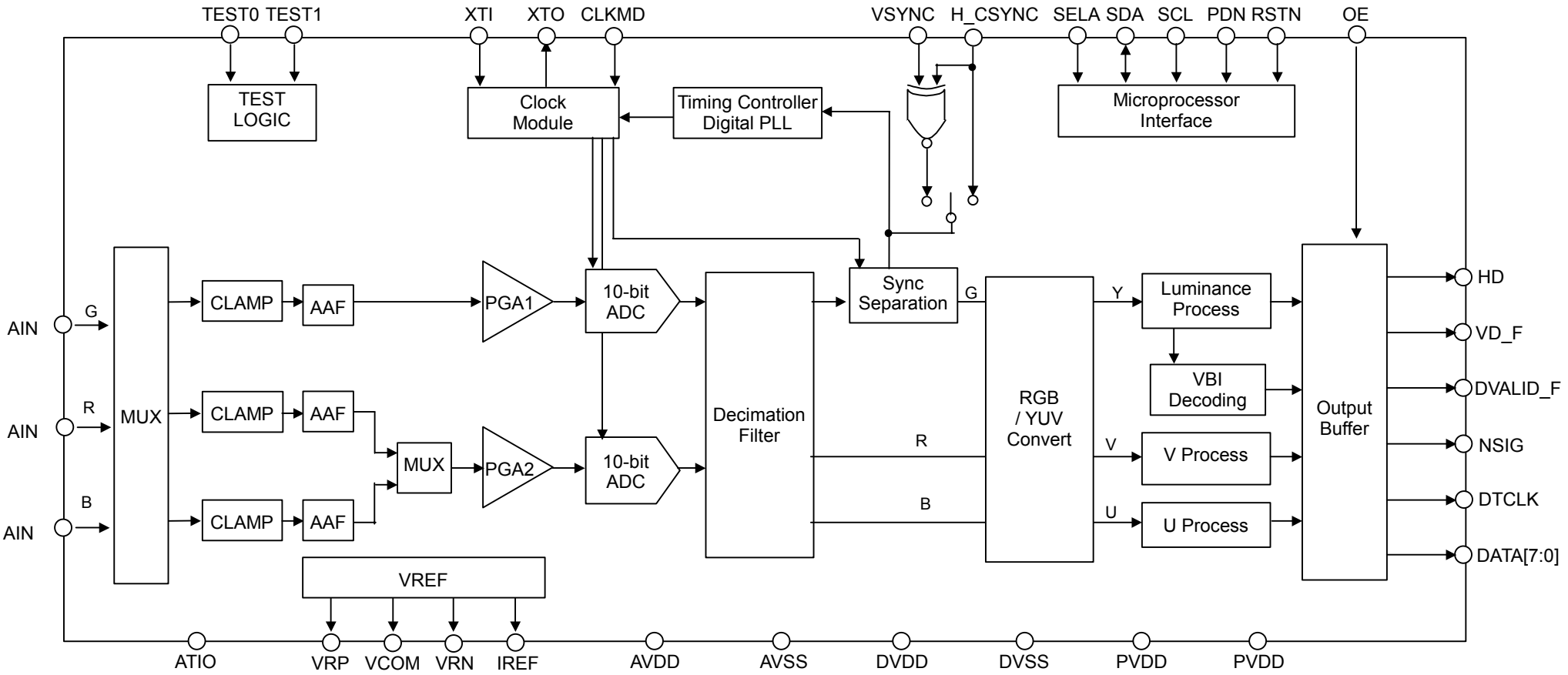
[S-video decode block diagram]



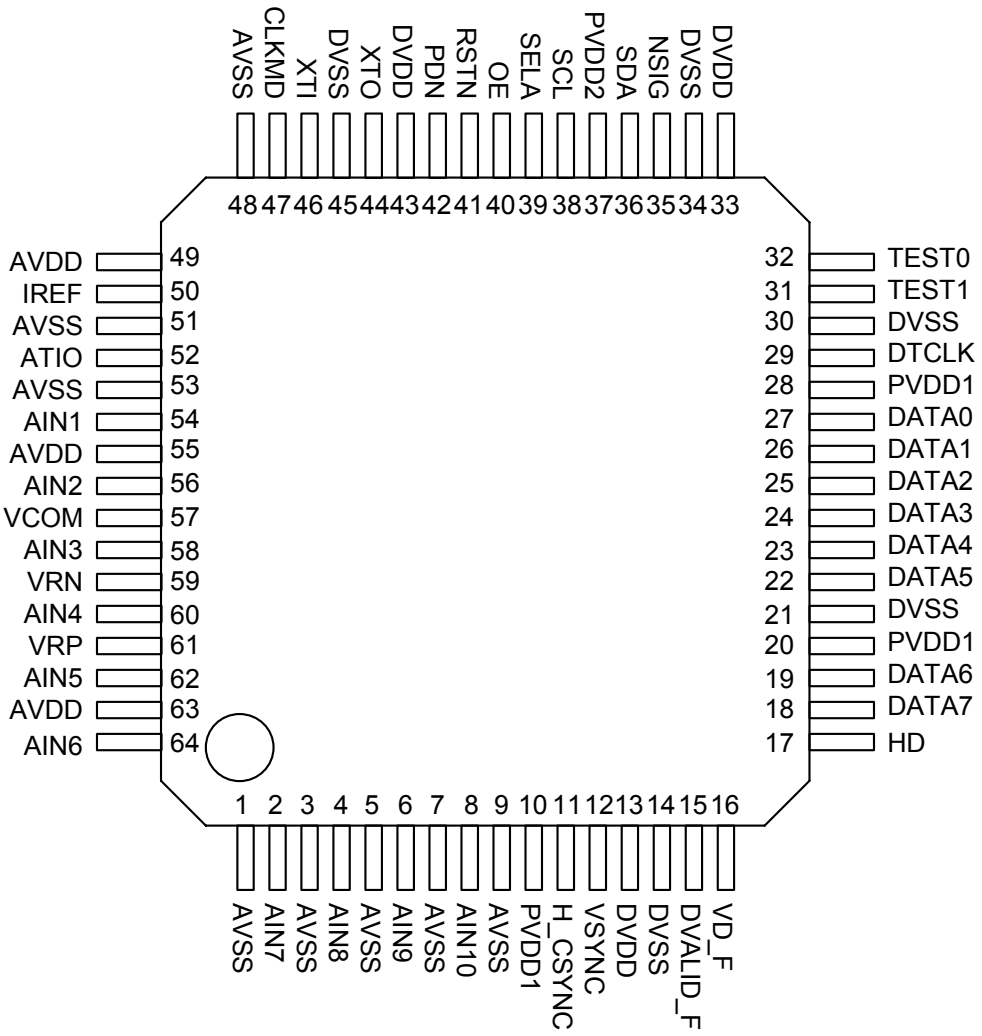
[YPbPr decode block diagram]



[RGB decode block diagram]



2. Pin assignment – 64 pins LQFP



3. Pin functions

Pin No.	Symbol	P/S[1]	I/O[2]	Description
1	AVSS	A	G	Analog ground pin.
2	AIN7	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
3	AVSS	A	G	Analog ground pin.
4	AIN8	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
5	AVSS	A	G	Analog ground pin.
6	AIN9	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
7	AVSS	A	G	Analog ground pin.
8	AIN10	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
9	AVSS	A	G	Analog ground pin.
10	PVDD1	P1	P	I/O power supply pin.
11	H_CSYNC	P1	I	External H-Sync or CSYNC signal input pin. If it is not used, connect to DVSS.
12	VSYNC	P1	I	External V-Sync signal input pin. If it is not used, connect to DVSS.
13	DVDD	D	P	Digital power supply pin.
14	DVSS	D	G	Digital ground pin.
15	DVALID_F	P1	O (I/O)	DVALID/FIELD signal output pin. DVALID and FIELD output signals switched by register setting. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
16	VD_F	P1	O	Vertical timing/ field timing signal output pin. VD and FIELD output signals switched by register setting. See Table below for relation of output to OE, PDN and RSTN pin status.
17	HD	P1	O (I/O)	Horizontal timing signal output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
18	DATA7	P1	O (I/O)	Data output pin. (MSB) Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
19	DATA6	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
20	PVDD1	P1	P	I/O power supply pin.
21	DVSS	D	G	Digital ground pin.

[1]Power supply: A, AVDD; D, DVDD; P1, PVDD1; P2, PVDD2.
[2]Input/Output: O, output pin; I, intput pin; I/O, input/output pin; P, power supply pin;
G, ground connection pin.

Pin No.	Symbol	P/S[1]	I/O[2]	Description
22	DATA5	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
23	DATA4	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
24	DATA3	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
25	DATA2	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
26	DATA1	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
27	DATA0	P1	O (I/O)	Data output pin. Used as I/O pin in Test Mode. See Table below for relation of output to OE, PDN and RSTN pin status.
28	PVDD1	P1	P	I/O power supply pin.
29	DTCLK	P1	O	Data clock output pin. Approx. 27 MHz clock output. See Table below for relation of output to OE, PDN and RSTN pin status.
30	DVSS	D	G	Digital ground pin.
31	TEST1	D	I	Pin for test mode setting. Connect to DVSS.
32	TEST0	D	I	Pin for test mode setting. Connect to DVSS.
33	DVDD	D	P	Digital power supply pin.
34	DVSS	D	G	Digital ground pin.
35	NSIG	P2	O	Shows status of synchronization with input signal. Low: Signal present (synchronized). High: Signal not present or not synchronized. See Table below for relation of output to OE, PDN, RSTN pin status.
36	SDA	P2	I/O	I^2C data pin. Connect to PVDD2 via a pull-up register. Hi-z input possible when PDN=L. Will not accept SDA input during reset sequence.
37	PVDD2	P2	P	Microprocessor I/F power supply pin.
38	SCL	P2	I	I^2C clock input pin. Use PVDD2 or lower for input. Hi-z input possible when PDN=L. Will not accept SCL input during reset sequence.
39	SELA	P2	I	I^2C bus address selector pin. PVDD2 connection: Slave address [0x8A] DVSS connection: Slave address [0x88]

[1]Power supply: A, AVDD; D, DVDD; P1, PVDD1; P2, PVDD2.
[2]Input/Output: O, output pin; I, intput pin; I/O, input/output pin; P, power supply pin;
G, ground connection pin.

Pin No.	Symbol	P/S[1]	I/O[2]	Description
40	OE	P2	I	Output enable pin. L: Digital output pin in Hi-z output mode. H: Data output mode. Hi-z input to OE pin is prohibited.
41	RSTN	P2	I	Reset signal input pin. Hi-z input is prohibited. L: Reset. H: Normal operation.
42	PDN	P2	I	Power-down control pin. Hi-z input is prohibited. L: Power-down. H: Normal operation.
43	DVDD	D	P	Digital power supply pin.
44	XTO	D	O	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 11. Use 24.576 MHz crystal. When PDN=L, output level is DVSS. If crystal is not used, connect to NC or DVSS.
45	DVSS	D	G	Digital ground pin.
46	XTI	D	I	Crystal connection pin. Connect to digital ground via 22 pF capacitor as shown in Sec. 11. Use 24.576 MHz crystal resonator. For input from 24.576 MHz crystal oscillator, use this pin.
47	CLKMD	D	I	Clock mode selection pin. Connect to DVDD or DVSS. DVSS connection: For crystal. DVDD connection: For quartz generator or other external clock input; not for crystal.
48	AVSS	A	G	Analog ground pin.
49	AVDD	A	P	Analog power supply pin.
50	IREF	A	O	Reference current setting pin. Connect to ground via 6.8 kΩ (≤1% accuracy) resistor.
51	AVSS	A	G	Analog ground pin.
52	ATIO	A	I/O	Analog test pin. For normal operation, connect to AVSS.
53	AVSS	A	G	Analog ground pin.
54	AIN1	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
55	AVDD	A	P	Analog power supply pin.
56	AIN2	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
57	VCOM	A	O	Common internal voltage for AD convertor. Connect to AVSS via ≥0.1 µF ceramic capacitor.
58	AIN3	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
59	VRN	A	O	Internal reference negative voltage pin for AD converter. Connect to AVSS via ≥0.1 µF ceramic capacitor.

[1]Power supply: A, AVDD; D, DVDD; P1, PVDD1; P2, PVDD2.
[2]Input/Output: O, output pin; I, intput pin; I/O, input/output pin; P, power supply pin; G, ground connection pin.

Pin No.	Symbol	P/S[1]	I/O[2]	Description
60	AIN4	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
61	VRP	A	O	Internal reference positive voltage pin for AD converter. Connect to AVSS via ≥0.1 µF ceramic capacitor.
62	AIN5	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.
63	AVDD	A	P	Analog power supply pin.
64	AIN6	A	I	Analog video signal input pin. Connect via 0.033 µF capacitor and voltage-splitting resistors as shown in Sec. 11. If it is not used, connect to NC.

[1]Power supply: A, AVDD; D, DVDD; P1, PVDD1; P2, PVDD2.
[2]Input/Output: O, output pin; I, intput pin; I/O, input/output pin; P, power supply pin; G, ground connection pin.

Output pin status as determined by OE, PDN, and RSTN pin status.

OE	PDN	RSTN	Output1[1]	Output2[1]
L	x	x	Hi-z output	L output
H	L	x	L output	L output
H	H	L	L output	L output
		H	Default Data Out[2]	Default Data Out[2]

[1] Output1: DATA [7:0], HD, VD_F, DVALID_F, DTCLK
Output2: NSIG
If OE=H and PDN=H just after power is turned on, output pin status will be indefinite until internal state is determined by reset sequence.
[2]In the absence of AIN signal input, output will be black data ((Y=0x10, Cb/Cr=0x80). (Blueback output can be obtained by register setting.)

AK8854VQ is hereafter the “AK8854”.

4. Electrical specifications

4.1 Absolute maximum ratings

Parameter	Min	Max	Units	Notes
Supply voltage DVDD, AVDD PVDD1 , PVDD2	 −0.3 −0.3	 2.2 4.2	 V V	–
Analog input pin voltage A (VinA)	−0.3	AVDD + 0.3 (≤2.2)	V	–
Digital input pin voltage D (VinD)	−0.3	DVDD + 0.3 (≤2.2)	V	XTI, XTO, CLKMD, TEST0, TEST1
Digital output pin voltage P1 (VoutP)	−0.3	PVDD1 + 0.3 (≤4.2)	V	DTCLK, DATA[7:0], HD, VD_F, DVALID_F, H_CSYNC, VSYNC
Digital input pin current P2 (VinP)	−0.3	PVDD2 + 0.3 (≤4.2)	V	OE, SELA, PDN, RSTN, SDA, SCL, NSIG
Input pin current (Iin) (except for power supply pin)	−10	10	mA	–
Storage temperature	−40	125	˚C	–

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage). All power supply grounds (AVSS, DVSS) should be at the same electric potential.
If digital output pins are connected to data bus, the data bus operating voltage should be in the same range as shown above for the digital output pin.

4.2 Recommended operating conditions

Parameter	Min	Typ	Max	Units	Condition
Analog supply voltage (AVDD) Digital supply voltage (DVDD)	1.70	1.80	2.00	V	AVDD=DVDD
I/O supply voltage (PVDD1) MPU I/F supply voltage (PVDD2)	1.70	1.80	3.60	V	PVDD1≥DVDD PVDD2≥DVDD
Operating temp. (Ta)	−40	–	85	˚C	–

The above supply voltages are referenced to ground pins (DVSS=AVSS) at 0 V (the Reference Voltage). All power supply grounds (AVSS, DVSS) should be at the same electric potential.

4.3 DC characteristics

Where no specific condition is indicated in the following table, the supply voltage range is the same as that shown for the recommended operating conditions in 4-2 above.

Parameter	Symbol	Min	Typ	Max	Units	Condition
Digital P2 input high voltage	VIH	0.8PVDD2	–	–	V	Case 1[a]
		0.7PVDD2	–	–	V	Case 2[b]
Digital P2 input low voltage	VIL	–	–	0.2PVDD2	V	Case 1[a]
		–	–	0.3PVDD2	V	Case 2[b]
Digital D input high voltage	VDIH	0.8DVDD	–	–	V	–
Digital D input low voltage	VDIL	–	–	0.2DVDD	V	–
Digital input high voltage	VIH	0.8PVDD1	–	–	V	Case 1[a]
		0.7PVDD1	–	–	V	Case 2[b]
Digital input low voltage	VIL	–	–	0.2PVDD1	V	Case 1[a]
		–	–	0.3PVDD1	V	Case 2[b]
Digital input leak current	IL	–	–	±10	uA	–
Digital P1 output high voltage	VOH	0.7PVDD1	–	–	V	IOH = −600uA
Digital P1 output low voltage	VOL	–	–	0.3PVDD1	V	IOL = 1mA
Digital P2 output high voltage	VOH	0.7PVDD2	–	–	V	IOH = −600uA
Digital P2 output low voltage	VOL	–	–	0.3PVDD2	V	IOL = 1mA
I^2C (SDA)L output	VOLC	–	–	0.4 0.2PVDD2	V	IOLC = 3mA PVDD2≥2.0V PVDD2<2.0V

[a]DVDD = 1.70V~2.00V, 1.70V≤PVDD1<2.70V, 1.70V≤PVDD2<2.70V, Ta: −40~85°C
[b]DVDD = 1.70V~2.00V, 2.70V≤PVDD1≤3.60V, 2.70V≤PVDD2≤3.60V, Ta: −40~85°C

Definition of above input/output terms

Digital P2 input: Collective term for SDA, SCL, SELA, OE, PDN, RSTN pin inputs.
Digital D input: Collective term for CLKMD, TEST0, TEST1 pin inputs.
Digital input: Collective term for H_CSYNC, VSYNC pin inputs.
Digital P1 output: Collective term for DTCLK, DATA[7:0], HD, VD_F, DVALID_F pin outputs.
Digital P2 output: Collective term for NSIG pin outputs.
SDA pin output: Not termed digital pin output unless otherwise specifically stated.

4.4 Analog characteristics (AVDD=1.8V, Temp.25˚C)

Selector clamp

Parameter	Symbol	Min	Typ	Max	Units	Condition
Maximum input range	VIMX	0	0.50	0.60	V_{PP}	Max value at minimum PGA_GAIN setting. Typical value at default PGA_GAIN setting.

PGA

Parameter	Symbol	Min	Typ	Max	Units
Resolution		–	7	–	bits
Minimum gain	GMN	–	−6	–	dB
Maximum gain	GMX	–	6	–	dB
Gain step	GST	–	0.094	0.235	dB

AD converter

Parameter	Symbol	Min	Typ	Max	Units	Condition
Resolution	RES		10		bits	–
Operating clock frequency	FS	–	27	–	MHz	–
Integral nonlinearity	INL	–	2.0	4.0	LSB	FS = 27 MHz, PGA_GAIN default setting
Differential nonlinearity	DNL	–	1.0	2.0	LSB	FS = 27 MHz, PGA_GAIN default setting
S/N	SN	–	53	–	dB	Fin = 1 MHz*, FS = 27 MHz, PGA_GAIN default setting
S/(N+D)	SND	–	51	–	dB	Fin=1MHz*, FS=27MHz PGA_GAIN default setting
Full scale Gain matching	IFGM			5		PGA_GAIN default setting
ADC internal common voltage	VCOM	–	0.9	–	V	–
ADC internal positive VREF	VRP	–	1.1	–	V	–
ADC internal negative VREF	VRN	–	0.7	–	V	–

*Fin = AIN input signal frequency

AAF (Anti-Aliasing Filter)

Parameter	Symbol	Min	Typ	Max	Units	Condition
Pass band ripple	Gp	−1		+1	dB	6 MHz
Stop band blocking	Gs	10	22	–	dB	27 MHz

4.5 Current consumption (at DVDD = AVDD = PVDD1 = PVDD2 = 1.8V, Ta = −40 ~ 85˚C)

Parameter	Symbol	Min	Typ	Max	Units	Condition
(Active mode)						
Total	IDD		108	145	mA	RGB/YPbPr: 3ch
Analog block	AIDD		82		mA	RGB/YPbPr: 3ch
			(63)		mA	YC: 2ch(*1)
			(34)		mA	CVBS: 1ch(*1)
Digital block	DIDD		22		mA	With crystal connected
I/O block	PIDD		4		mA	Load condition: CL=15pF(*2)
(Power down mode)						PDN=L(DVSS)
Total	SIDD		≤ 1	100	uA	
Analog block	ASIDD		≤ 1		uA	
Digital block	DSIDD		≤ 1		uA	
I/O block	PSIDD		≤ 1		uA	

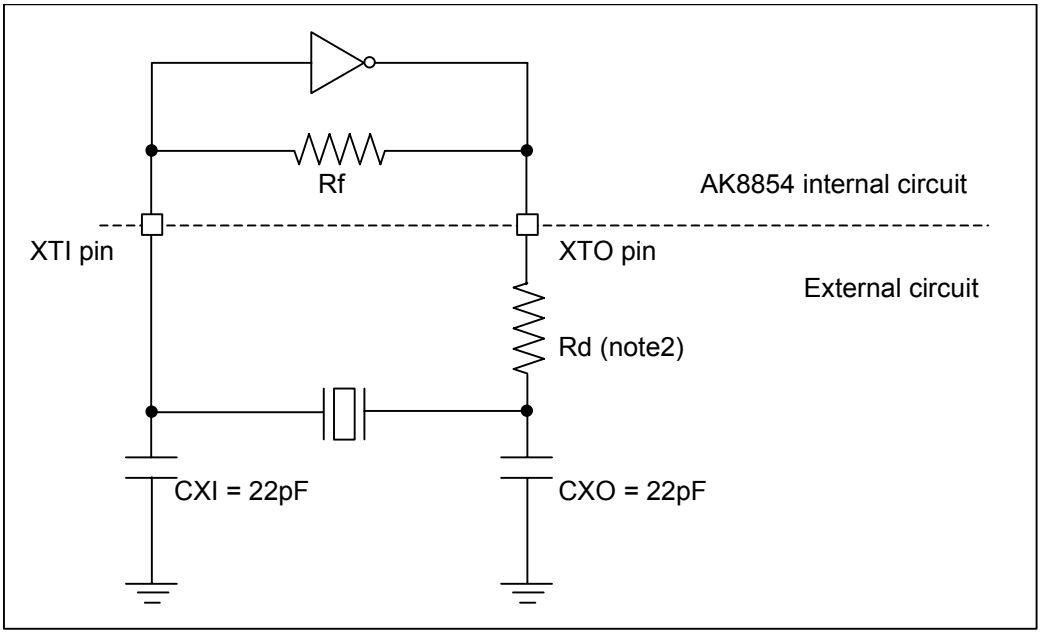
(*1) Reference Value
(*2) With NTSC-J 100% color bar input.

4.6 Crystal circuit block (Ta: −40~85˚C, CLKMD-pin is connected to DVSS.)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Frequency	f_0	–	24.576	–	MHz	–
Frequency tolerance	Δf/f	–		±100	ppm	–
Load capacitance	CL	–	15	–	pF	–
Effective equivalent resistance	Re	–	–	100	Ω	See note 1
Crystal parallel capacitance	CO	–	0.9	–	pF	–
XTI terminal external connection load capacitance	CXI	–	22	–	pF	If CL=15 pF
XTO terminal external connection load capacitance	CXO	–	22	–	pF	If CL=15 pF

(note1) Effective equivalent resistance generally may be taken as Re = R1 x $(1+CO/CL)^2$, where R1 is the crystal series equivalent resistance.

Example connection



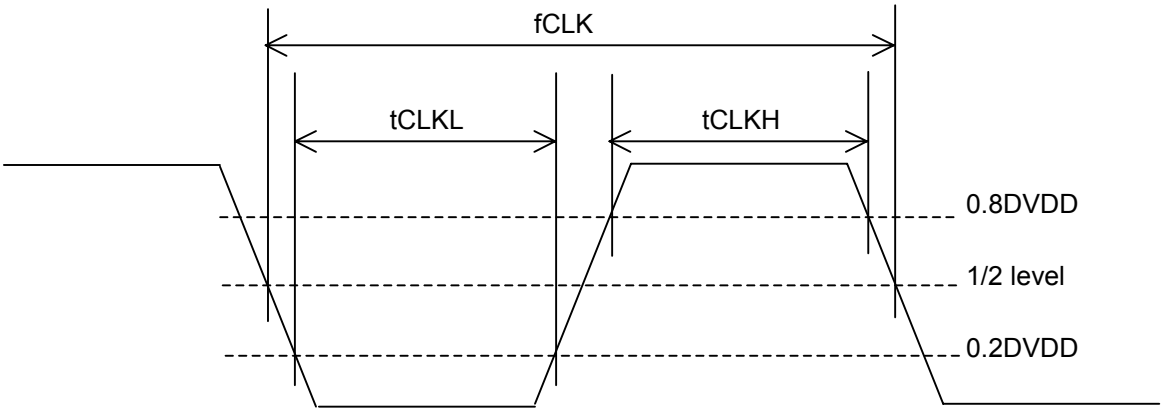
(note2) Determine need for and appropriate value of limiting resistance (Rd) in accordance with the crystal specifications.

5. AC timing (DVDD=1.70V~2.00V, PVDD1=PVDD2=1.70V~3.60V, −40 ~ 85°C)

Load condition: CL=15pF

5.1 Clock input (CLKMD-pin is connected to DVDD.)

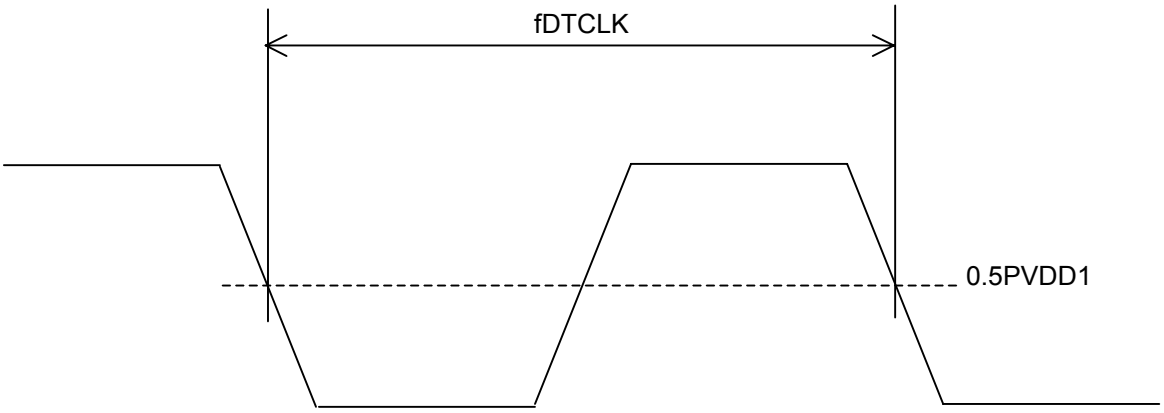
Set AK8854 clock input as follows.



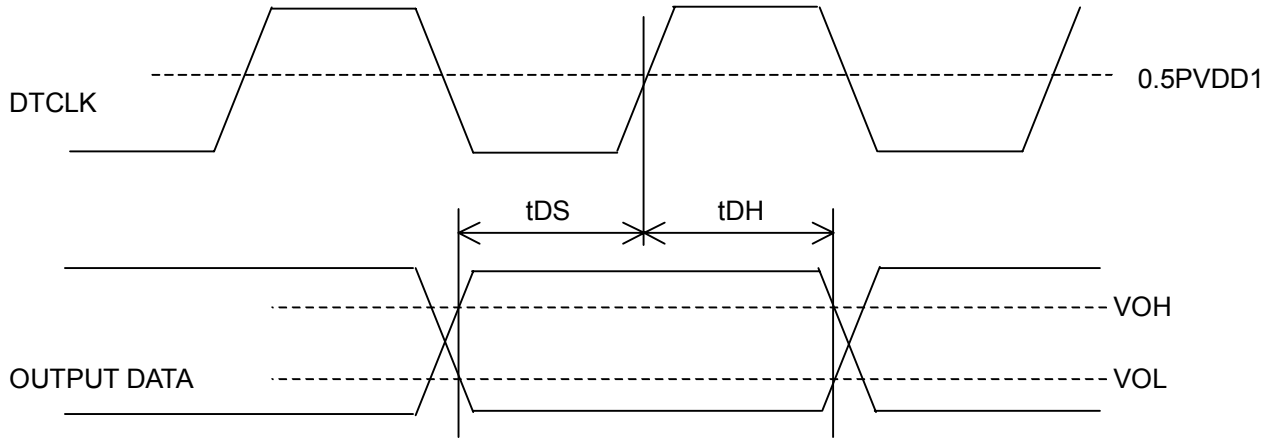
Parameter	Symbol	Min	Typ	Max	Units
Input CLK	fCLK	–	24.576	–	MHz
CLK pulse width H	tCLKH	16	–	–	ns
CLK pulse width L	tCLKL	16	–	–	ns
Frequency tolerance	–	–	–	±100	ppm

5.2 Clock output (DTCLK output)

Parameter	Symbol	Min	Typ	Max	Units
DTCLK	fDTCLK	–	27	–	MHz

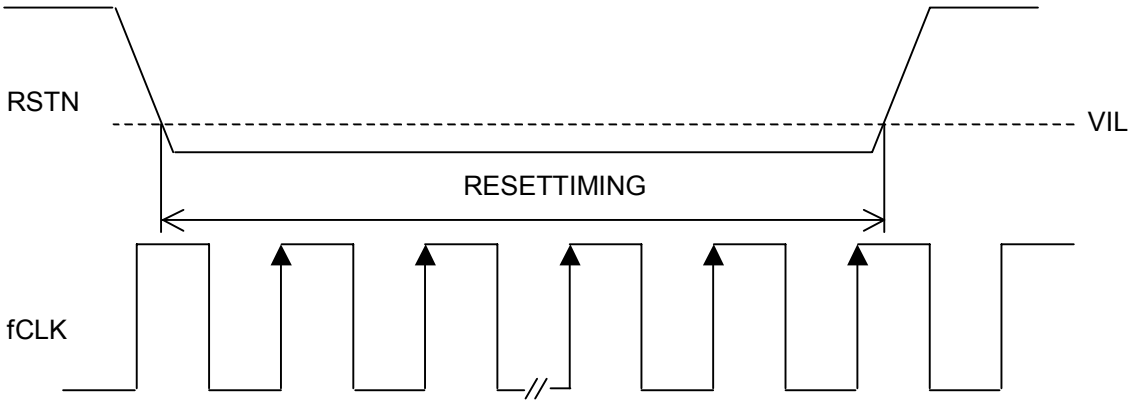


5.3 Output data (DATA[7:0], HD, VD_F, DVALID_F) timing



Parameter	Symbol	Min	Typ	Max	Units
Output Data Setup Time	tDS	10			nsec
Output Data Hold Time	tDH	10			nsec

5.4 Register reset timing

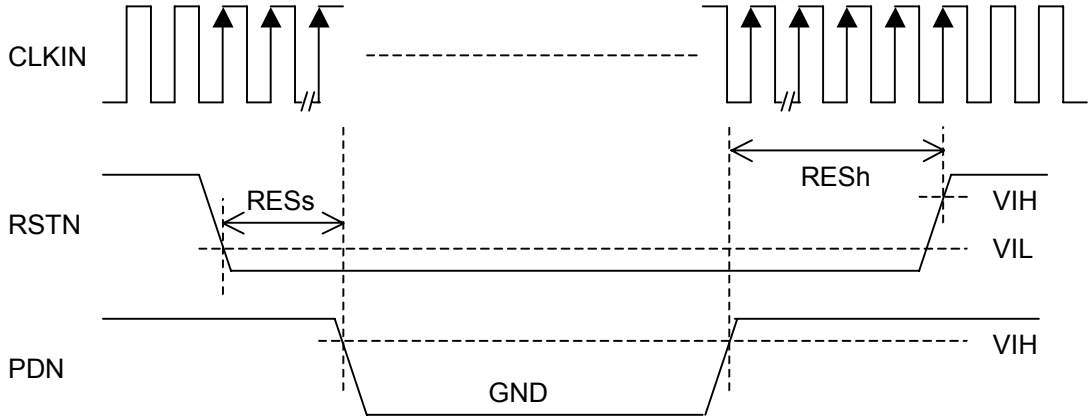


Parameter	Symbol	Min	Typ	Max	Units	Notes
RSTN pulse width	RESETTIMING	100 (4.1)	–	–	CLK (µsec)	Based on clock leading edge

Note. Clock input is necessary for reset operation.
RSTN pin must be pulled low following clock application.

5.5 Power-down sequence and Reset sequence after power-down

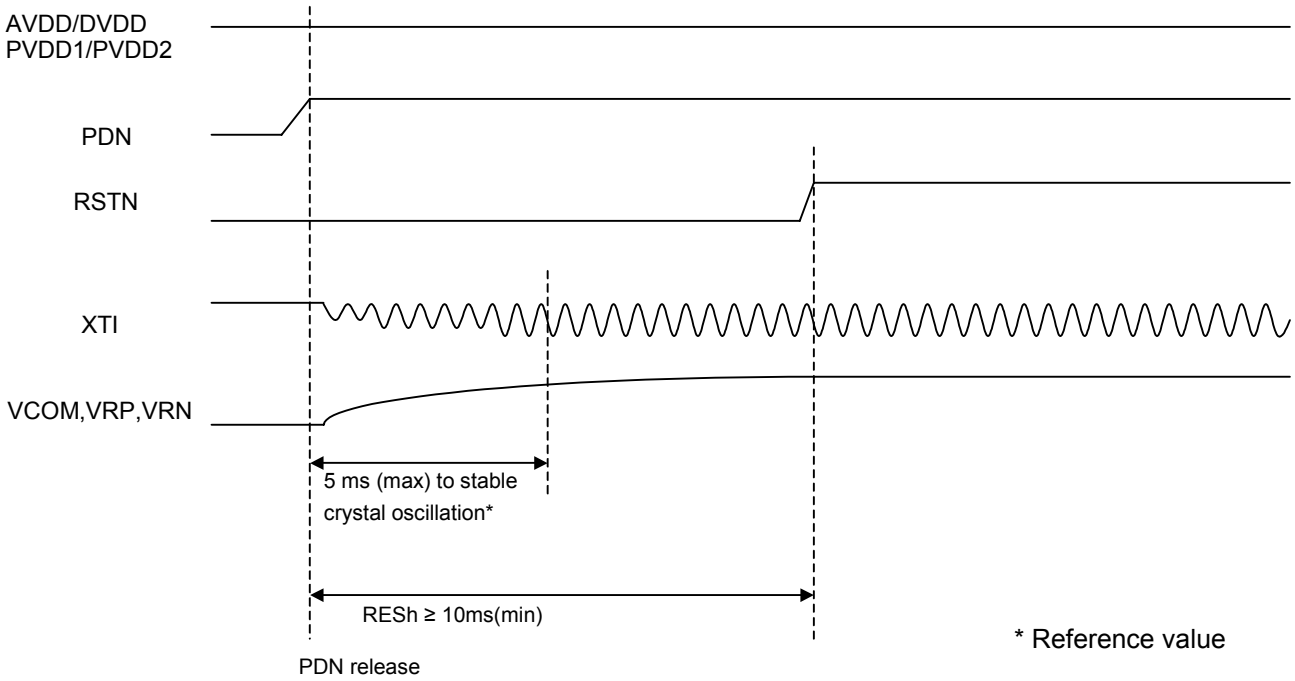
Reset must be applied for at least 2048 clock cycles (or 83.33 μs) before setting PDN (PDN=Low).
Reset must be applied for at least 10 ms after PDN release (PDN=Hi).



Parameter	Symbol	Min	Typ	Max	Units
Reset width before setting PDN	RESs	2048 (83.33)	–	–	CLK (μs)
Reset width after PDN release	RESh	10	–	–	ms

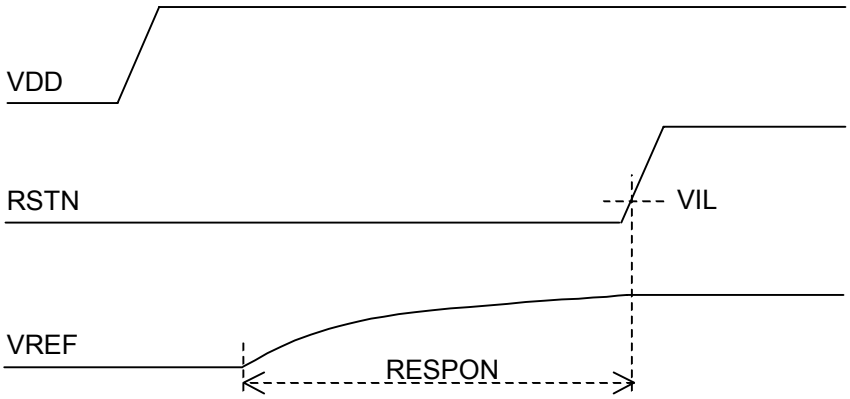
To perform power-down, all control signals must always be brought to the voltage polarity to be used or to ground level.
For any power supply removal, all power supplies must be removed.
Clock input is necessary for resetting.

The power-down sequence for connection of the crystal is as follows.



5.6 Power-on reset

At power-on, reset must be applied until the analog reference voltage and current have stabilized.[1] AVDD/DVDD/PVDD1/PVDD2 should be raised simultaneously at power-on.[2]

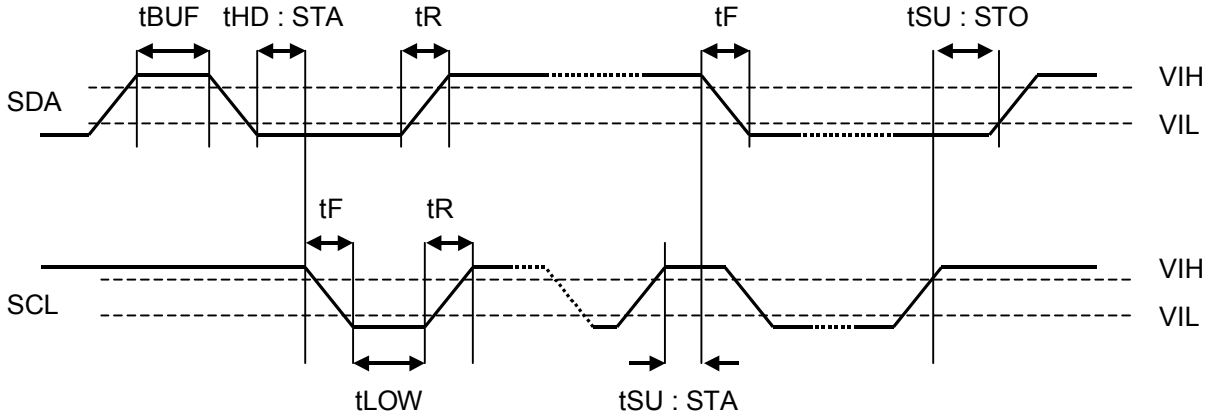


Parameter	Symbol	Min	Typ	Max	Units
RSTN pulse width	RESPON	10			ms

[1]Clock input is necessary for resetting.
[2]If not simultaneous, then raise in the order PVDD2 -> AVDD/DVDD -> PVDD1.

5.7 I²C bus input timing (DVDD=1.70V~2.00V , PVDD1=PVDD2=1.70V~3.60V , −40~85°C)

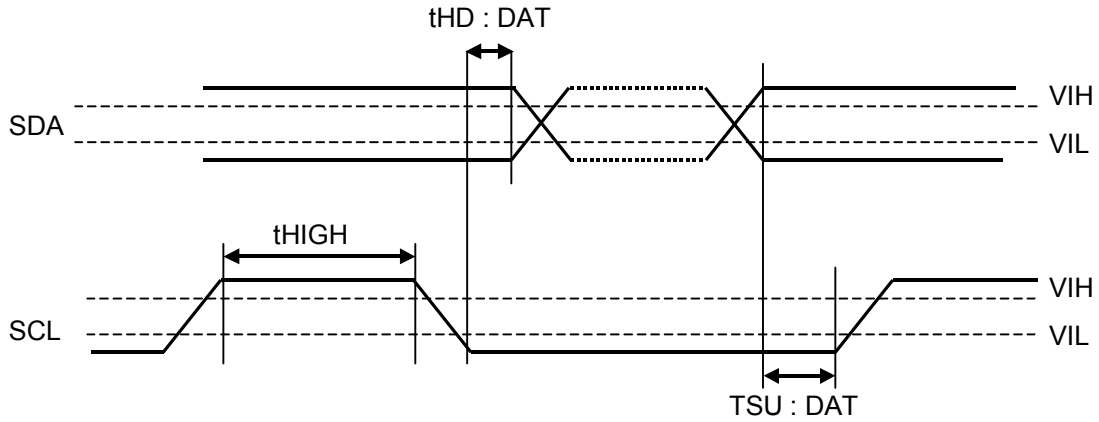
5.7.1 Timing 1



Parameter	Symbol	Min	Max	Units
Bus Free Time	tBUF	1.3		usec
Hold Time (Start Condition)	tHD:STA	0.6		usec
Clock Pulse Low Time	tLOW	1.3		usec
Input Signal Rise Time	tR		300	nsec
Input Signal Fall Time	tF		300	nsec
Setup Time(Start Condition)	tSU:STA	0.6		usec
Setup Time(Stop Condition)	tSU:STO	0.6		usec

Note. The timing relating to the I²C bus is as stipulated by the I²C bus specification, and not determined by the device itself. For details, see I²C bus specification.

5.7.2 Timing 2



Parameter	Symbol	Min	Typ	Units
Data Setup Time	tSU:DAT	100[1]		nsec
Data Hold Time	tHD:DAT	0.0	0.9[2]	usec
Clock Pulse High Time	tHIGH	0.6		usec

[1] If I²C is used in standard mode, tSU: DAT ≥ 250 ns is required.
[2] This condition must be met if the AK8854 is used with a bus that does not extend tLOW (to use tLOW at minimum specification).