Single Clock Generator
AK8112

Features

- **Output Frequency Range:**
  33.75MHz / 67.5MHz (Selectable)
- **Input Frequency:**
  27MHz
- **Low Jitter Performance:**
  15 ps (Typ.) Period, 1σ
- **Low Current Consumption:**
  3.5mA (Typ.)
- **Output Load:**
  15pF (max.)
- **Supply Voltage:**
  2.7 – 3.6V
- **Operating Temperature Range:**
  -10 to +80℃
- **Package:**
  6-pin SON (lead-free)
  Body Size 2.6mm x 1.6mm

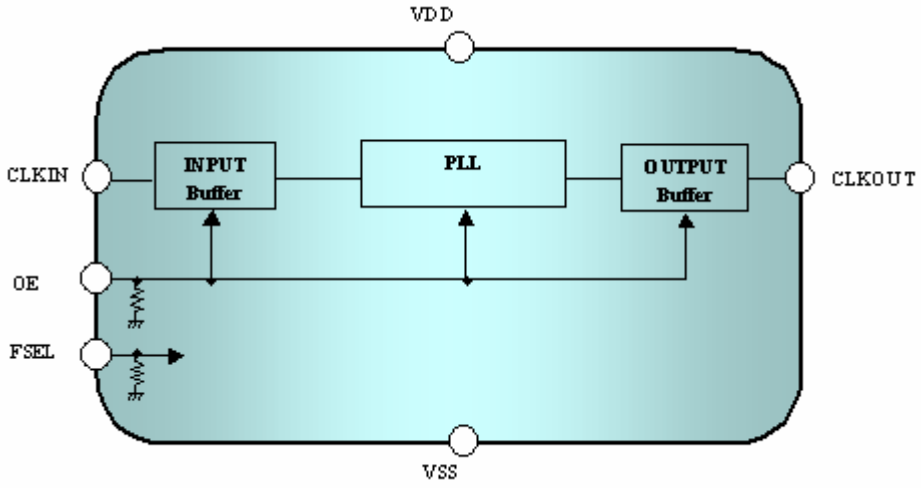
Description

The AK8112 is a single clock generator IC with an integrated PLL. It can generate either a 33.75MHz or a 67.5MHz clock from a 27MHz master clock input frequency. Through pin control, the output can be enabled or disabled, the frequency can be changed, and the device can be placed in a power-down mode. A high performance PLL locks to the master clock input, generating a low jitter, highly accurate clock output without an external crystal.

Applications

- Digital Still Camera

Block Diagram



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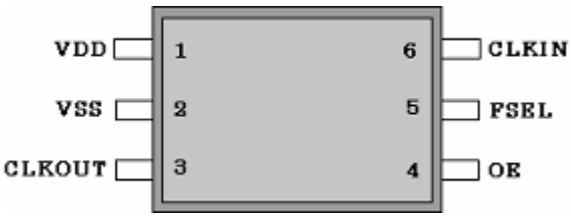
Pin Descriptions



Package: 6-Pin SON (Top View)
***lead-free**

Pin No.	Pin Name	Pin Type	Description
1	VDD	--	Power Supply
2	VSS	--	Ground
3	CLKOUT	OUT	Clock output Output clock frequency is selectable to 33.75MHz or 67.5MHz by setting the FSEL pin. In power down mode (OE = “L”), this pin is “L”.
4	OE	IN	CLKOUT output enable control “L”: CLKOUT=”L” and power down. “H”: active (1)
5	FSEL	IN	Clock frequency select “L”: 67.5MHz, “H”: 33.75MHz (1)
6	CLKIN	IN	Clock input (27MHz) Place the AK8112 in power down (OE = “L”) mode when an input clock is not supplied. Unstable input to the CLKIN causes the unstable CLKOUT signal. DC input to the CLKIN also causes the unstable CLKOUT signal.

(1) Internal pull down 100kΩ (Typ.)

Ordering Information

Part Number	Marking	Shipping Packaging	Package	Temperature Range
AK8112L	112(AK8112)	Tape and Reel	6-pin SON	-10 to 80 ℃

Absolute Maximum Rating

Over operating free-air temperature range unless otherwise noted (1)

Items	Symbol	Ratings	Unit
Supply Voltage	VDD	-0.3 to 4.6	V
Input Voltage	Vin	VSS-0.3 to VDD+0.3	V
Input Current (any pins except supplies)	I_{IN}	± 10	mA
Storage Temperature	Tstg	-55 to 130	°C

Note

(1) Stress beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rating conditions for extended periods may affect device reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

ESD Sensitive Device

This device is manufactured on a CMOS process, therefore, generically susceptible to damage by excessive static voltage. Failure to observe proper handling and installation procedures can cause damage. AKEMD recommends that this device is handled with appropriate precautions.

Recommended Operation Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Temperature	Ta		-10		80	°C
Supply Voltage	VDD		2.7	3.0	3.6	V
Input Clock Frequency	Fin			27		MHz
Input Clock Duty Cycle				50		%
Output Load Capacitance	Cp1	Pin: CLKOUT			15	pF

DC Characteristics

All specifications at VDD: over 2.7 to 3.6V, Ta: -10 to +80℃, Input Frequency: 27MHz, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
High Level Input Voltage	V_{IH}	Pin: CLKIN, FSEL, OE	0.8VDD			V
Low Level Input Voltage	V_{IL}	Pin: CLKIN, FSEL, OE			0.2VDD	V
Input Current 1	I_L 1	Pin: CLKIN	-10		+10	μA
Input Current 2	I_L 2	Pin: OE, FSEL	-10		+75	μA
High Level Output Voltage	V_{OH}	Pin: CLKOUT I_{OH}=-4mA (VDD=3.0V, Ta=25℃)	0.8VDD			V
Low Level Output Voltage	V_{OL}	Pin: CLKOUT I_{OL}=+4mA (VDD=3.0V, Ta=25℃)			0.2VDD	V
Current Consumption	I_{DD}	No load (VDD=3.0V, Ta=25℃)		3.5		mA
Power down current	I_{pd}	OE="L" FSEL="L" or open		0	10	μA

AC Characteristics

All specifications at VDD: over 2.7 to 3.6V, Ta: -10 to +80℃, Input Frequency: 27MHz, unless otherwise noted

Parameter	Symbol	Conditions	MIN	TYP	MAX	Unit
Output Clock Duty Cycle(2) (3)			45	50	55	%
Output Clock Rise Time(2) (3)	t_{rise}	0.2VDD to 0.8VDD			4.0	ns
Output Clock Fall Time(2) (3)	t_{fall}	0.2VDD to 0.8VDD			4.0	ns
Output Clock Jitter (2) (3)	Jit	Period, 1σ		15		ps
Output Lock Time(1)	t_{lock}	Power-up		1		ms

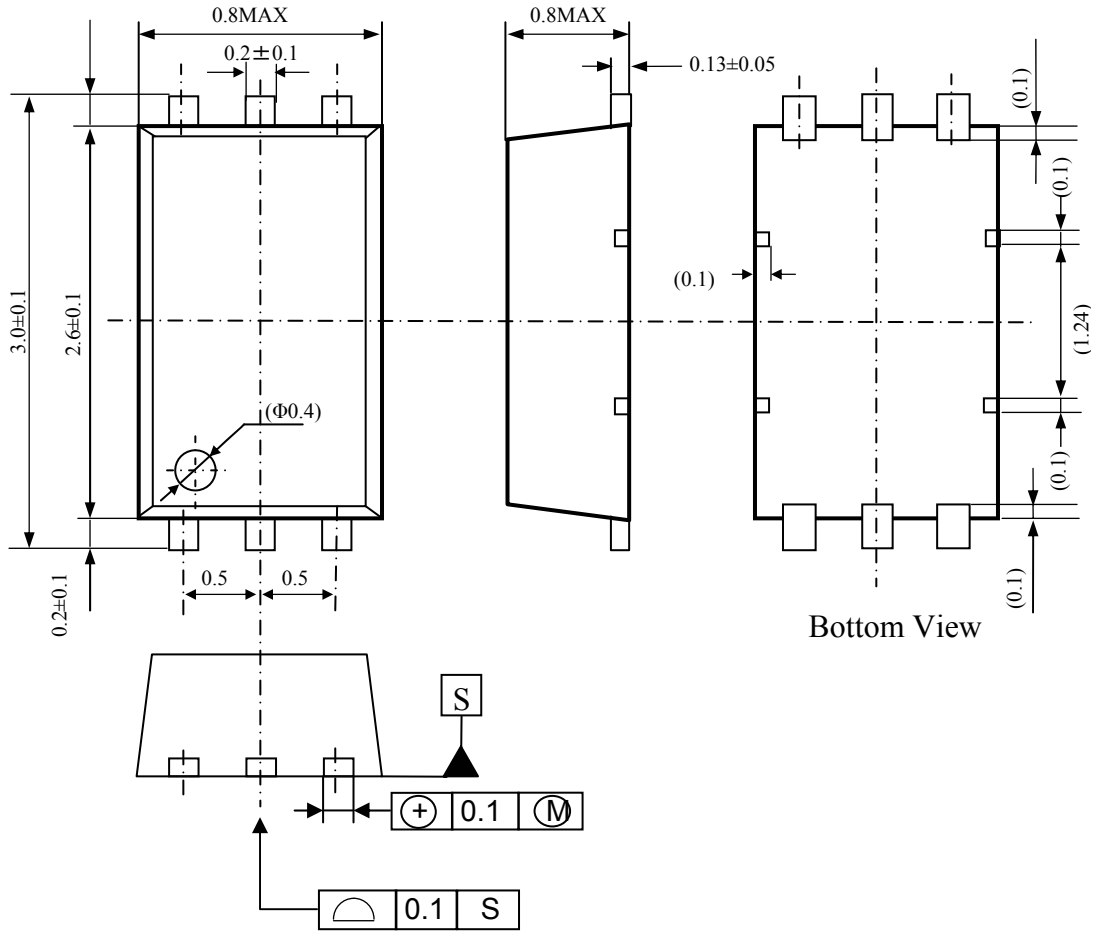
(1) The time that output reaches the target frequency within accuracy of ± 0.1% from the point that the power supply reaches VDD

(2) With the load capacitance specified by the recommended operation conditions

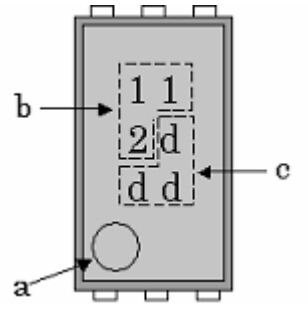
(3) Design value

Package Information

- **Mechanical data (Units:mm)**



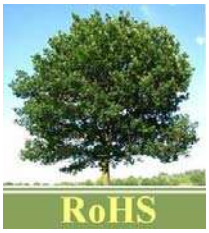
- **Marking**



a: #1 Pin Index
b: Part number
c: Date code (3 digits)

AKM and the logo - AKM - are the brand of AKEMD's IC's and identify that AKEMD continues to offer the best choice for high performance mixed-signal solution under this brand.

- **RoHS Compliance**



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(*) RoHS compliant products from AKEMD are identified with "Pb free" letter indication on product label posted on the anti-shield bag and boxes.

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