AsahiKASEI
ASAHI KASEI EMD

AK2300
3.3V Single channel PCM CODEC LSI

GENERAL DESCRIPTION

The AK2300 is a single channel PCM CODEC for various applications for example, AFE. It includes the selectable linear PCM interface, A/μ-law function, mute and power down. All of these functions are controlled by the pin.

It includes Band limiting filter, A/D and D/A converter, and A-law/μ-law converter. All functions are provided in very small QFN(16pins) package and it is good for reducing the mounting space.

PACKAGE

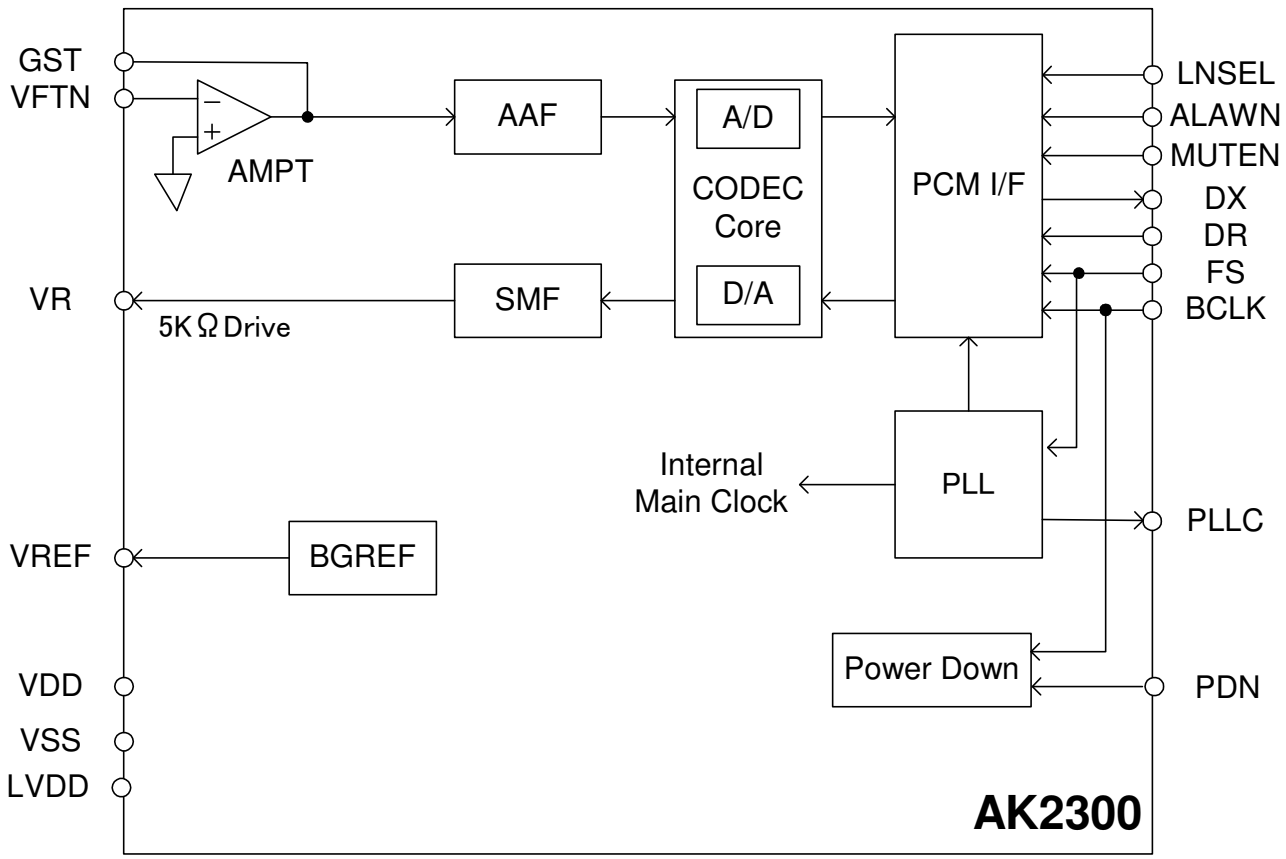
♦ 16pin QFN
Body 3.0*3.0mm
Pin pitch 0.5mm

FEATURE

♦ Single PCM CODEC and filtering system
♦ Selectable functions
- Mute
- Power down (PDN='L' or BCLK='L')
- A-law / μ-law / linear PCM

♦ Long Frame / Short Frame are selected by pin
♦ PCM data rate
(64k*N)Hz (N=1~32)
♦ Op-amp for the external gain adjustment
♦ Single power supply voltage: +2.6~+3.6V(VDD)
♦ Digital I/F power supply voltage: +1.7~3.6V(LVDD)
♦ Low power consumption
- Power on : 5.3mA(typ)
- Power down : 0.1uA(typ)

BLOCK DIAGRAM



CONTENT

PIN CONDITIONS

Pin#	Name	I/O	Pin type	AC load (MAX.)	DC load (MIN.)	Output status (mute)	Output status (PD)	Remarks
7	VFTN	I	Analog					
6	GST	O	Analog	50pF	AC load(*1) 10kΩ(*2)		Hi-Z	
4	VR	O	Analog	40pF	AC load(*1) 5kΩ	Analog ground	Hi-Z	
14	FS	I	CMOS					Pull down 100K±50Kohm
15	BCLK	I	CMOS					Pull down 100K±50Kohm
11	DX	O	CMOS	50pF		0 code	VSS	
16	DR	I	CMOS					Pull down 100K±50Kohm
1	MUTEN	I	CMOS					Do not open
2	PDN	I	CMOS					Do not open
13	DIF0	I	CMOS					Do not open
5	DIF1	I	CMOS					Do not open(*3)
3	VDD	-	PWR					
12	LVDD	-	PWR					
10	VSS	-	GND					
8	VREF	O	Analog				VSS	- External capacitance 0.1uF
9	PLLC	O	Analog				VSS	- External capacitance 0.056uF±30% (Includes temperature characteristic)

*1) AC load is feedback resistance to VFTN.
*2) This value includes a feedback resistance of input/output op-amps.
*3) Please connect it with VDD when DIF1 is “H”.

PIN FUNCTION

Pin types
DIN: Digital input DOUT: Digital output PWR: Power / Ground
AIN: Analog input AOUT: Analog output

Pin#	Name	Type	Function
7	VFTN	AIN	**Negative analog onput of analog input OP amp.** Signgle-end amplifire is composed the exernal registers. Transmit gain is defined by the ratio of the external registers.
6	GST	AOUT	**Output of the transmit OP amp.** The external feedback resister is connected between this pin and VFTN.
4	VR	AOUT	**Analog output of the D/A converter equivalent to the received PCM code.**
14	FS	DIN	**Frame sync input** This clock is input for the internal PLL which generates the internal system clocks. FS must be 8kHz clock which synchronized with BCLK.
5	BCLK	DIN	**Bit clock of PCM data interface** This clock defines the input/output timing of DX and RX. The frequency of BCLK should be 64kHz × N (N=1~32) and duty should be 40~60%. When this pin is taken low, power down the device. *Please don't stop BCLK at "H" level.
11	DX	DOUT	**Serial output of PCM data** The PCM data is synchronized with BCLK. This output remains in the low level except for the period in which PCM data is transmitted.
16	DR	DIN	**Serial input of PCM data** The PCM data is synchronized with BCLK.
1	MUTEN	DIN	**Mute setting pin** "L" level forces both A/D, D/A output to mute state.
2	PDN	DIN	**Power down setting pin** "L" level forces power down mode.
13	DIF0	DIN	**Audio data interface select pin** "L"=A-law,"H"=μ-law,"FS"=Linear PCM (Please connect DIF0 with FS(#14) at a Linear PCM mode.)
5	DIF1	DIN	**Audio data interface timing select pin** "H" : MSB of DX/DR are input/output by rising edge of FS.(Connect to VDD) "L" : MSB of DX/DR are input/output by next rising edge of BCLK after the rising edge of FS. (Please connect it with VDD when DIF1 is "H".)
3	VDD	PWR	**Positive supply voltage**
12	LVDD	PWR	**Positive supply voltage for digital interface**
10	VSS	PWR	**Ground (0V)**
8	VREF	AOUT	**Analog reference voltage output** External capacitance (0.1μF) should be connected between this pin and VSS. **Please do not connect external load to this pin.**
9	PLLC	AOUT	**PLL loop filter output** External capacitance (0.056μF±30%: Includes temperature characteristic) should be connected between this pin and VSS.
	Exposed Pad	-	**Flip side PAD** VSS or Open

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	min	max	Units
Power supply voltage				
Analog/Digital power supply	VDD	-0.3	4.6	V
Digital interface power supply	LVDD	-0.3	4.6	V
Digital input voltage	V_{TD}	-0.3	LVDD+0.3	V
Analog input voltage	V_{TA}	-0.3	VDD+0.3	V
Input current (except power supply pins)	I_{IN}	-10	10	uA
Storage temperature	Tstg	-55	125	℃

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	min	typ	max	Units
Power supply voltage					
Analog/Digital power supply	VDD	2.6	3.3	3.6	V
Digital interface power supply *1)	LVDD	1.7	3.3	3.6	V
Ambient operating temperature	Ta	-30		85	℃
Frame sync frequency *2)	FS	-1.0%	8	+1.0%	kHz

Note) All voltages reference to ground: VSS = 0V
*1)VDD≧LVDD
*2) All the characteristics of the CODEC are defined by 8kHz FS.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, guaranteed for VDD = +2.6V~3.6V, LVDD=+1.7V~+3.6V (VDD≧LVDD),
Ta = -30~+85℃, FS=8kHz, VSS=0V

DC Characteristics

Parameter	Symbol	Conditions	min	typ	Max	Unit
Power Consumption (All output unloaded)	P_{DD1}*1)	*1)BCLK=2.048		5.3	9.0	mA
	P_{DD2}	Power down		0.1	5.0	uA
Output high voltage	V_{OH}	I_{OH}＝-200uA	0.8VDD			V
Output low voltage	V_{OL}	I_{OL}＝200uA			0.4	V
Input high voltage1	VIH1	FS,BCLK,DR,MUTEN, PDN,DIF0	0.7LVDD			V
Input low voltage1	VIL1	FS,BCLK,DR,MUTEN, PDN,DIF0			0.3LVDD	V
Input high voltage2	VIH2	DIF1	0.7VDD			V
Input low voltage2	VIL2	DIF1			0.3VDD	V
Input leakage current	ILL	Except pull down pins	-10		+10	uA
Analog ground output	VRG	VREF pin	1.2	1.3	1.4	V

*1) VFTN=1020Hz@0dBm0 input, DR=1020Hz@0dBm0 Code input.

PCM INTERFACE **(Long Frame, Short Frame)**

All timing parameters of the output pins are measured at VOH = 0.8LVDD and VOL = 0.4V. Input pins are measured at VIH = 0.7LVDD and VIL = 0.3LVDD.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref Fig
FS Frequency	f_{PF}	-1.0%	8	+1.0%	kHz	Fig1,2, 3,4
BCLK Frequency	f_{PB}	-	$f_{PF} \times 8N$ (N=1~32)	-	kHz	
BCLK Duty Cycle	t_{WB}	40		60	%	
Rising/Falling Time: (BCLK,FS, DX,DR)	t_{RB} t_{FB}			40	ns	
Hold Time: BCLK Low to FS High	t_{HBF}	60			ns	
Setup Time: FS High to BCLK Low	t_{SFB}	20			ns	
Setup Time: DR to BCLK Low	t_{SDB}	20			ns	
Hold Time: BCLK Low to DR	t_{HBD}	60			ns	
FS Pulse Width Low	t_{WFSL}	1			BCLK	
Delay time: FS or BCLK High, whichever is later,to DX valid Note1)	T_{DZFL}			60	ns	
Hold time: BCLK Low to FS Low	T_{HBFS}	60			ns	
Setup time: FS Low to BCLK Low	T_{SFBS}	20			ns	
Delay Time: BCLK High to DX valid Note1)	t_{DBD}	0		60	ns	

Note1) Measured with 50pF load capacitance and 0.2mA drive.

Interface Timing

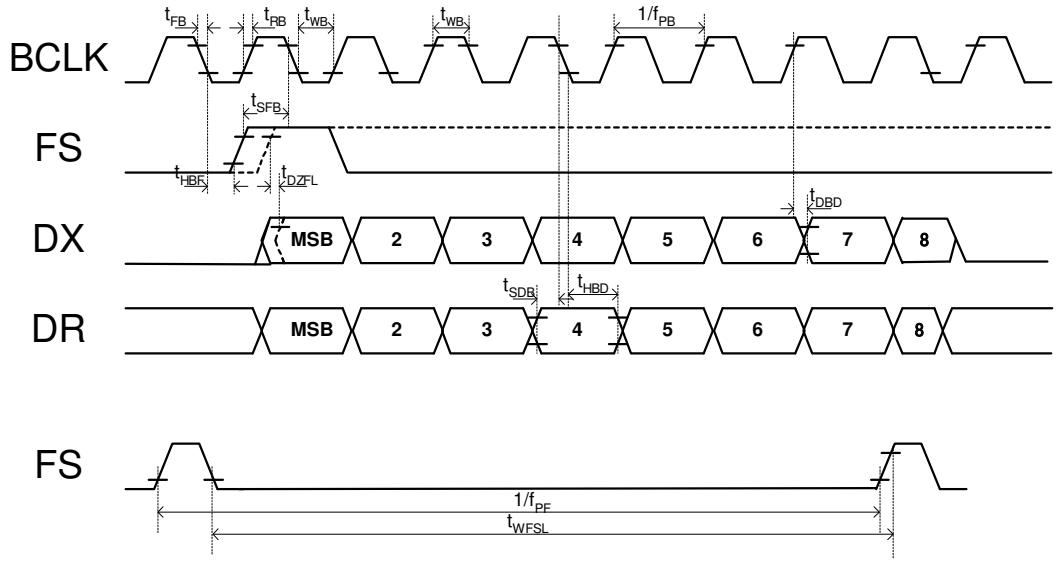


Fig1. DIF0=”L” or “H” , DIF1=”H”

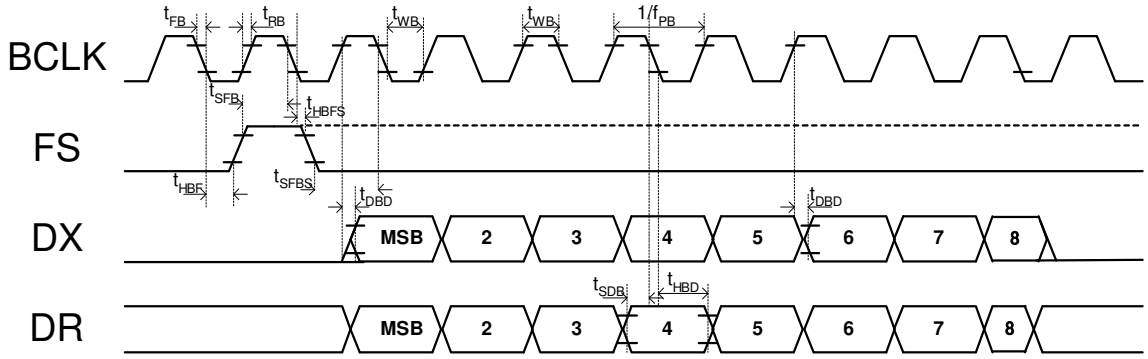


Fig2. DIF0=”L” or “H” , DIF1=”L”

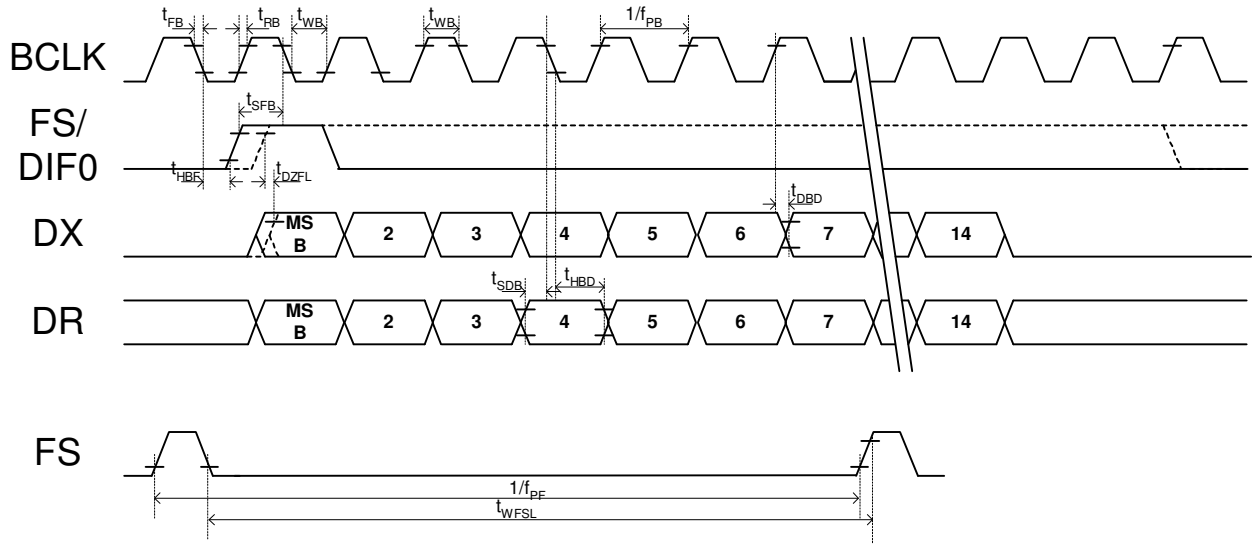


Fig3. DIF0=”FS”, DIF1=”H”

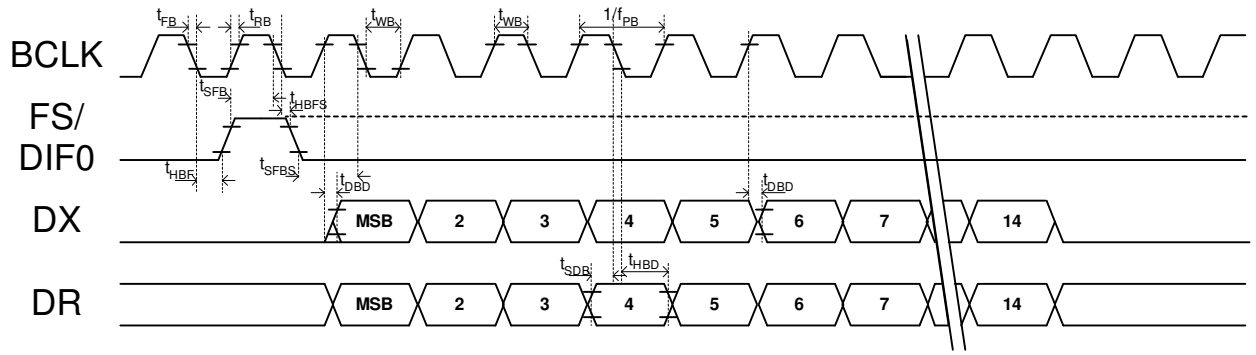


Fig4. DIF0=”FS”, DIF1=”L”

* The AMPT characteristics is measured at the 0dB gain.
The frequency specifications when FS deviation from 8kHz are as follows:

$$\frac{Used\text{FS}}{8\text{k[Hz]}} \times \text{noted frequency specification} = \text{Effective frequency specification}$$

Absolute Gain

Parameter		Conditions	min	typ	max	Unit
Analog input level	VFTN → DX	0dBm0@1020Hz input		0.460		Vrms
Absolute transmit gain			-0.6	—	0.6	dB
Maximum overload level		3.14dBm0		0.660		Vrms
Analog output level	DR → VR	0dBm0@1020Hz input		0.460		Vrms
Absolute receive gain			-0.6	—	0.6	dB
Maximum overload level		3.14dBm0		0.660		Vrms

Frequency response

Parameter	Conditions		min	Typ	max	Unit
Transmit frequency response (A→D)	Relative to:	-55dBm0～-50dBm0	-1.2	—	1.2	dB
	-10dBm0	-50dBm0～-40dBm0	-0.4	—	0.4	
VFTN → DX	1020Hz Tone	-40dBm0～ 3dBm0	-0.2	—	0.2	
Receive frequency response (D→A)	Relative to:	-55dBm0～-50dBm0	-1.2	—	1.2	dB
	-10dBm0	-50dBm0～-40dBm0	-0.4	—	0.4	
DR → VR	1020Hz Tone	-40dBm0～ 3dBm0	-0.2	—	0.2	

Frequency response

Parameter	Conditions		min	typ	max	Unit
Transmit Frequency response (A→D)	Relative to:	0.05kHz	—	—	-30	dB
	0dBm0@1020Hz	0.06kHz	—	—	-26	
		0.2kHz	-1.8	—	0	
VFTN → DX		0.3～3.0kHz	-0.15	—	0.15	
		3.4kHz	-0.8	—	0	
		4.0kHz	—	—	-14	
Receive Frequency response (D→A)	Relative to:	0～3.0kHz	-0.15	—	0.15	dB
	0dBm0@1020Hz	3.4kHz	-0.8	—	0	
DR → VR		4.0kHz	—	—	-14	

Distortion (A-law, μ-law)

Parameter	Conditions		min	typ	max	Unit
Transmit signal to Distortion (A→D)	1020Hz Tone	-40dBm0～-45dBm0	25	—	—	dB
		-30dBm0～-40dBm0	30	—	—	
VFTN → DX		0dBm0～-30dBm0	36	—	—	
Receive signal to Distortion (D→A)	1020Hz Tone	-40dBm0～-45dBm0	25	—	—	dB
		-30dBm0～-40dBm0	30	—	—	
DR → VR		0dBm0～-30dBm0	36	—	—	

Distortion (Liear PCM)

Parameter	Conditions		min	typ	max	Unit
Transmit signal to Distortion (A→D) VFTN → DX	1020Hz Tone	0dBm0 (C-massage)		78		dB
Receive signal to Distortion (D→A) DR → VR	1020Hz Tone	0dBm0 (C-massage)		81		dB

Noise

Parameter	Conditions	min	typ	max	Units
Idle channel noise A→D (*1) VFTN → DX	u-law, C-message	—	12	17	dBrnC0
	A-law, Psophometric		-78	-73	dBm0p
	Linear, C-message	—	12	17	dBrnC0
Idle channel noise D→A(*2) DR → VR	u-law, C-message	—	9	14	dBrnC0
	A-law, Psophometric	—	-81	-76	dBm0p
	Linear, C-message	—	9	14	dBrnC0
PSRR Transmit path	VDD=3.3V/±66mVop f=0～10kHz	—	55	—	dB
PSRR Receiver path	VDD=3.3V/±66mVop f=0～10kHz	—	55	—	dB

(*1) Analog input is set to the analog ground level
(*2) Digital input is set to the +0 CODE

Crosstalk

Parameter	Conditions	min	Typ	max	Units
Transmit to receive VFTN → VR	VFTN 0dBm0@1020Hz DR = 0-Code	—	—	-75	dB
Receive to transmit DR → DX	DR=0dBm0@1020Hz code level VFTN = 0 Vrms	—	—	-75	dB

Analog input op-amp characteristics :AMPT

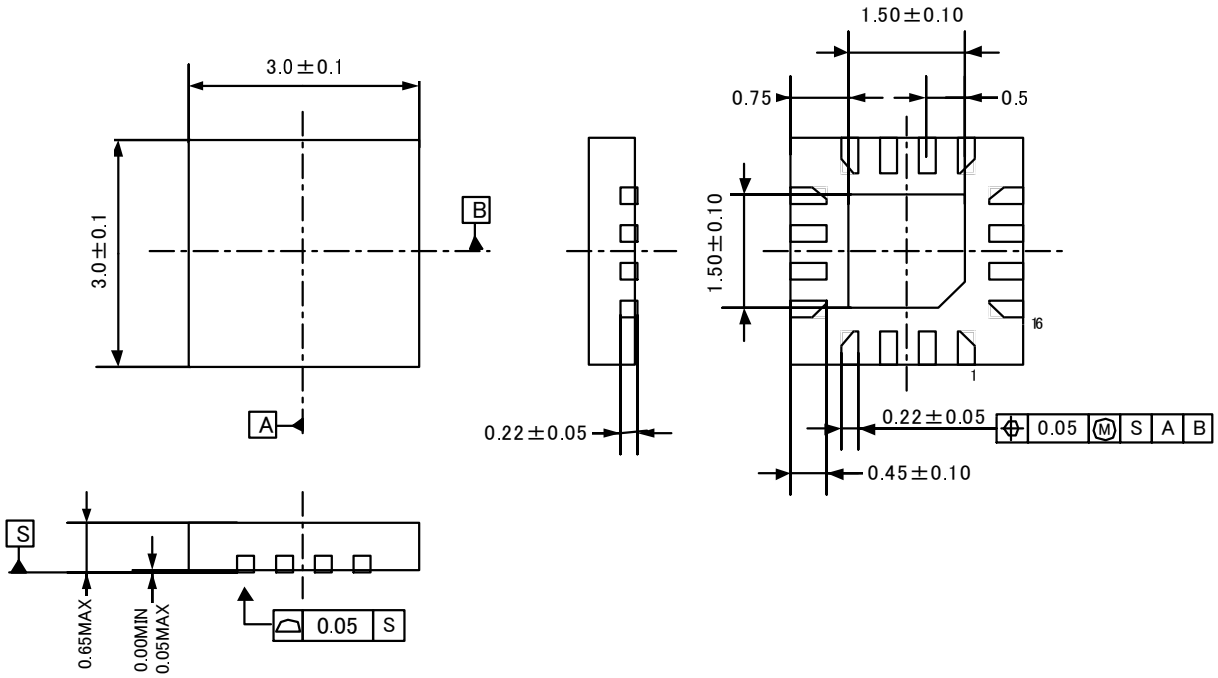
Parameter	Conditions	min	Typ	max	Units
Load resistance	AC load, Including feedback resistance	10	—	—	kΩ
Load capacitance		—	—	50	pF
Gain	Inverting amplifiers	-6	—	20	dB

Receive signal output characteristics :VR

Parameter	Conditions	min	typ	max	Units
Output voltage(AGND level)	PCM +0 code input	—	1.3	—	V
Load resistance	AC load	5	—	—	kΩ
Load capacitance		—	—	40	pF

PACKAGE INFORMATION

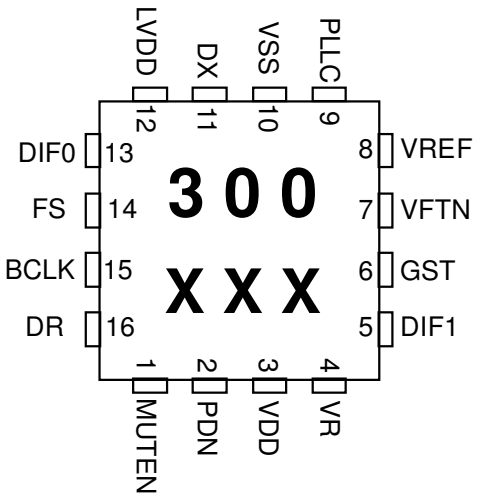
16pin QFN (3mm x 3mm)



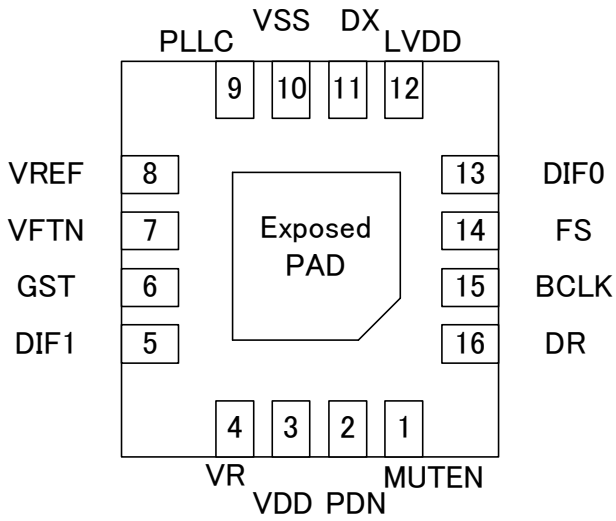
PIN ASSIGNMENT

16pin QFN

Top View

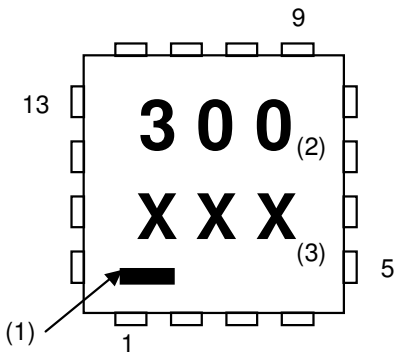


Bottom View



MARKING

(1) 1pin sign
(2) Marketing Code: 300
(3) Date Code: 3digit XXX



CIRCUIT DESCRIPTION

BLOCK	FUNCTION
AMPT	Op-amp for input gain adjustment. This op-amp is used as an inverting amplifier. Adjusting the gain with external resistors. The resistor should be larger than 10kohm for the feedback resistor. VFTN: Negative op-amp input. GST: Op-amp output.
AAF	Integrated anti-aliasing filter which prevents signals around the sampling rate from folding back into the voice band. AAF is a 2nd order RC active low-pass filter.
CODEC A/D	Converting the analog signal to 14bits linear data. And it is PCM data according to the companding schemes of ITU recommendation G.711; A-law or u-law. The band limiting filter is also integrated. The selection of companding schemes(A-law/ and interface timing are set by DIF0/1pins.
CODEC D/A	Converting the 14bits linear PCM data or 8bits PCM data accroding to A-law / u-law. The selection of expanding schemes and interface timing are set by DIF0/1pins.
SMF	Extracts the inband signal from D/A output. It also corrects the sinx/x effect of the D/A output.
BGREF	Provide the stable analog reference voltage using an on-chip band-gap reference circuit which is temperature compensated. The output voltage is 1.3V for 3.3V An external capacitor of 0.1uF should be connected between VREF and VSS to stabilize analog ground (VREF). **Please do not connect external load to this pin.**
PCM I/F	For the PCM data rate, 64kHz × N (N=1~32) are available. The 8bit PCM data is input/output by A/u-law data. The 14bit PCM data is input/output by the 2's compliment 16bit serial data format. PCM data is input to DR pin and output from DX pin. The selection of interface timing is selected by DIF0/1 pins. DIF0 / DIF1 "L" : A-law / "H" : MSB of DX/DR are input/output by rising edge of FS "H" : u-law / "L" : MSB of DX/DR are input/output by next rising edge of BCLK after the rising edge of FS. "FS" : Linear

PCM CODEC

- A/D
Analog input signal is converted to 14bit PCM data. The analog signal is fed to the anti-aliasing filter (AAF) before the converting PCM data, to prevent signals around the sampling rate from folding back into the voice band. The converted PCM data passes through the band limiting filter which Frequency response is designated in page8, and output from the DX pin with MSB first format. It is synchronized with rising edge of the BCLK. This PCM data is 8bit A/u-law or 14bit linear. And full scale is defined as 3.14dBm0. The analog input of 0.660Vrms is converted to a digital code of 3.14dBm0.

- D/A
Input PCM data from the DR pin is through the digital filter which Frequency response is designated in page8, and converted analog signal. This analog signal is removed the high frequency element with SMF (fc=30kHz typ) and output from the VR pin. The input PCM data is 8bit A/u-law data or 14bit linear. And full scale is defined as 3.14dBm0. When the input signal is 3.14dBm0, the level of the analog output signal becomes 0.660Vrms.

- 14bit linear PCM digital code
The relation ship between the analog signal and the 14bit linear code.

Signal level	14bit linear CODE (MSB First)
+Full code	01 1111 1111 1111
Peak value of the PCM 0dBm0 CODEC	01 0110 0100 1010
PCM 0-CODE	00 0000 0000 0000
-Full scale	10 0000 0000 0000

PCM Data Interface

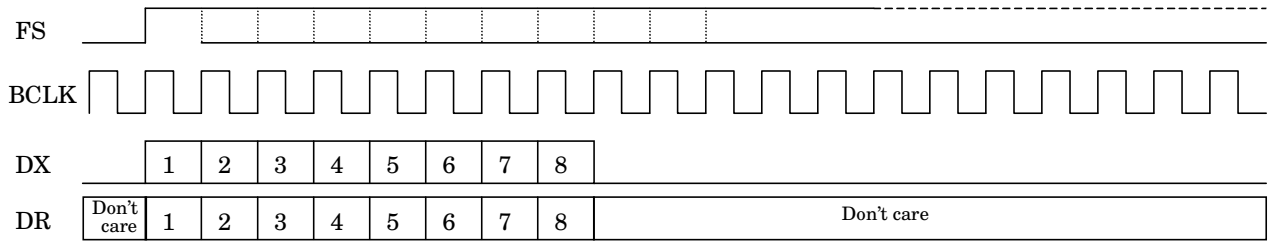
AK2300 supports the following PCM data formats
- DIF0="L" : A-Law
- DIF0="H": u-Law
- DIF0="FS": Linear PCM
- DIF1="H" : MSB of DX/DR are input/output by rising edge of FS
- DIF1="L" : MSB of DX/DR are input/output by next rising edge of BCLK after the rising edge of FS.

PCM data is interfaced through the pin (DX, DR).
In each case, PCM data is interfaced by A/u-law data with 8bit format and 2's compliment 2digit data with 16bit MSB first format. However, internal CODEC is 14bit format operation, then the lowest 2bits output become to "L" level. For the input, the lowest 2bits are ignored.

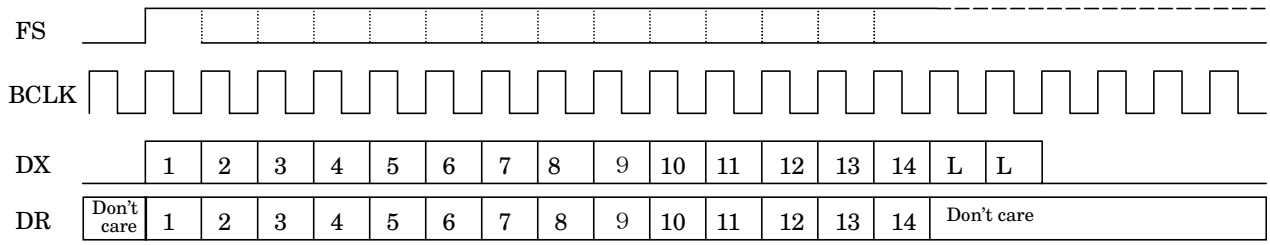
- Frame sync signal（FS）
8kHz reference signal. This signal indicated the timing and the frame position of 8kHz PCM interface. All the internal clock of the LSI is generated based on this FS signal.

-Bit clock（BCLK）
BCLK defines the PCM data rate. BCLK rate is 64kHz × N (N=1~32). This clock must be synchronized with FS.

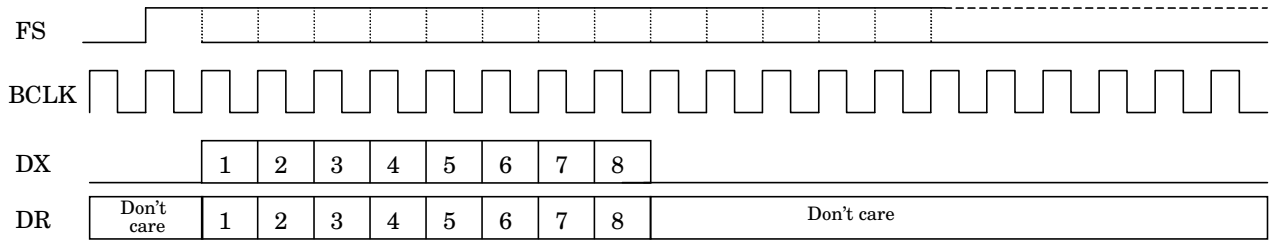
DIF0="L or H", DIF1="H"



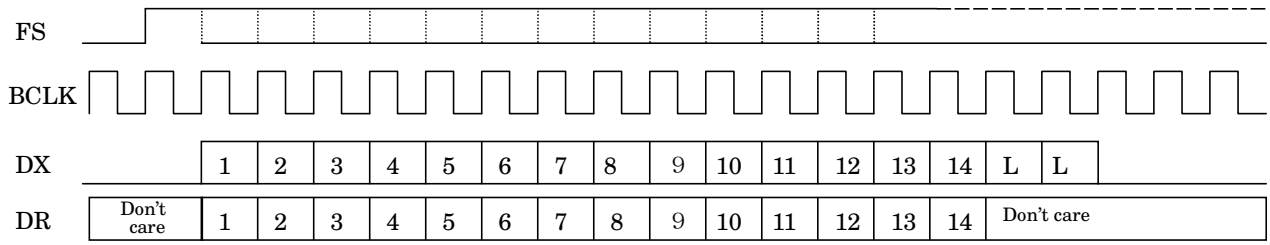
DIF0="FS", DIF1="H"



DIF0="L or H", DIF1="L"



DIF0="FS", DIF1="L"



MUTE

The output of the PCM CODEC can be muted by pin control.

MUTEN pin

MUTEN pin	Operation	DX pin	VR pin
L	Mute	0 Code	VREF level(1.3V)
H	Normal	PCM data output	CODEC analog output

[DX pin]
When the MUTEN pin turns to “L” during the data output, the mute function becomes available at the top of the next FS.

[VR pin]
When the MUTEN pin turns to “L”, 0 code is fed to the D/A converter and VR becomes at analog reference level (VREF level=1.3V).

POWER DOWN MODE

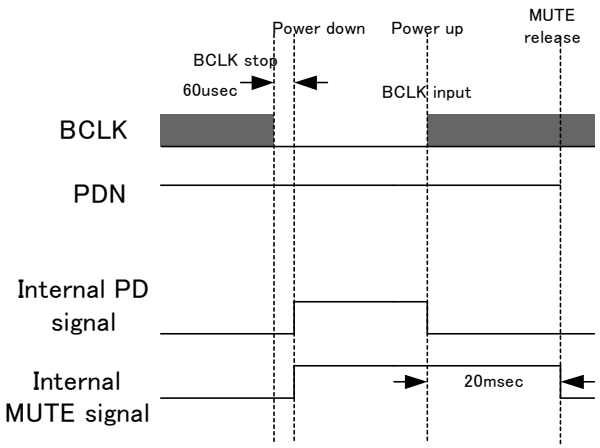
PDN pin “L” or to hold the BCLK pin “L”, the AK2300 is powered down.
(*Please don’t stop BCLK at “H” level.)

Power up/down sequence

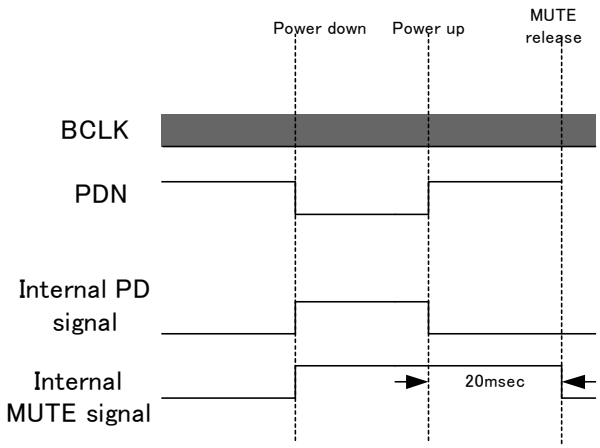
1) Power down
60usec(typ) passed after the PDN pin turns “L” or the BCLK pin hold “L”, internal PDN signal turn to L and the AK2300 is powered down.
When power down mode the output pins are as follows.

PIN Name	GST	VR	DX	VREF	PLLC
Output state	Hi-Z	Hi-Z	VSS	VSS	VSS

2) Power up
FS and BCLK pins are clocked and PDN pin =”H”, internal PDN signal is turn to “H” and power down mode is released.
During power down mode and 20msec (typ) after the power up, the voice path is muted for not to output abnormal noise.



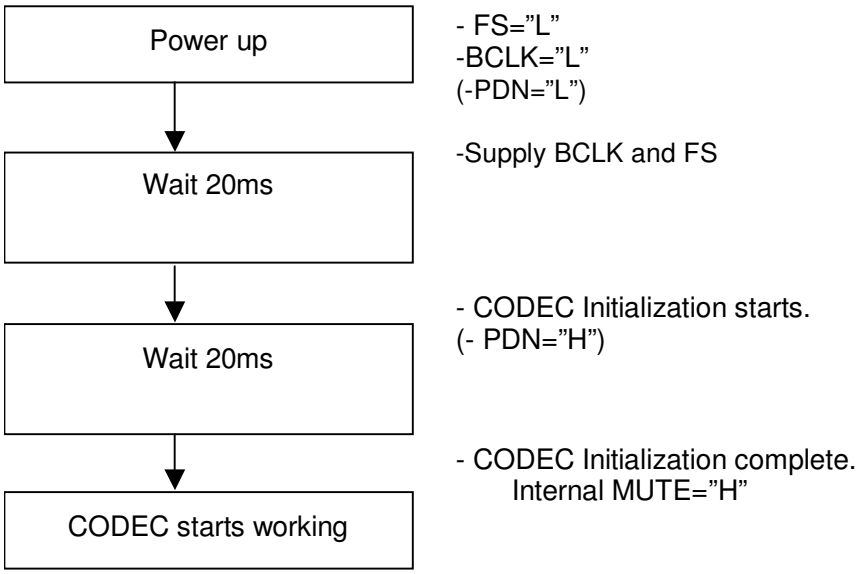
Power Down by BCLK=”L”



Power Down by PDN=”L”

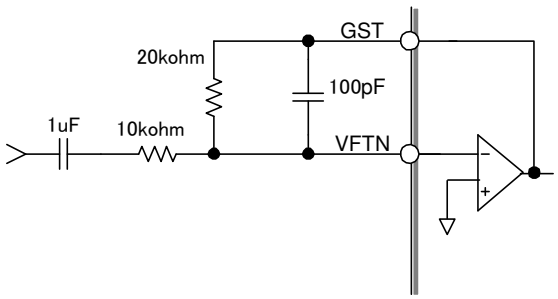
Recommended start up procedure

The following start up procedure is recommended when AK2300 is going to power up.
Power up is 5ms or less, internal Power On Reset is working, because ( ) in the following sequence can be omitted.

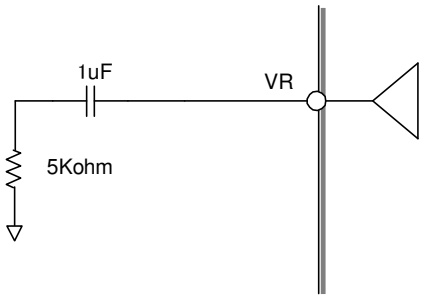


APPLICATION CIRCUIT EXAMPLES

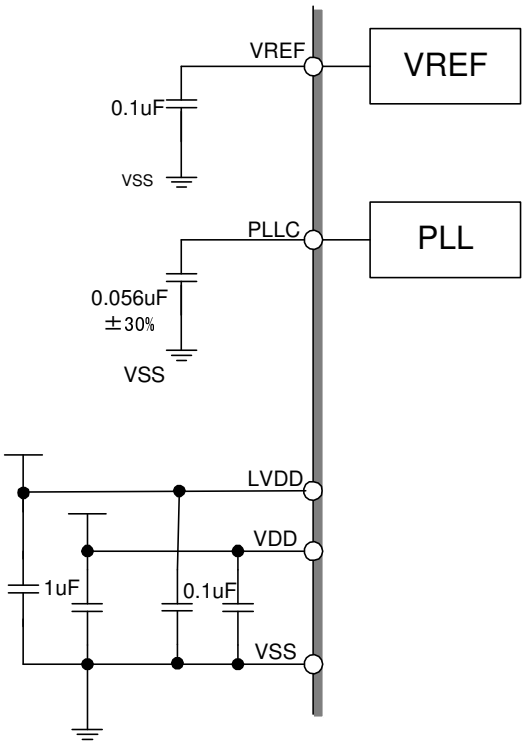
Analog input circuit (single)



Analog output circuit



Power supply, PLL loop filter capacitor and analog ground stabillization capacitor



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