AK2301A
3.3V Single channel PCM CODEC LSI

GENERAL DESCRIPTION

The AK2301A is a single channel PCM CODEC for speech processing 8kHz sampling PCM data by DSP. The AK2301A interfaces with 14bit linear data (16bit format).

It includes Band limiting filter, A/D and D/A converter, and universal op-amps for construction of the output filter. All functions are provided in small 24pin VSOP package and it is good for reducing the mounting space.

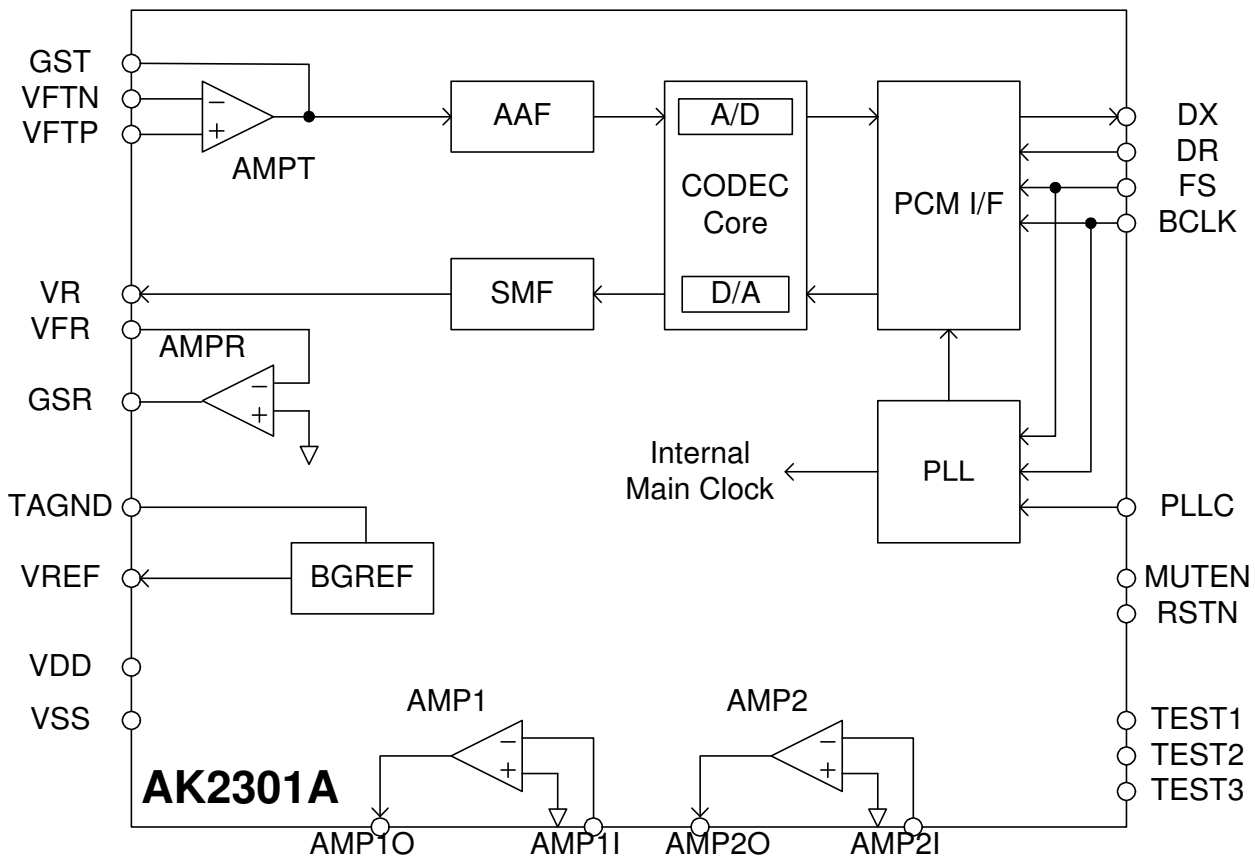
PACKAGE

- 24pin VSOP
  Pin to pin 7.9*7.6mm
  Pin pitch 0.65mm

FEATURE

- Single PCM CODEC and filtering system
- Mute function
- PCM interface; 14bits linear data (16bit format, serial interface)
- Long Frame / Short Frame are selected automatically
- PCM data rate 256kHz/512kHz
- Op-amp for the external gain adjustment
- Dual universal op-amps
- Single power supply voltage +3.0~+3.6V
- Low power consumption
- Small package

BLOCK DIAGRAM



CONTENT

PIN CONDITIONS

Pin#	Name	I/O	Pin type	AC load (MAX.)	DC load (MIN.)	Output status (mute)	Remarks
15	VFTN	I	Analog				
16	VFTP	I	Analog				
14	GST	O	Analog	50pF	AC load(*1) 10kΩ(*2)		
7	GSR	O	Analog	40pF	AC load(*1) 8kΩ		
8	VFR	I	Analog				
9	VR	O	Analog	40pF	AC load(*1) 8kΩ	Analog ground	
6	VDD	-					
19	VSS	-					
5	FS	I	CMOS				
3	BCLK	I	CMOS				
2	DX	O	CMOS	50pF		Hi-Z	
4	DR	I	CMOS				
23	MUTEN	I	CMOS				
22	RSTN	I	CMOS				
18	VREF	O	Analog				- External capacitance 1.0uF or more
20	PLLC	O	Analog				- External capacitance 0.33uF±40% (Includes temperature characteristic)
17	TAGND	O	Analog				- External capacitance 1.0uF or more - 150uA load max
11	AMP2I	I	Analog				
12	AMP1I	I	Analog				
13	AMP1O	O	Analog	40pF	AC load(*1) 8kΩ		
10	AMP2O	O	Analog	40pF	AC load(*1) 8kΩ		
21	Test1	I	CMOS				- Tie to the VSS
24	Tset2	I	CMOS				- Tie to the VSS
1	Test3	I	CMOS				- Tie to the VSS

*1)AC load is a load against AGND. This value includes a feedback resistance of input/output op-amps.

PIN FUNCTION

Pin types
NIN: Normal input TOUT: Try state output PWR: Power / Ground
AIN: Analog input AOUT: Analog output

Pin#	Name	Type	Function
15	VFTN	AIN	**Negative analog onput of transmit OP amp.** Diffelential or signal amplifire is composed with the VFTP and the exernal registers. Transmit gain is defined by the ratio of the external registers.
16	VFTP	AIN	**Positive analog input of the transmit OP amp.**
14	GST	AOUT	**Output of the transmit OP amp.** The external feedback resister is connected between this pin and VFTP.
7	GSR	AOUT	**Output of the receive OP amp.** Receive gain is defined by the ratio of the external registers. The differential output can be composed with using the VR.
8	VFR	AIN	**Negative analog input of the receive OP amp.**
9	VR	AOUT	**Analog output of the D/A converter equivalent to the received PCM code.**
6	VDD	PWR	**Positive supply voltage** +3.3V supply
19	VSS	PWR	**Ground (0V)**
5	FS	NIN	**Frame sync input** This clock is input for the internal PLL which generates the internal system clocks. FS must be 8kHz clock which synchronized with BCLK and do not stop feeding. *
3	BCLK	NIN	**Bit clock of PCM data interface** This clock defines the input/output timing of DX and RX. The frequency of BCLK should be 256kHz or 512kHz and do not stop feeding. *
2	DX	TOUT	**Serial output of PCM data** The PCM data is synchronized with BCLK. This output remains in the high impedance except for the period in which PCM data is transmitted.
4	DR	NIN	**Serial input of PCM data** The PCM data is synchronized with BCLK.
23	MUTEN	NIN	**Mute setting pin** "L" level forces both A/D, D/A output to mute state.
22	RSTN	NIN	**Reset signal input pin** Reset operation starts by low input. This pin is used for the initialization at the power up.Please use MUTEN pin together to avoid the popping sound output until the LSI finish the initialization after the power up. (Refer to P.13)
18	VREF	AOUT	**Analog ground output** External capacitance (1.0μF or more) should be connected between this pin and VSS. **Please do not connect external load to this pin.**
20	PLLC	AOUT	**PLL loop filter output** External capacitance (0.33μF±40%: Includes temperature characteristic) should be connected between this pin and VSS.
17	TAGND	AIN	**Analog ground output for transmit OP amp** 150μA load max. External capacitance (1.0μF or more) should be connected between this pin and VSS. This pin is used as an analog ground for transmit OP amp (AMPT).
12 11	AMP1I AMP2I	AIN	**Negative input of the universal OP amp**
13 10	AMP1O AMP2O	AOUT	**Output of the universal OP amp**
21 24 1	TEST1 TEST2 TEST3	NIN	**Test pins ("H"=test mode)** Please tie to VSS

*) When stop the BCLK and FS, please set RSTN="L".

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	min	max	Units
Power supply voltage Analog/Digital power supply	VDD	-0.3	4.6	V
Digital input voltage	V_{TD}	-0.3	VDD+0.3	V
Analog input voltage	V_{TA}	-0.3	VDD+0.3	V
Input current (except power supply pins)	I_{IN}	-10	10	mA
Storage temperature	Tstg	-55	125	℃

Warning: Exceeding absolute maximum ratings may cause permanent damage.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	min	typ	max	Units
Power supply voltage Analog/Digital power supply	VDD	3.0	3.3	3.6	V
Ambient operating temperature	Ta	-40		85	℃
Frame sync frequency *)	FS	-1.0%	8	+1.0%	kHz

Note) All voltages reference to ground: VSS = 0V
*) All the characteristics of the CODEC is defined by 8kHz FS.

ELECTRICAL CHARACTERISTICS

Unless otherwise noted, guaranteed for VDD = +3.3V±0.3V, Ta = -40~+85℃, FS=8kHz, VSS=0V

DC Characteristics

Parameter	Symbol	Conditions	min	typ	Max	Unit
Power Consumption BCLK=512kHz	P_{DD1}	All putput unloaded *1)		10	15	mA
Output high voltage	V_{OH}	I_{OH}=-1.6mA	0.8VDD			V
Output low voltage	V_{OL}	I_{OL}=1.6mA			0.4	V
Input high voltage	VIH		0.7VDD			V
Input low voltage	VIL				0.3VDD	V
Input leakage current	ILL		-10		+10	uA
Analog ground output	VRG		1.4	1.5	1.6	V
Output leakage current	ILT	Tri-state mode	-10		+10	uA

*1) VFTN/P=1020Hz@0dBm0 input, DR=1020Hz@0dBm0 Code input

PCM INTERFACE **(Long Frame, Short Frame)**

All timing parameters of the output pins are measured at VOH = 0.8VDD and VOL = 0.4V. Input pins are measured at VIH = 0.7VDD and VIL = 0.3VDD.

AC Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Ref Fig
FS Frequency	f_{PF}	-1.0%	8	+1.0%	kHz	Fig1,2
BCLK Frequency	f_{PB}	-	32FS/ 64FS	-	kHz	
BCLK Pulse width (High/Low) (BCLK=32xFS=256kHz)	t_{WBH} t_{WBL}	1.563	1.953	2.344	us	
BCLK Pulse width (High/Low) (BCLK=64xFS=512kHz)	t_{WBH} t_{WBL}	0.781	0.977	1.172	us	
Rising/Falling Time: (BCLK,FS, DX,DR)	t_{RB} t_{FB}			40	ns	
Hold Time: BCLK Low to FS High	t_{HBF}	60			ns	
Setup Time: FS High to BCLK Low	t_{SFB}	60			ns	
Setup Time: DR to BCLK Low	t_{SDB}	60			ns	
Hold Time: BCLK Low to DR	t_{HBD}	60			ns	
Delay Time: BCLK High to DX valid Note1)	t_{DBD}	0		60	ns	
Delay Time: BCLK High to DX High-Z Note1)	t_{DZC}	0		60	ns	
Long Frame						
Hold Time: 2nd period of BCLK Low to FS Low	t_{HBFL}	60			ns	Fig1
Delay Time: FS or BCLK High, whichever is later,to DX valid 注1)	t_{DZFL}			60	ns	
FS Pulse Width Low	t_{WFSL}	1			BCLK	
Short Frame						
Hold Time: BCLK Low to FS Low	t_{HBFS}	60			ns	Fig2
Setup Time: FS Low to BCLK Low	t_{SFBS}	60			ns	

Note1) Measured with 50pF load capacitance and 0.2mA drive.

Interface Timing

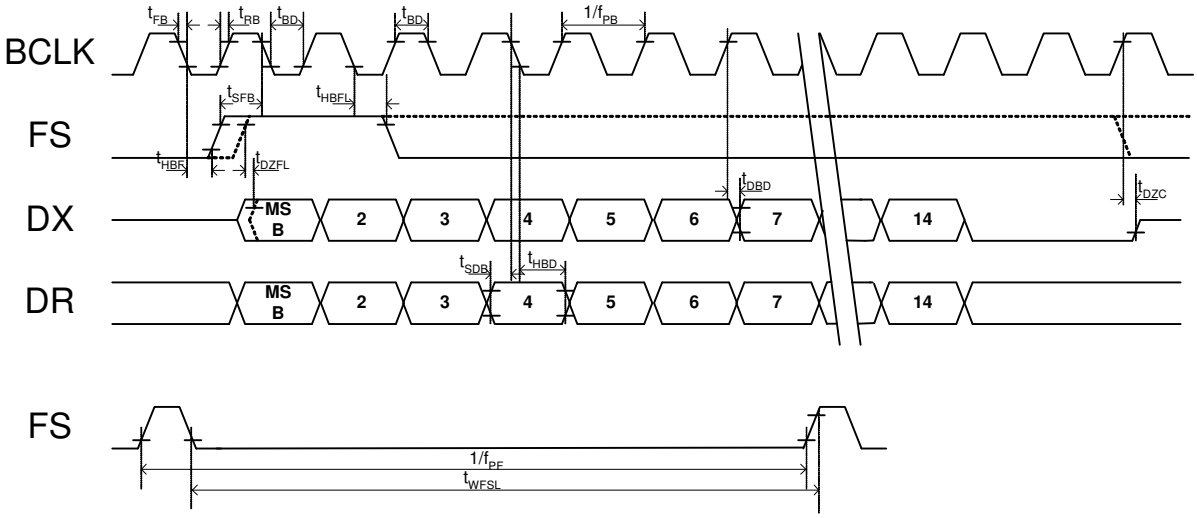


図1. Long Frame

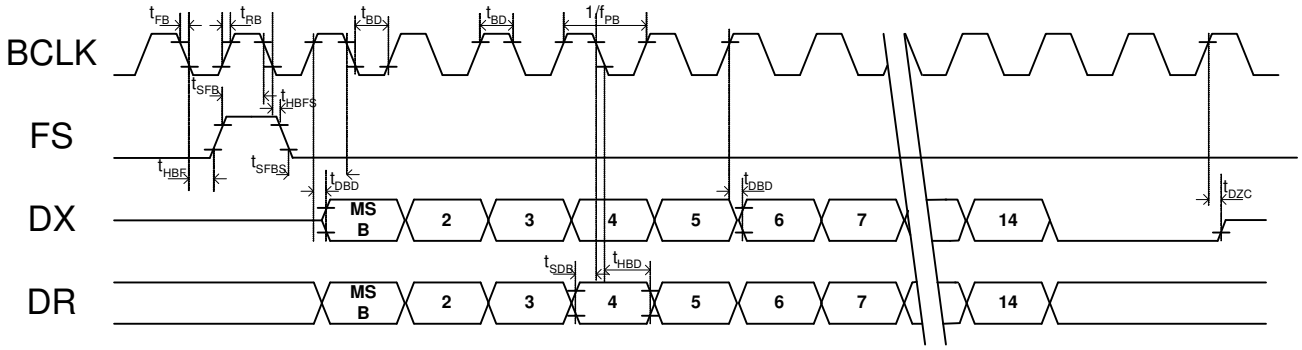


図2. Short Frame

CODEC

* The receive and transmit op-amp's characteristics are measured at the 0dB gain.
The frequency specifications when FS deviation from 8kHz are as follows:

$$\frac{Used\mathrm{FS}}{8\mathrm{k[Hz]}} \times \text{noted frequency specification} = \text{Effective frequency specification}$$

Absolute Gain

Parameter		Conditions	min	typ	max	Unit
Analog input level	VFTP,VFTN	0dBm0@1020Hz input		0.531		Vrms
Absolute transmit gain	→		-0.6	–	0.6	dB
Maximum overload level	DX	3.14dBm0		0.762		Vrms
Analog output level	DR	0dBm0@1020Hz input		0.531		Vrms
Absolute receive gain	→		-0.6	–	0.6	dB
Maximum overload level	VR	3.14dBm0		0.762		Vrms

Frequency response

Parameter	Conditions		min	typ	max	Unit
Transmit Frequency response (A→D)	Relative to:	0.05kHz	30	–	–	
	0dBm0@1020Hz	0.06kHz	26	–	–	
		0.2kHz	0	–	1.8	
VFTP,VFTN → DX		0.3～3.0kHz	-0.15	–	0.15	dB
		3.4kHz	0	–	0.8	
		4.0kHz	14	–	–	
Receive Frequency response (D→A)	Relative to:	0～3.0kHz	-0.15	–	0.15	
	0dBm0@1020Hz	3.4kHz	-0.8	–	0.8	dB
DR → VR		4.0kHz	14	–	–	

Distortion

Parameter	Conditions		min	typ	max	Unit
Transmit signal to Distortion (A→D)	1020Hz Tone	0dBm0	70	75	–	dB
VFTP,VFTN → DX	C-message					
Receive signal to Distortion (D→A)	1020Hz Tone	0dBm0	70	75	–	dB
DR → VR	C-message					

Noise

Parameter	Conditions	min	typ	max	Units
Idle channel noise A→D (*1) VFTP,VFTN → DX	C-message	—	8	13	dBrnC0
Idle channel noise D→A(*2) DR → VR	C-message	—	5	10	dBrnC0
PSRR Transmit path	VDD=3.3V/±66mVop f=0～10kHz	—	55	—	dB
PSRR Receiver path	VDD=3.3V/±66mVop f=0～10kHz	—	55	—	dB

(*1) Analog input is set to the analog ground level
(*2) Digital input is set to the +0 CODE

Crosstalk

Parameter	Conditions	min	typ	max	Units
Transmit to receive VFTP,VFTN → VR,GSR	VFTN 0dBm0@1020Hz DR = 0-Code	—	—	-75	dB
Receive to transmit DR → DX	DR=0dBm0@1020Hz code level VFTP,VFTN = 0 Vrms	—	—	-75	dB

Transmit op-amp characteristics: AMPT

Parameter	Conditions	min	typ	max	Units
Load resistance	AC load, Including feedback resistance	10	—	—	kΩ
Load capacitance		—	—	50	pF
Gain	Inverting amplifiers	-12	—	6	dB

Receive signal output characteristics: VR

Parameter	Conditions	min	typ	max	Units
Output voltage (AGND level)	PCM +0 code input	—	1.5	—	V
Load resistance	AC load	8	—	—	kΩ
Load capacitance		—	—	40	pF

Receive op-amp characteristics: AMPR

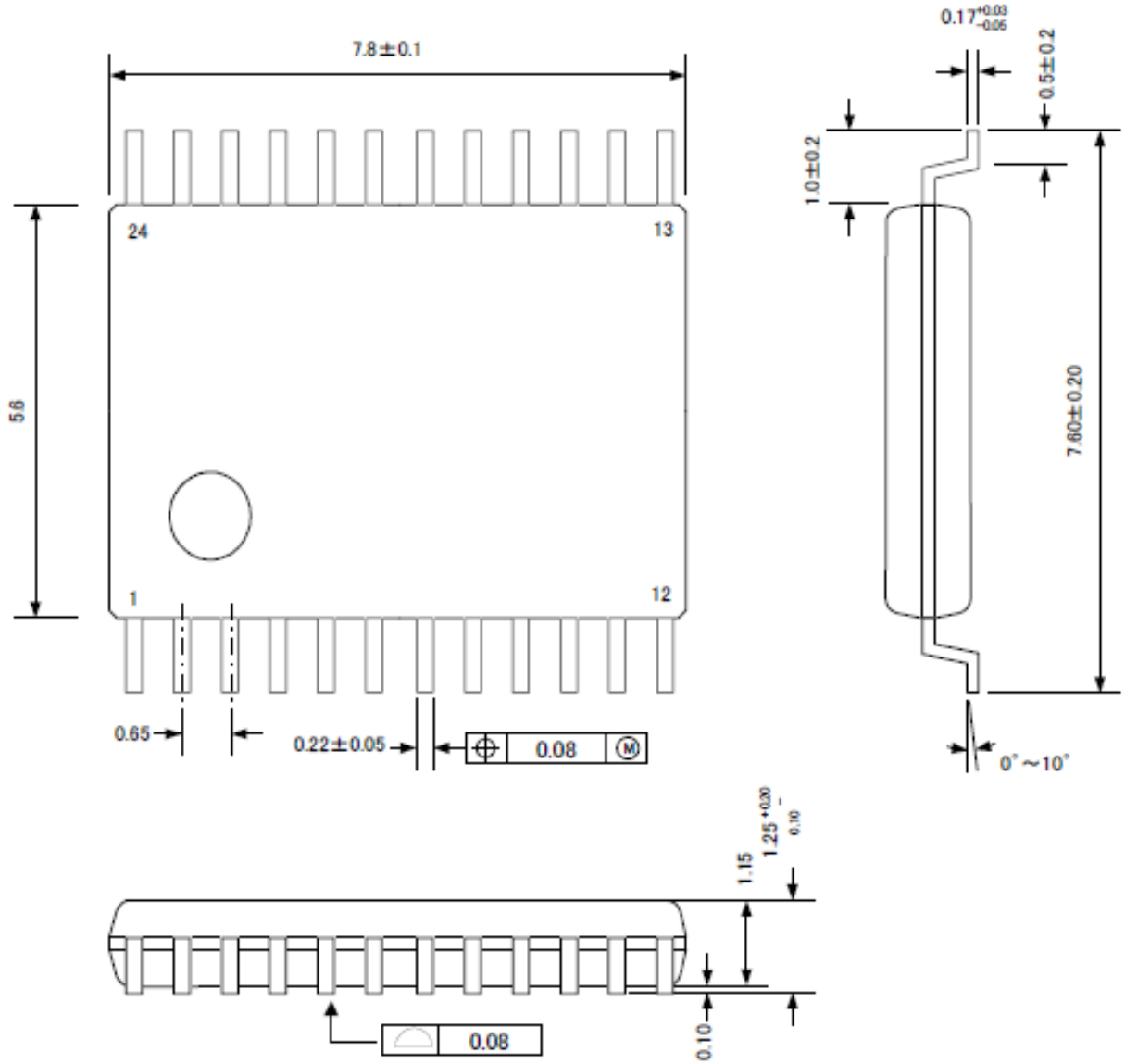
Parameter	Conditions	min	typ	max	Units
Load resistance	AC load, Including feedback resistance	8	—	—	kΩ
Load capacitance		—	—	40	pF
SINAD	0dB setting, 1020Hz@0dBm0 input VR, GSR differential output With C-message	70	75	—	dB
Gain	Inverting amplifire	-12	—	6	dB
Output voltage swing	DR = 3.14dBm0 digital code input	—	2.15	—	Vp-p

Universal op-amp characteristics: AMP1,2

Parameter	Conditions	min	typ	max	Units
Load resistance	AC load, Including feedback resistance	8	—	—	kΩ
Load capacitance		—	—	40	pF
SINAD	+6dB setting, 1020Hz@1.125Vp-p input 5Hz~30kHz measurement	62	87	—	dB
Gain	Inverting amplifier	-12	—	6	dB
Output voltage swing	+6dB setting, 1020Hz@1.125Vp-p input	2.1	2.25	—	Vp-p

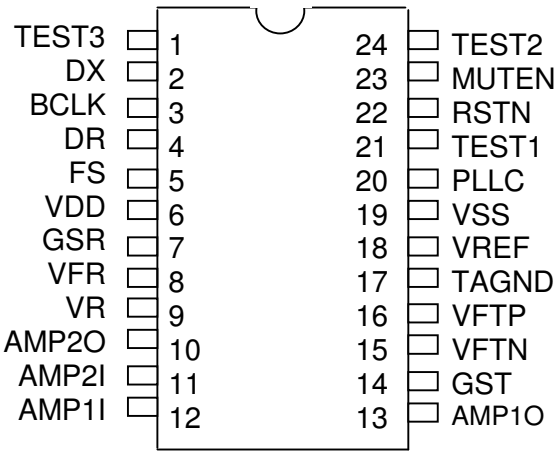
PACKAGE INFORMATION

24pin VSOP



PIN ASSIGNMENT

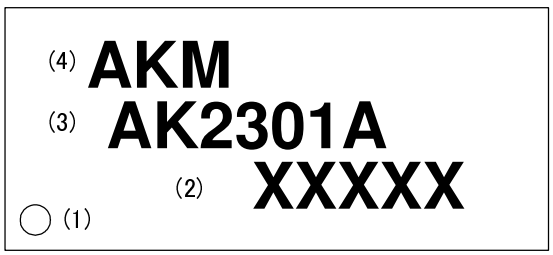
24pin VSOP



TEST1, TEST2, TEST3 are test pins.
Please tie them to the VSS.

MARKING

(1) 1pin sign
(2) Date Code: 5digit XXXXX
(3) Marketing Code: AK2301A
(4) AKM logo



CIRCUIT DESCRIPTION

BLOCK	FUNCTION
AMPT	Op-amp for input gain adjustment. This op-amp is used as an inverting or differential amplifier. Adjusting the gain with external resistors. The resistor should be larger than 10kΩ for the feedback resistor. VFTN: Negative op-amp input. VFTP: Positive op-amp input. GST: Op-amp output.
AMPR	Op-amp for output gain adjustment. This op-amp is used as an inverting amplifier. Adjusting the gain with external resistors. The combined resistor larger than 8kΩ is recommended for the feedback and the output load VFR: Negative op-amp input. GSR: Op-amp output. VR and GSR can be used as the differential output.
AAF	Integrated anti-aliasing filter which prevents signals around the sampling rate from folding back into the voice band. AAF is a 2nd order RC active low-pass filter.
CODEC A/D	Converts the analog signal to 14bit PCM data. The band limiting filter is also intergrated.
CODEC D/A	Converting the 14bit PCM data from the DR to the analog signal. Output of the D/A coverter is fed into the SMF to suppress the high frequency element.
SMF	Extracts the inband signal from D/A output. It also corrects the sinx/x effect of the D/A output.
BGREF	Provide the stable analog ground voltage using an on-chip band-gap reference circuit which is temperature compensated. The output voltage is 1.5V for 3.3V An external capacitor of 1.0uF or larger should be connected between VREF and VSS to stabilize analog ground (VREF). **Please do not connect external load to this pin.** TAGND pin is used as the analog ground level output for the AMPT. An external capacitor of 1.0uF or larger should be connected between TAGND and VSS to stabilize analog ground.
PCM I/F	For the PCM data rate, 256kHz or 512kHz are available. The 14bit PCM data is input/output by the 2's compliment 16bit serial data format. Two kinds of data format (Long Frame/Short Frame) are available. Each data format is automatically detected by AK2301A. PCM data is input to DR pin and output from DX pin.
AMP1, AMP2	Universal op-amp for the filter of the external voice path. The maximum load is 8kΩ (including the feedback resistor and AC load). These op-amps are assumed as using for the inverting LPF with 20kHz cut off frequency.

FUNCTIONAL DESCRIPTIONS

PCM CODEC

- A/D

Analog input signal is converted to 14bit PCM data. The analog signal is fed to the anti-aliasing filter (AAF) before the converting PCM data, to prevent signals around the sampling rate from folding back into the voice band. The converted PCM data passes through the band limiting filter which Frequency response is designated in page8, and output from the DX pin with MSB first format. It is synchronized with rising edge of the BCLK. This PCM data is 2's compliment 2digit data and full scale is defined as 3.14dBm0. The analog input of 0.762Vrms is converted to a digital code of 3.14dBm0.

- D/A

Input PCM data from the DR pin is through the digital filter which Frequency response is designated in page8, and converted analog signal. This analog signal is removed the high frequency element with SMF (fc=30kHz typ) and output from the VR pin. The input PCM data is 2's compliment 2digit data and full scale is defined as 3.14dBm0. When the input signal is 3.14dBm0, the level of the analog output signal becomes 0.762Vrms.

- PCM digital code

The relation ship between the analog signal and the 14bit linear code.

Signal level	14bit linear CODE (MSB First)
+Full code	01 1111 1111 1111
Peak value of the PCM 0dBm0 CODEC	01 0110 0100 1010
PCM 0-CODE	00 0000 0000 0000
-Full scale	10 0000 0000 0000

PCM Data Interface

AK2301A supports the following 2 PCM data formats
- Long Frame Sync (LF)
- Short Frame Sync (SF)
PCM data is interfaced through the pin (DX, DR).
In each case, PCM data is interfaced by the 2's compliment 2digit data with 16bit MSB first format. However, internal CODEC is 14bit format operation, then the lowest 2bits output become to "L" level. For the input, the lowest 2bits are ignored.

Selection of the interface format

The AK2301A automatically selects the Long Frame/Short frame by means of detecting the length frame signal.

LONG FRAME (LF) / SHORT FRAME (SF)

-Automatic LF/SF detection

AK2301A monitors the duration of the "H" level of FS and automatically selects LF or SF interface format.

Period of FS="H"	Frame type
More than 2 clocks of BCLK	LF
1 clock of BCLK	SF

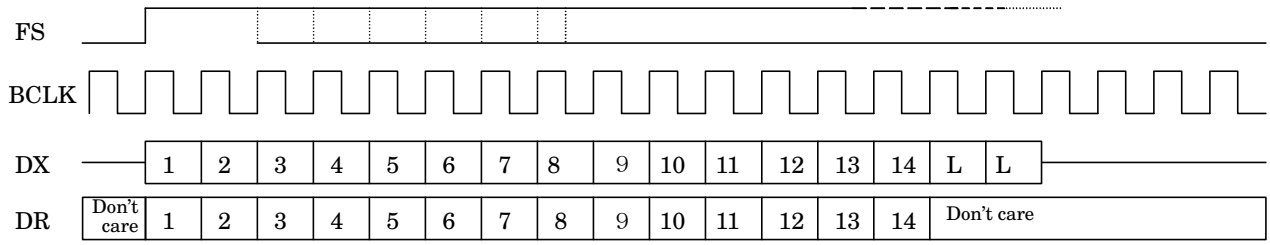
Timing of the interface

16bit PCM data is accommodated in 1 flame (125μs) defined by 8kHz frame sync signal. Although there are 4time slot at maximum in 8kHz frame (when BCLK = 512kHz), PCM data for AK2301A occupies first time slot.

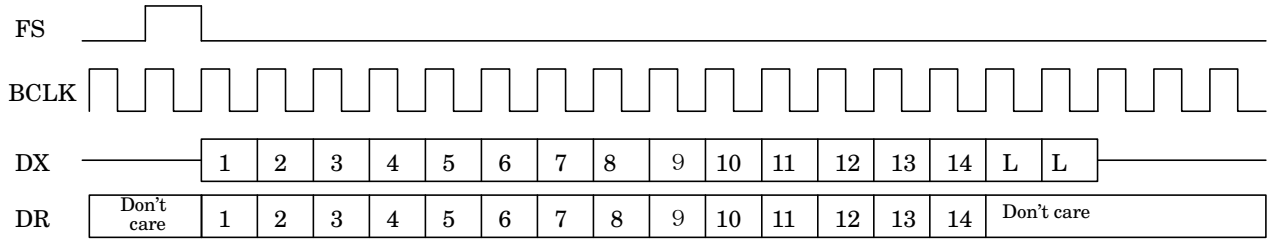
- Frame sync signal（FS）
8kHz reference signal. This signal indicated the timing and the frame position of 8kHz PCM interface.
All the internal clock of the LSI is generated based on this FS signal.

-Bit clock（BCLK）
BCLK defines the PCM data rate. BCLK rate is 256kHz or 512kHz. This clock must be synchronized with FS.

LongFrame



ShortFrame



Important notice!

Please don't stop feeding FS and BCLK.
Both FS and BCLK is used as the internal reference clock. LSI does not work when the FS and BCLK are not provided.
When stop the BCLK and FS, please set RSTN="L".

MUTE

The output of the PCM CODEC can be muted by pin control.

MUTEN pin

MUTEN pin	Operation	DX pin	VR pin
0	Mute	High-Impedance	CODEC analog ground
1	Normal	PCM data output	CODEC analog output

[DX pin]
When the MUTEN pin turns to “L” during the data output, the mute function becomes available at the top of the next FS.

[VR pin]
When the MUTEN pin turns to “L”, 0 code is fed to the D/A converter and VR becomes at analog ground level.

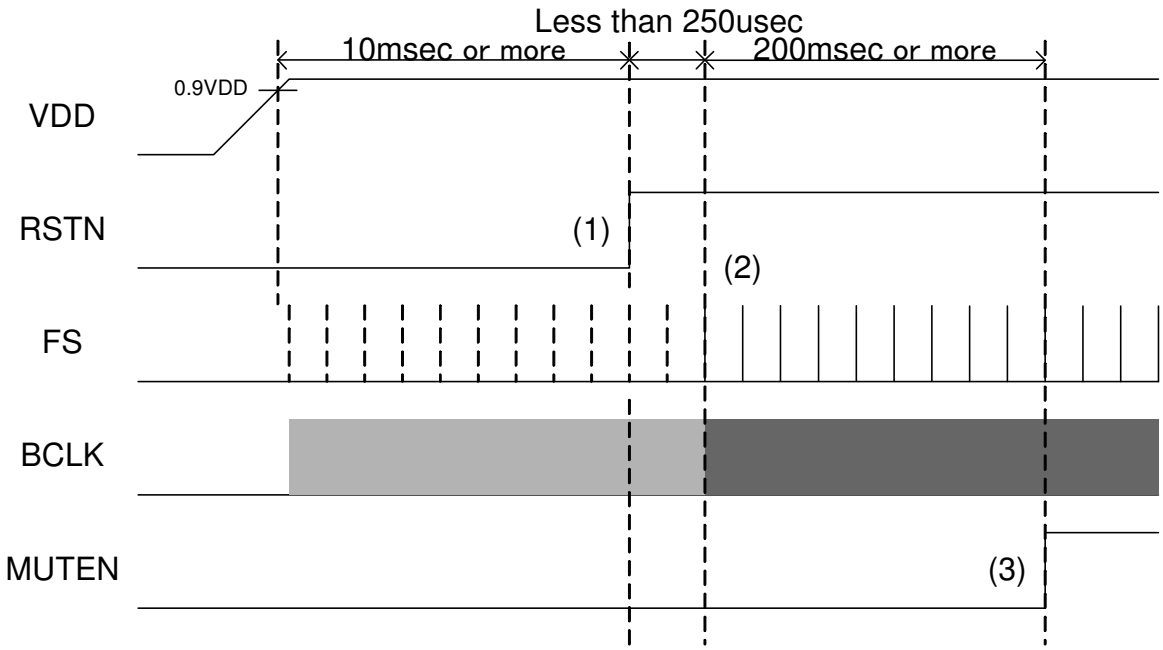
Reset and Start up sequence

Reset operation starts by low input.

This function is used for the initialization at the power up. Please use MUTEN together with RSTN to avoid the popping sound from the output until the AK2301A moves into the stable operation.

- Start up sequence

(1) After the power on, please set the RSTN pin to low level for 10msec or more.
(2) Before the first sequence or less than 250μs after the cancellation of reset, please provide the FS and the BCLK.
(3) Please set the MUTEN pin to low level during the period of the AK2301A's initialization which is less than 200msec after the FS and the BCLK provided. The CODEC voice path is established by releasing the mute function.

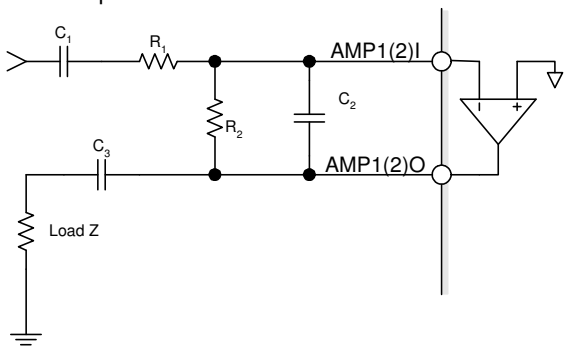


Universal op-amps

The op-amps for construction of the external filter.
The AMP1(2)I is negative input and the AMP1(2)O is output of the op-amp.

- Circuit example

Please design output load may become 8kΩ or more. The output load includes a feedback register and AC load. These op-amps are assumed to be used for 20kHz max cut off frequency LPF. And please design the gain may become –12~+6dB.
The following figure shows the circuit example.

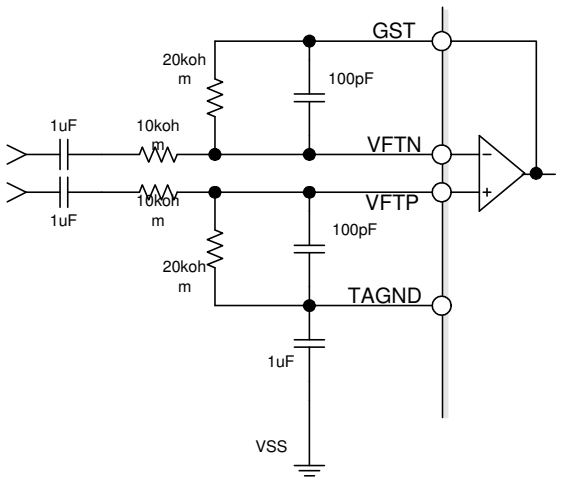


Each parameter is calculated as is shown below.

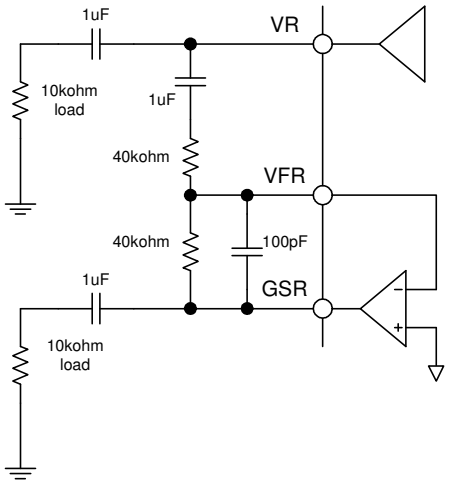
LPFcut-off frequency f_{CL}[Hz] : $f_{CL}=1/(2\pi R_2C_2)$
Output load L[Ω] : $L=R_2Z/(R_2+Z)$
Gain A[dB] : $A=20\log(R_2/R_1)$
HPF cut-off frequency f_{CH}[Hz] : $f_{CH}=1/(2\pi R_1C_1)$

APPLICATION CIRCUIT EXAMPLES

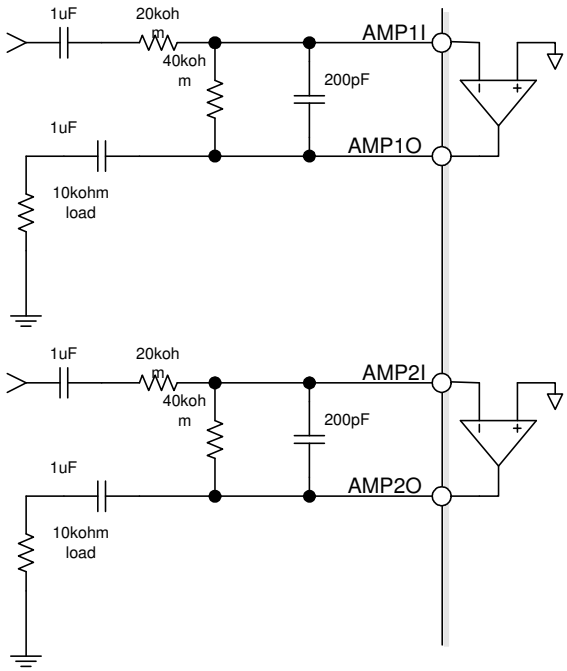
Analog input circuit



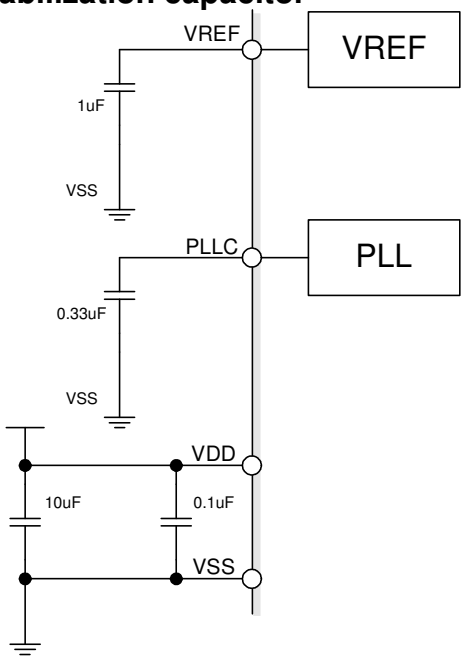
Analog output circuit



Universal op-amps



Power supply, PLL loop filter capacitor and analog ground stabilization capacitor



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