AK7719

Low Power DSP for Voice and Audio Processing

GENERAL DESCRIPTION

The AK7719 is a highly integrated digital signal processor (DSP) with four digital interface ports. AKM's DSP core is optimized for both narrowband and wideband voice processing, as well as full bandwidth digital audio processing. An integrated clock generator for the DSP master clock eliminates the need for external clocks. The RAM-based DSP can be programmed for user requirements. The AK7719 is housed in a 25-pin CSP package. It is a very low power device, suitable for mobile applications.

FEATURES

□ **Embedded DSP**
- **Flexible programming with built-in program and data memories**
- **Hardware accelerator**
- **Word length: 24-bits (Data RAM 24-bit floating point)**
- **Multiplier 20 x 20 → 40-bits (double precision available)**
- **Divider 20 / 20 → 20-bits**
- **ALU: 44-bit arithmetic operation (with 4-bit overflow margin)**
  24-bit floating point arithmetic and logic operation
- **Program RAM: 4096w x 36-bits**
- **Coefficient RAM: 2048w x 20-bits**
- **Data RAM: 2048w x 24-bits (24-bit floating point)**
- **Offset Register: 32w x 15-bits**
- **Delay RAM: 16384w x 24-bits(24-bit floating point)**
- **5625 steps at 16kHz sampling rate, 1875 steps at 48kHz sampling rate**
- **Internal clock generator**

□ **Audio Interface Format**
- **24-bit Left justified, I^2S,**
- **16/24bit linear, 8-bit A-law, 8-bit μ-law PCM**
- **Sampling rate 8kHz ~ 48kHz**
- **Up/Down Sampling rate converter for Port#2 (8kHz → 16kHz)**

□ **μC I/F: I^2C-Compatible, SPI**

□ **Operational, Sleep, Power down**

□ **Power Supply**
VDD (DSP Core): 1.2V ±0.1V
TVDD (PCM I/F): 1.6V ~ 3.6V

□ **Operating Temperature Range: -20°C ~ 85°C**

□ **Package: 25-Pin WL-CSP (2.62mm x2.93mm, 0.5mm pitch)**

□ **Power Consumption: 7.4mA (8.9mW) typ. (Narrowband Handset mode operation)**

■ Block Diagram

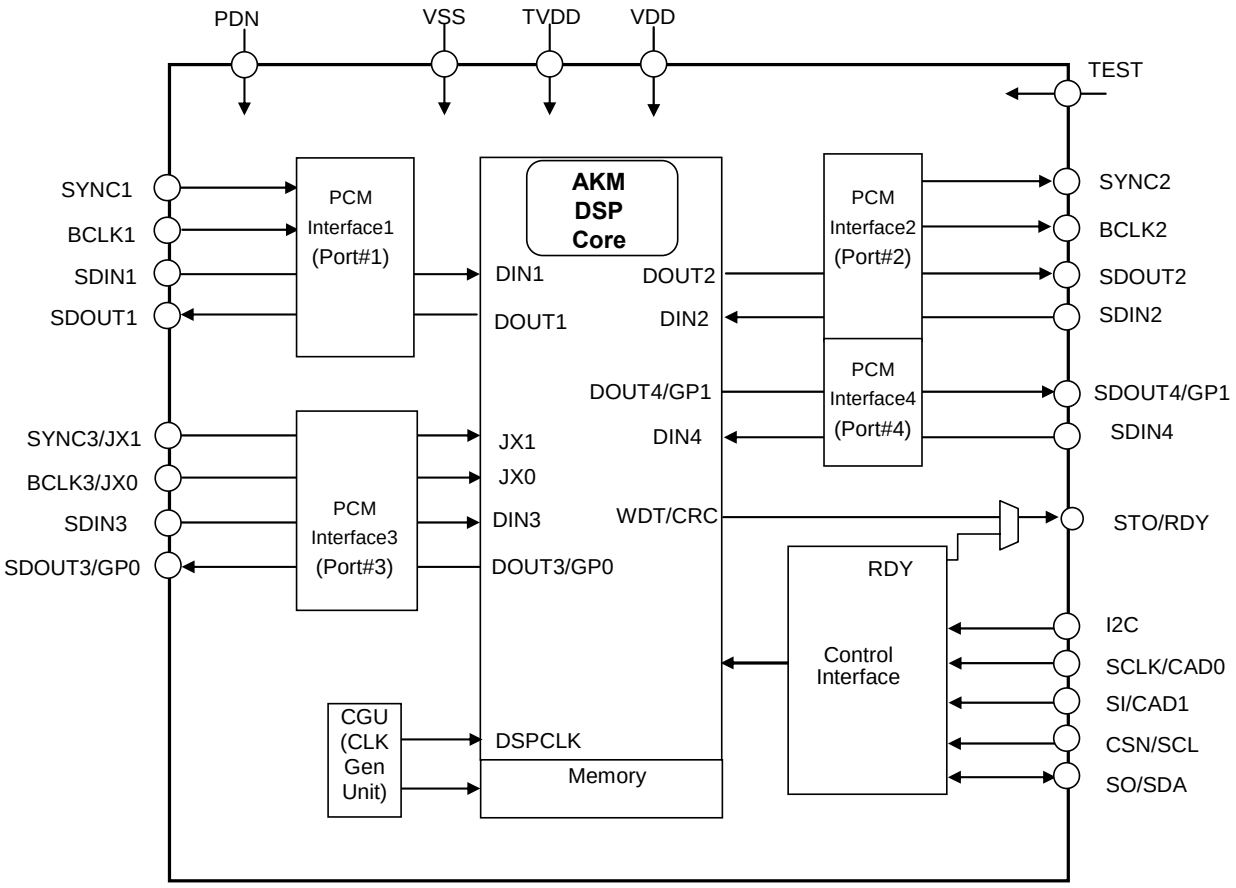
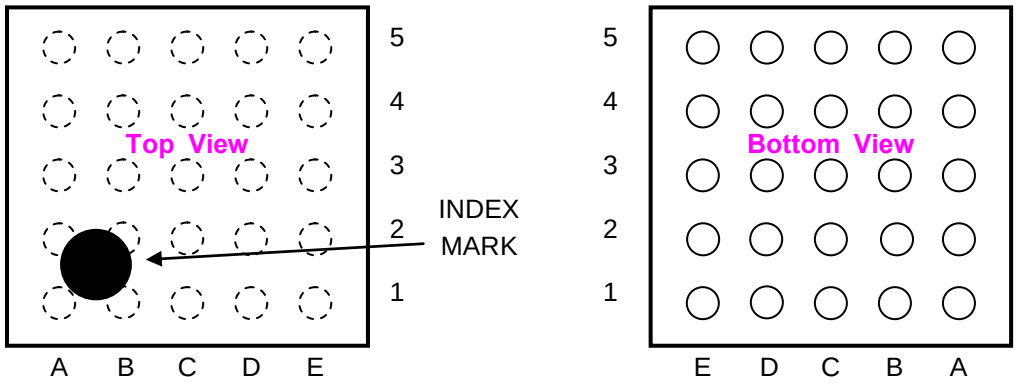


Figure 1. Block Diagram

■ Ordering Guide

AK7719ECB	-20 ~ +85°C	25-pin CSP (0.5mm pitch) Black type
AKD7719	Evaluation board for AK7719	

■ Pin Layout



5	PDN	SDIN1	SDOUT1	BCLK1	SYNC1
4	VDD	BCLK3/ JX0	SDIN3	SDOUT3/ GP0	SYNC2
3	VSS	SYNC3/ JX1	TEST	STO/ RDY	BCLK2
2	TVDD	I2C	SDIN4	SDOU4/ GP1	SDIN2
1	SI/CAD1	SCLK/ CAD0	CSN/ SCL	SO/ SDA	SDOUT2
	A	B	C	D	E

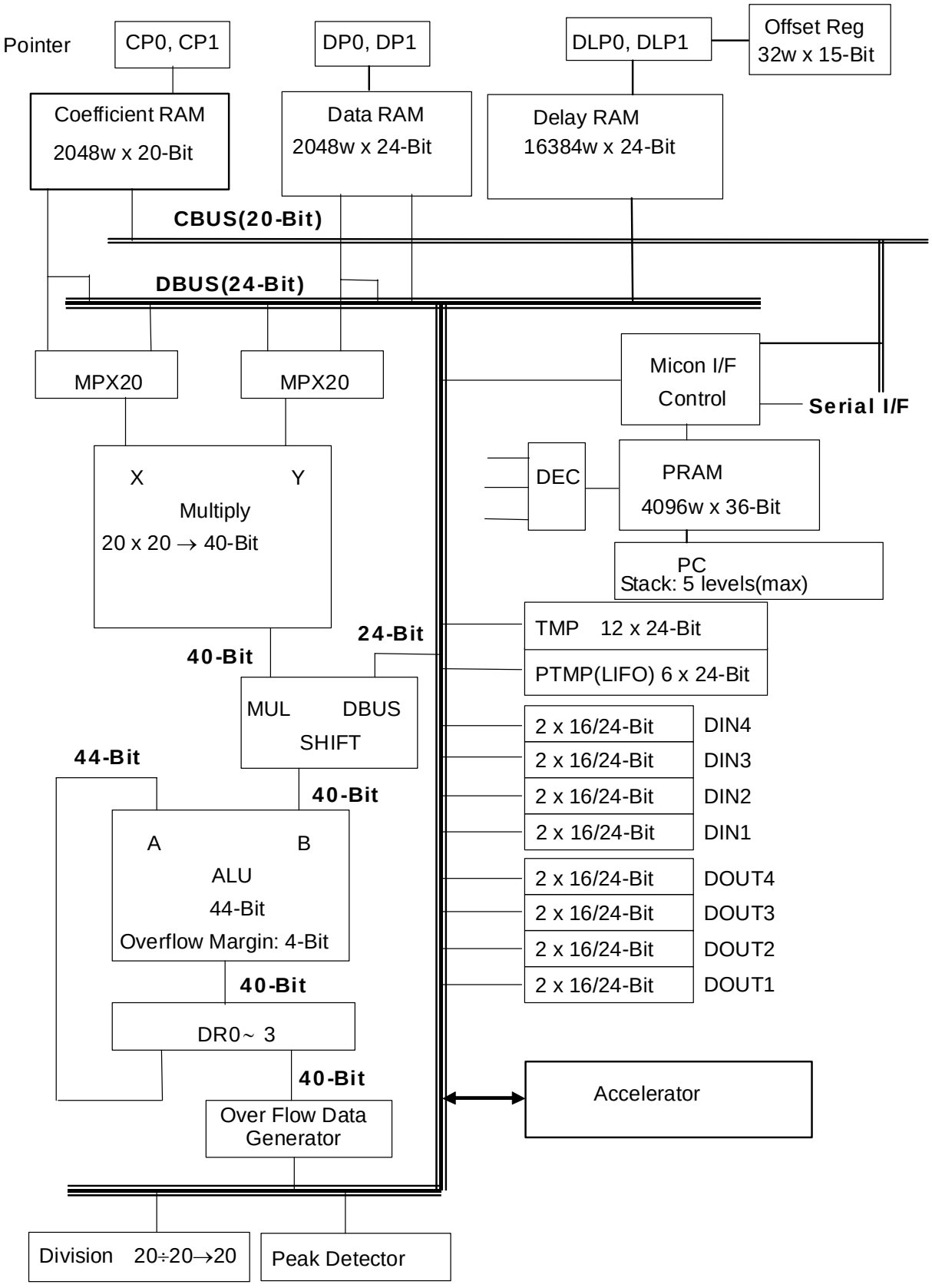
TOP View

PIN/FUNCTION

NO	Pin Name	I/O	Function
A4	VDD	-	Core Power Supply Pin 1.2V
A2	TVDD	-	I/O power Supply Pin 1.6~3.6V
A3	VSS	-	Ground Pin 0V
A5	PDN	I	P Power-Down Mode Pin "H": Power-up, "L": Power-down, reset the control register. The AK7719 must be reset once upon power-up.
D3	STO	O	Status Output Pin (Active High) (STRDY bit = "0")
	RDY		Data Write Ready output pin for control I/F (STRDY bit = "1")
E5	SYNC1	I	Frame Sync 1 pin
D5	BCLK1	I	Serial Data Clock 1 Pin AK7719 goes into standby state when BCLK1 is not present.
B5	SDIN1	I	Serial Data Input 1 Pin
C5	SDOUT1	O	Serial Data Output 1 Pin
E4	SYNC2	O	Frame Sync 1 pin
E3	BCLK2	O	Serial Data Clock 2 Pin
E2	SDIN2	I	Serial Data Input 2 Pin
E1	SDOUT2	O	Serial Data Output 2 Pin
B3	SYNC3	I	Frame Sync 3 pin (SELPT bit = "1")
	JX1		Conditional Jump 1 Pin (SELPT bit = "0")
B4	BCLK3	I	Serial Data Clock 3 Pin (SELPT bit = "1")
	JX0		Conditional Jump 0 Pin (SELPT bit = "0")
C4	SDIN3	I	Serial Data Input 3 Pin
D4	SDOUT3	O	Serial Data Output 3 Pin (SELDO3 bit = "0")
	GP0		DSP Programmable output 0 Pin (SELDO3 bit = "1")
C2	SDIN4	I	Serial Data Input 4 Pin
D2	SDOUT4	O	Serial Data Output 4 Pin (SELDO4 bit = "0")
	GP1		DSP Programmable output 1 Pin (SELDO4 bit = "1")
B2	I2C	I	Control Interface Mode Select Pin "H": I^2C, "L": SPI
B1	SCLK	I	Serial Clock Input pin SPI (I2C pin = "L")
	CAD0		Slave Address 0 Input pin I2C (I2C pin = "H")
C1	CSN	I	Chip select pin SPI (I2C pin = "L")
	SCL		Control Interface clock input pin I2C (I2C pin = "H")
D1	SO	O	Serial data output pin SPI (I2C pin = "L")
	SDA	I/O	Control Interface input/output acknowledge pin I2C (I2C pin = "H")
A1	SI	I	Serial data input pin SPI (I2C pin = "L")
	CAD1		Slave Address 1 Input pin I2C(I2C pin = "H")
C3	TEST	I	Test pin (pull-down resistor) must be connected to VSS.

Note 1. All input pins must not be allowed to float.
Note 2. I2C and CAD0/1 pins must be fixed to "L" (VSS) or "H" (TVDD).

DSP Block Diagram



■ Handling of Unused Pins

Unused I/O pins must be connected appropriately:

Pin Name	Setting
STO/RDY, SDOUT3/GPO, SDOUT4/GP1	Leave Open
SYNC1, BCLK1, SDIN1, SDIN2, SDIN3, SDIN4, SYNC3/JX1, BCLK3/JX0, TEST	Connect to VSS.

■ Pin States in Power-down Mode

The table below shows pin states when the PDN pin= "L".

NO	Pin Name	I/O	Pin state
D3	STO RDY	O	Low
C5	SDOUT1	O	SDIN2 data output
E4	SYNC2	O	SYNC1 data output
E3	BCLK2	O	BCLK1 data output
E1	SDOUT2	O	SDIN1 data output
D4	SDOUT3 GP0	O	SDIN4 data output
D2	SDOUT4 GP1	O	SDIN3 data output
D1	SO	O	Low level (I2C pin = "L": SPI)
	SDA	I/O	Hi-z (I2C pin = "H" :I^2C)

ABSOLUTE MAXIMUM RATINGS

(VSS=0V; All voltages are with respect to ground.)

Parameter	Symbol	min	max	Unit
Power Supply Voltage (DSP Core)	VDD	–0.3	1.6	V
Power Supply Voltage (Digital I/O)	TVDD	–0.3	4.1	V
Input Current (except for power supply pins)	IIN	-	±10	mA
Input Voltage	VIND	–0.3	TVDD+0.3	V
Operating Ambient Temperature	Ta	–20	85	°C
Storage Temperature	Tstg	–65	150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATION CONDITION

(VSS=0V; All voltages are with respect to ground.)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage Range (DSP core)	VDD	1.1	1.2	1.3	V
Supply Voltage Range (I/Os)	TVDD	1.6	1.8	3.6	V

Note 3. The power-up sequence with VDD and TVDD is not critical. The PDN pin should be held "L" when power is supplied. The PDN pin is allowed to be "H" after all power supplies are applied and settled.
Note 4. The external pull-up resistors at the SDA and SCL pins should be connected to TVDD voltage or less.

WARNING: AKM assumes no responsibility for the usage beyond the conditions in the datasheet.

ELECTRIC CHARACTERISTICS

DC CHARACTERISTICS

(Ta=-20ºC~85ºC; VDD=1.2V, TVDD =1.6V~3.6V; VSS =0V)

Parameter		Symbol	min	typ	max	Unit
High level input voltage		VIH	70%TVDD			V
Low level input voltage		VIL			30%TVDD	V
High level inptu voltage Iout=-200µA (Note 5)		VOH	TVDD-0.2			V
Low level input voltage Iout= 200µA (Note 5)		VOL			0.2	V
SDA low level output voltage Iout=3mA	TVDD ≥ 2.0V	VOL			0.4	V
	TVDD < 2.0V				20%TVDD	V
Input leak current		Iin			±10	µA

Note 5. Except for the SDA pin.

POWER CONSUMPTION

(Ta=25ºC; VDD=1.2V; TVDD=1.8V; VSS =0V, fin=1 KHz, fs=8kHz 16 bit (FS bits=0h, LAW bits = 0h, DIF bit = 2h, TESTC bit = 1h, DSP running with programmed connecting DIN1 with DOUT2 and DIN2 with DOUT1.

Parameter			min	typ	max	Unit
Power Supplies:						
Power-Up (PDN pin = "H") DSP-Operational State						
All Circuit Power-up						
	VDD	VDD=1.2V	-	3.1	-	mA
	TVDD	TVDD=1.8V (Note 6)	-	0.02	-	mA
	Power Consumption		-	3.76		mW
All Circuit Power-up						
	VDD	VDD=1.3V	-		20	mA
	TVDD	TVDD=3.6V (Note 6)	-		2.0	mA
	Power Consumption		-		33.2	mW
Power-Down state (PDN pin = "L"), (Note 7)						
VDD			-	2.4	8	µA
TVDD			-	0.2	1	µA

Note 6. The current of VDD, TVDD changes depending on the system frequency and contents of the DSP program.
Note 7. All digital input pins are fixed to TVDD or VSS.

SWITCHING CHARACTERISTICS

■ System Clock

(Ta= -20ºC ~ 85ºC, VDD=1.2V, TVDD= 1.6V ~ 3.6V, VSS=0V) CL=20pF (except SDA pin) or 400pF (SDA pin); unless otherwise specified

Parameter	Symbol	min	typ	max	Unit
Normal Operation mode: SYNC1/3, BCLK1/BCLK3 Input Timing					
SYNC1/3 Input Timing					
SYNC1/3 frequency	fs	8		48	kHz
BCLK1 Input Timing (Note 8, Note 9)	fBCLK	64		3072	kHz
BCLK1/3 Pulse width Low	tBCKL	0.4 x tBCLK			ns
BCLK1/3 Pulse width High	tBCKH	0.4x tBCLK			ns

Note 8. SYNC1 and BCLK1 or SYNC3 and BCLK3 should be synchronized and their sampling rates (fs) should be stable
Note 9. Required fBCLK: ≥ 2 (Data length set by LAW bit) x SYNC2 frequency

■ Reset and Standby

(Ta= -20ºC ~ 85ºC, VDD=1.2V, TVDD= 1.6V ~ 3.6V, VSS=0V)

Parameter	Symbol	min	typ	max	Unit
PDN (Note 10)	tPDN	600			ns

Note 10. The AK7719 can be reset by bringing the PDN pin = "L" upon power-up.

■ Serial Data Interface

(Ta= -20ºC ~ 85ºC, TVDD= 1.6V ~ 3.6V, VSS=0V, CL=20pF)

Parameter	Symbols	min	typ	max	Unit
SDIN1, SDIN3, SDIN4, SDOUT1, SDOUT3, SDOUT4					
Delay Time from BCLK1 "↑" to SYNC1 "↑" (Note 11)	tBSYD	20			ns
Delay Time from SYNC1 "↓" to BCLK1 "↑"	tSYBD	100			ns
Serial Data Input Latch Setup Time	tB1IDS	40			ns
Serial Data Input Latch Hold Time	tB1IDH	40			ns
Delay Time from SYNC1 to Serial Data Output	tSY1OD			40	ns
Delay Time from BCLK1 "↓" to Serial Data Output (Note 12)	tB1OD			40	ns
SDIN2, SDOUT2					
SYNC2 Duty cycle			50		%
Serial Data Input Latch Setup Time	tB2IDS	40			ns
Serial Data Input Latch Hold Time	tB2IDH	40			ns
Delay Time from SYNC2 to Serial Data Outputs	tSY2OD			40	ns
Delay Time from BCLK2 "↓"to Serial Data Output (Note 13)	tB2OD			40	ns
SDINn → SDOUTn (n=1, 2, 3)					
Delay time from SDINn to SDOUTn Output	tIOD			60	ns

Note 11. When the polarity of BCLK1 is inverted, delay time is from BCLK1 "↓"
Note 12. When the polarity of BCLK1 is inverted, delay time is from BCLK1 "↑".
Note 13. When the polarity of BCLK2 is inverted, delay time is from BCLK2 "↑".

■ Timing Diagram

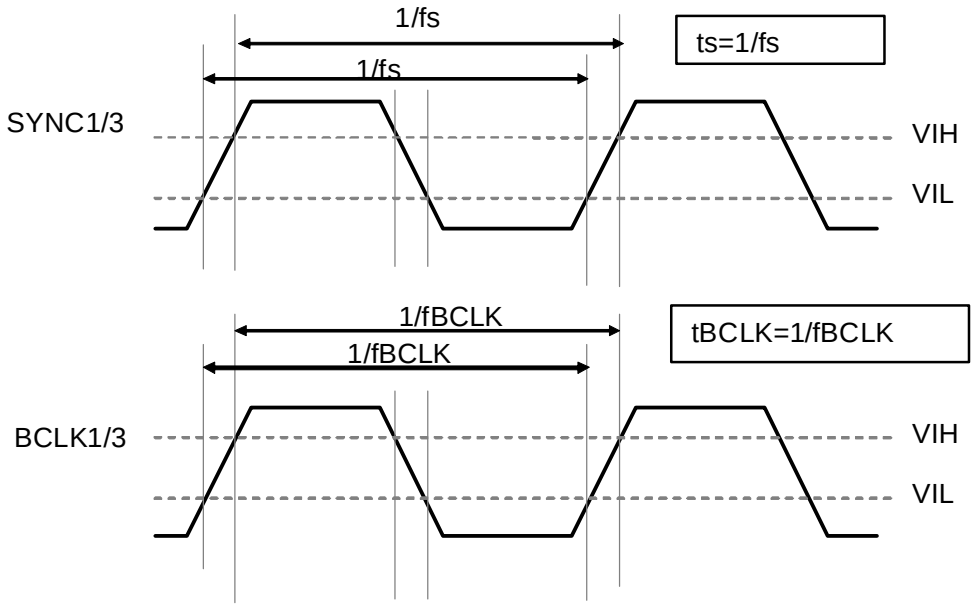


Figure 2. System Clock

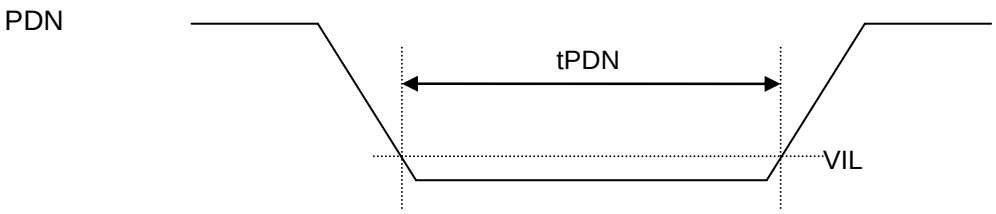


Figure 3. Power-down

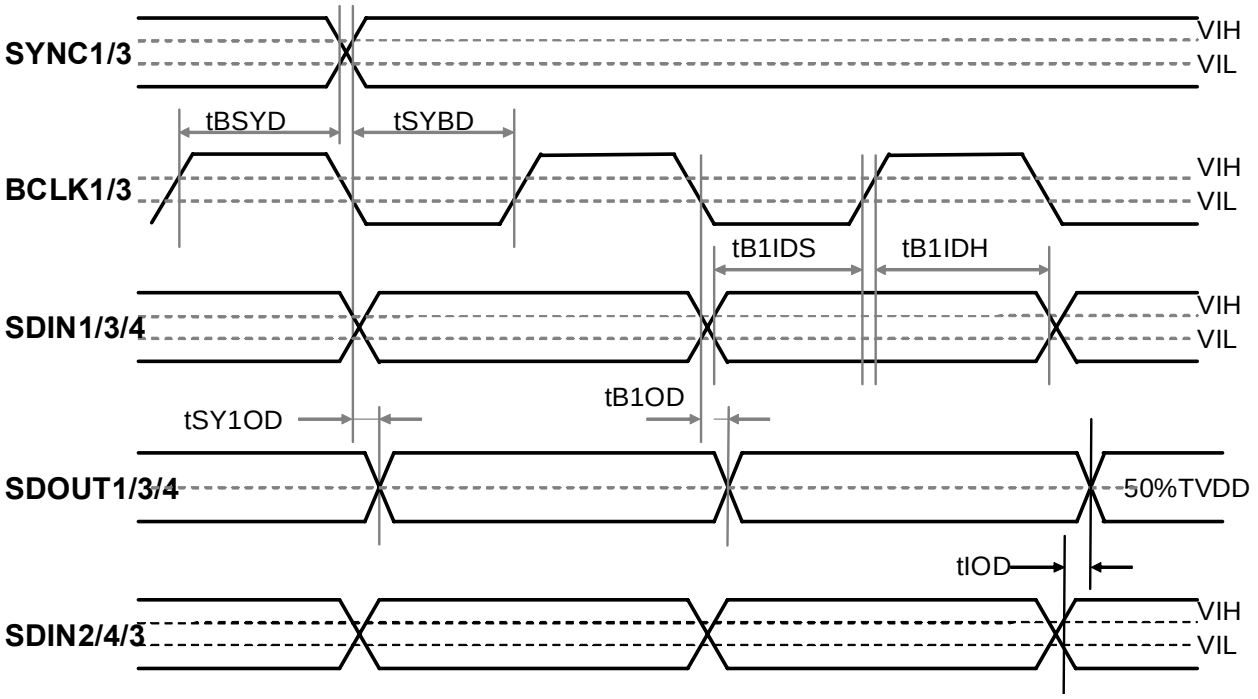


Figure 4. Serial Data Interface (Port#1, 3, 4)

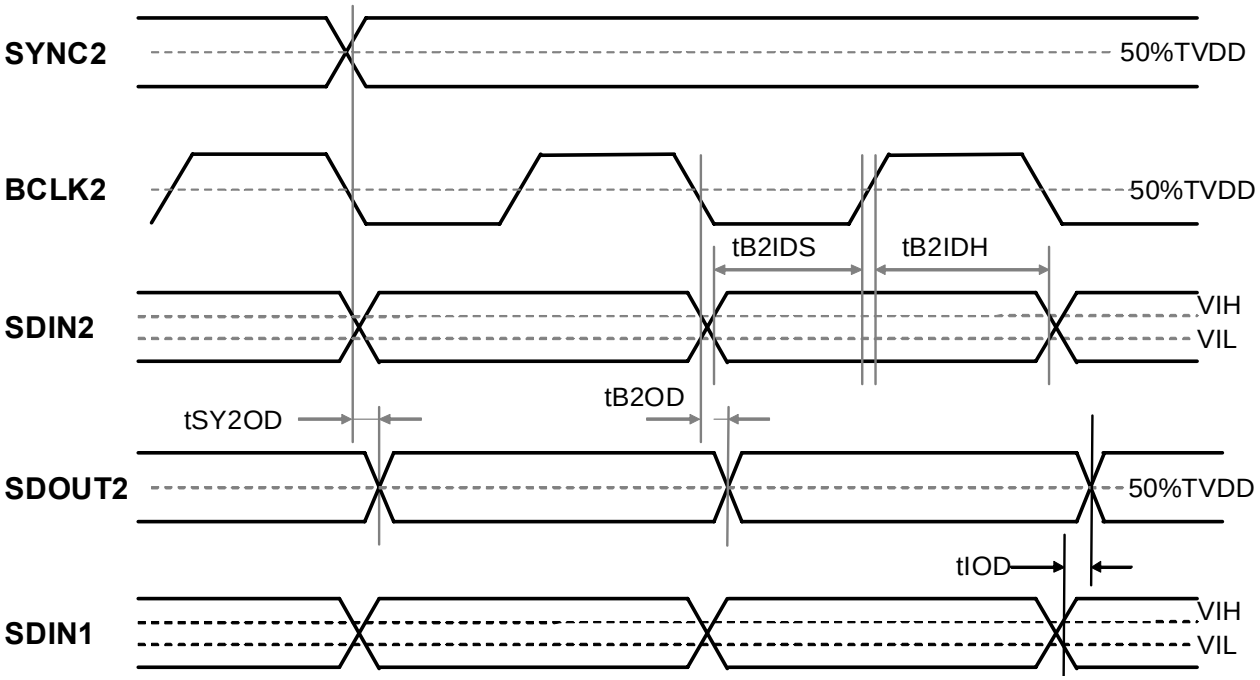


Figure 5. Serial Data Interface (Port#2)

■ µP Interface (SPI Mode)

(Ta= -20ºC ~ 85ºC, VDD=1.2V; TVDD=1.6~3.6V, VSS =0V; CL=20pF)

Parameter	Symbol	min	typ	max	Unit
µP Interface Timing (SPI mode)					
SCLK Fall Time	tSF			30	ns
SCLK Rise Time	tSR			30	ns
SCLK Frequency	fSCLK			4.0	MHz
SCLK Low Level Width	tSCLKL	120			ns
SCLK High Level Width	tSCLKH	120			ns
CSN High Level Width	tWRQH	500			ns
From CSN "↑" to PDN "↑"	tRST1	600			ns
From PDN "↑" to CSN "↓"	tIRRQ	100			µs
From SCLK "↓" to CSN "↑"	tWSC	500			ns
From SCLK "↑" to CSN "↑"	tSCW	800			ns
SI Latch Setup Time	tSIS	100			ns
SI Latch Hold Time	tSIH	100			ns
AK7719 → µP					
Delay Time from SCLK "↓"to SO Output	tSOS			100	ns
Hold Time from SCLK "↑" to SO Output (Note 14)	tSOH	100			ns

Note 14. Except when input the eighth bit of the command code.

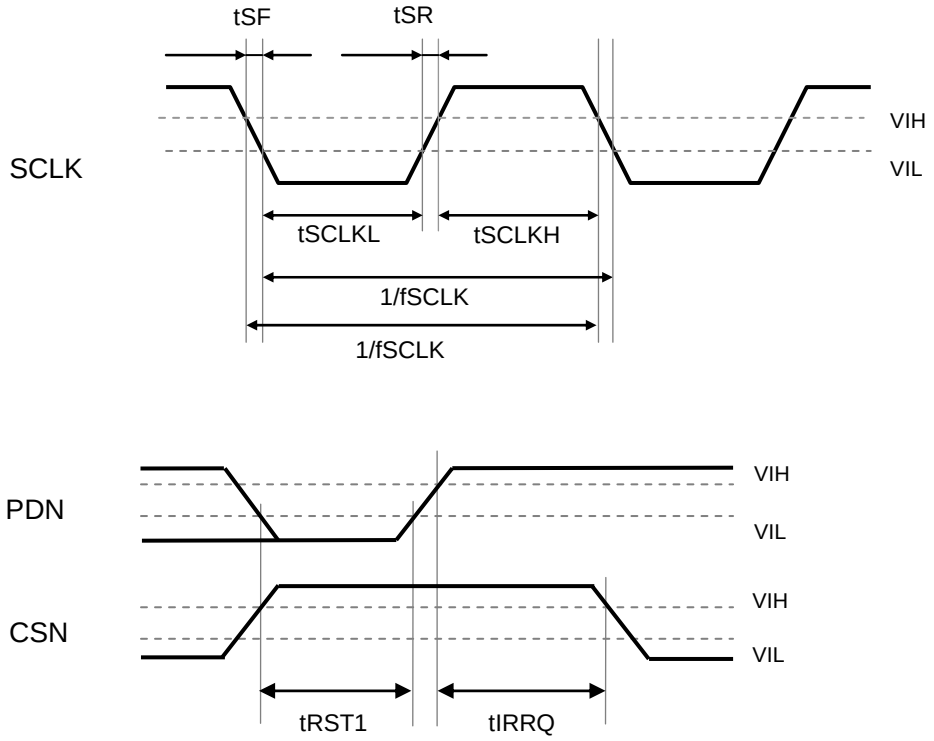


Figure 6. µP Interface 1 (SPI)

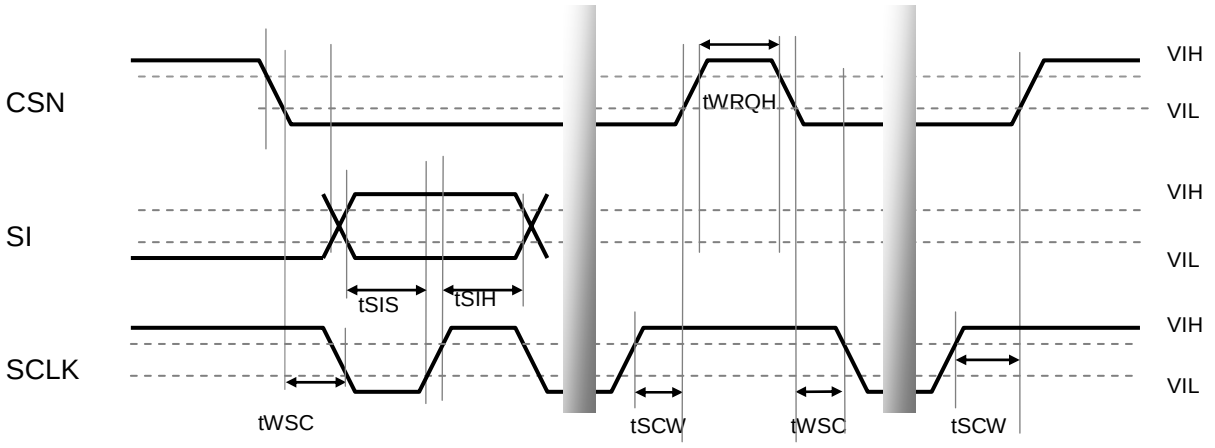


Figure 7. µP Interface 2 (SPI)

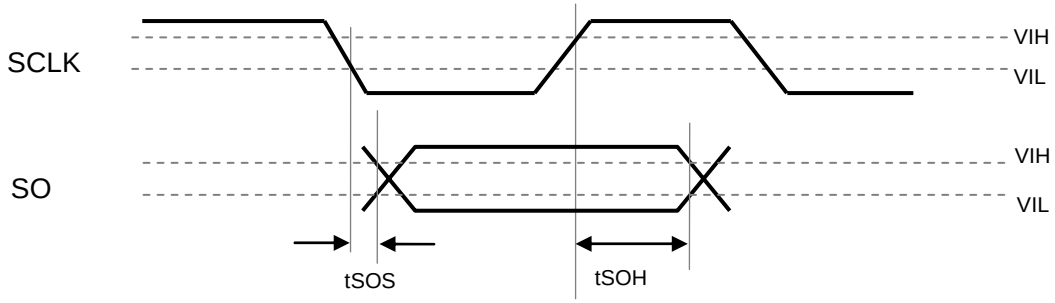


Figure 8. µP Interface 3 (SPI)

■ I²CBUS Interface

(Ta=-20ºC~85ºC, VDD=1.2V, VDD=1.6~3.6V, VSS =0V, CL=20pF)

Parameter	Symbol	min	typ	max	Unit
I²C Timing					
SCL clock frequency	fSCL	30		400	kHz
Bus Free Time Between Transmissions	tBUF	1.3			µs
Start Condition Hold Time (prior to first Clock pulse)	tHD:STA	0.6			µs
Clock Low Time	tLOW	1.3			µs
Clock High Time	tHIGH	0.6			µs
Setup Time for Repeated Start Condition	tSU:STA	0.6			µs
SDA Hold Time from SCL Falling	tHD:DAT	0		0.9	µs
SDA Setup Time from SCL Rising	tSU: DAT	0.1			µs
Rise Time of Both SDA and SCL Lines	tR			0.3	µs
Fall Time of Both SDA and SCL Lines	tF			0.3	µs
Setup Time for Stop Condition	tSU:STO	0.6			µs
Pulse Width of Spike Noise Suppressed by Input Filter	tSP	0		50	ns
Capacitive load on bus	Cb			400	pF

Note 15. I²C-bus is a trademark of NXP B.V.

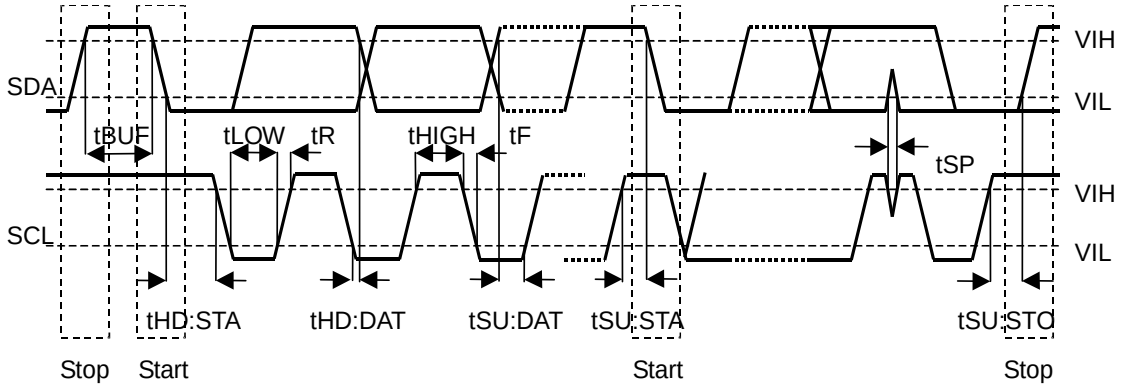
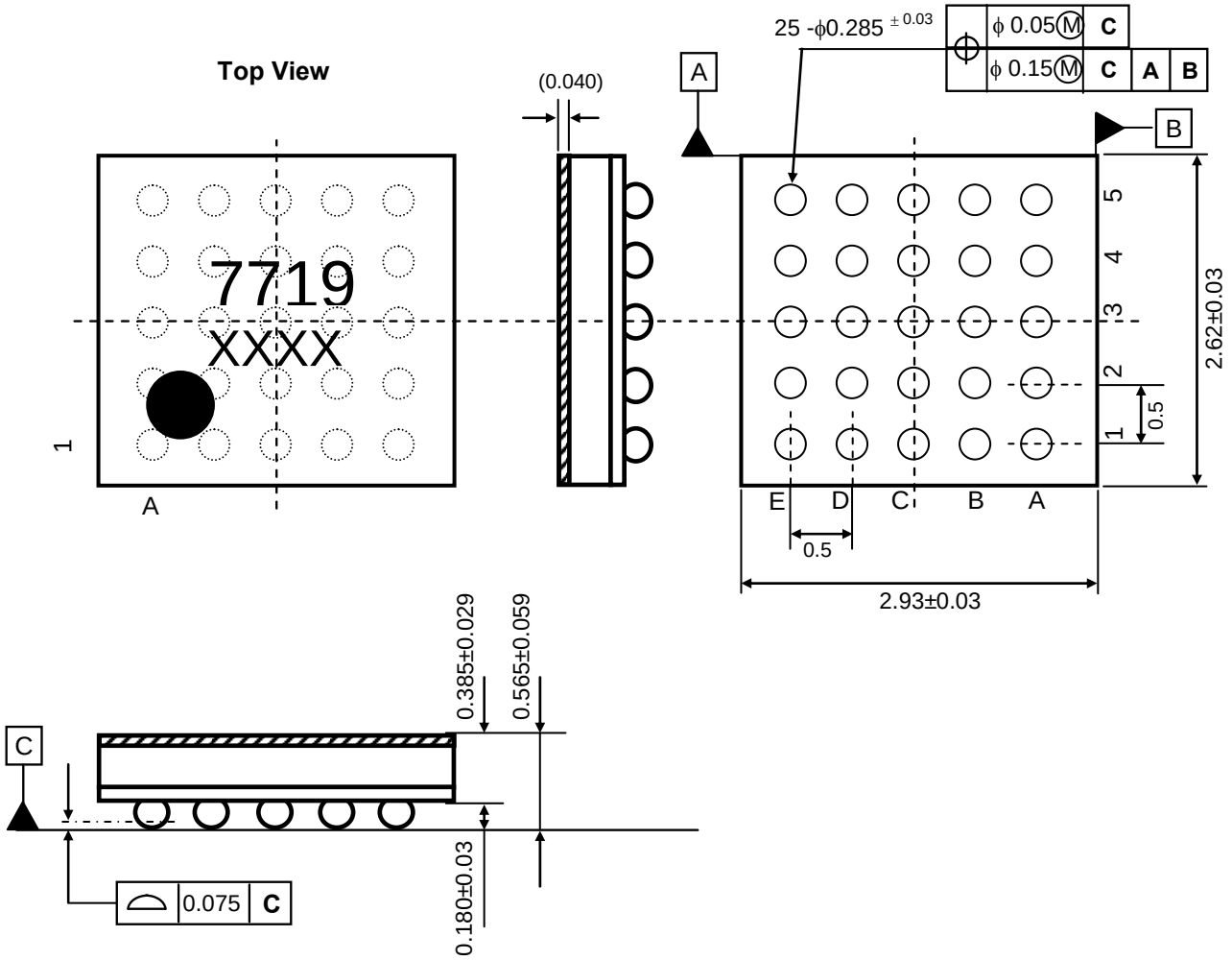


Figure 9. I²C Bus Interface

PACKAGE

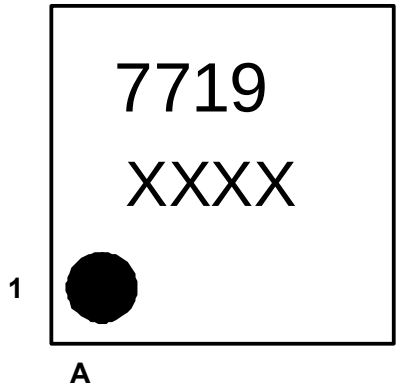
25pin CSP (Unit: mm)



■ Material & Lead Finish

Package: Epoxy, Halogen (bromine and chlorine) free
Solder ball material: SnAgCu

MARKING



XXXX: Date code (4 digit)

REVISION HISTORY

Date (Y/M/D)	Revision	Reason	Page	Contents
12/01/12	00	First Edition		
12/05/10	01	Specification Change	1	FEATURES Power Consumption: 6.2mA(7.5mW) → 7.4mA (8.9mW) typ.
			7	POWER CONSUMPTION Measurement Conditions: "TESTC bit =1h" was added. Power-Up, VDD=1.2V, TVDD=1.8V VDD: 1.7 → 3.1mA (typ) Power Consumption: 2.1 → 3.76mW (typ)

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