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# AK4183

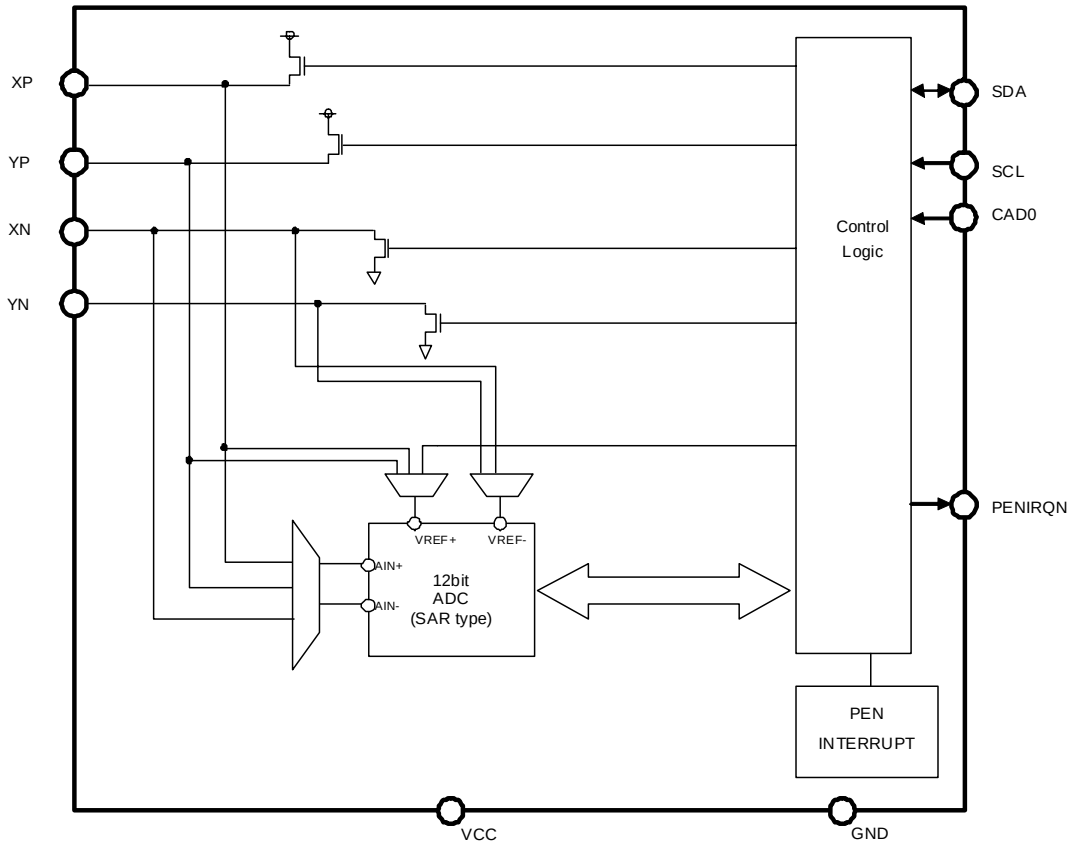
## I²C Touch Screen Controller

## GENERAL DESCRIPTION

The AK4183 is a 4-wire resistive touch screen controller that incorporates SAR type A/D converter. The AK4183 operates down to 2.5V supply voltage in order to connect a low voltage drive processor. The AK4183 can detect the pressed screen location by performing two A/D conversions. In addition to location, the AK4183 also measures touch pressure. As the package size of 10 pin TMSOP is 4.0mm x 2.9mm this is much smaller than QFN and BGA package. AK4183 is the best fit for cellular phone, PDA, or other portable devices.

## FEATURES

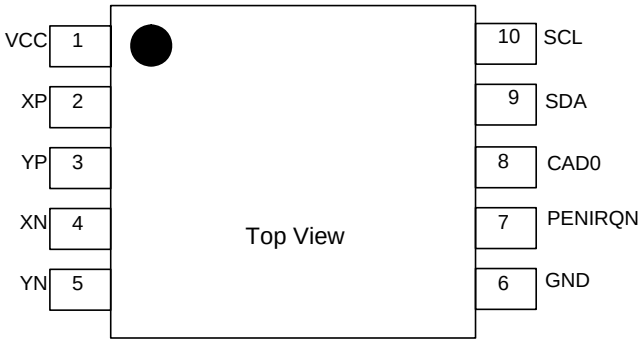
- **12-bit SAR type A/D Converter with S/H circuit**
- **Low Voltage Operation (2.5V ~ 3.6V)**
- **I²C bus I/F Supports**
  **(Standard mode 100 KHz, Fast mode 400 KHz)**
- **4-wire resistive touch screen Interface**
- **Pen Pressure Measurement**
- **Auto Power Down**
- **Continuous Read Operation**
- **Low Power Consumption (91μA @Fast mode)**
- **Package 10pin TMSOP**



## ■ Ordering Guide

| | | | |
|---|---|---|---|
| AK4183VT | -40°C ~ +85°C | 10pin TMSOP (0.5mm pitch) | Commercial Version |
| AK4183KT | -40°C ~ +85°C | 10pin TMSOP (0.5mm pitch) | Automotive Version |

## ■ Pin Layout




## PIN/FUNCTION

| No. | Signal Name | I/O | Description |
|---|---|---|---|
| 1 | VCC | - | Power Supply |
| 2 | XP | I/O | Touch Screen X+ plate Voltage supply<br>■ X axis Measurement: Supplies the voltage to X+ position input of the touch panel.<br>■ Y axis Measurement: This pin is used as the input for the A/D converter<br>■ Pen Pressure Measurement: This pin is the input for the A/D converter at Z1 measurement.<br>■ Pen Waiting State: Pulled up by an internal resistor (typ.10K ohm). |
| 3 | YP | I/O | Touch Screen Y+ plate Voltage supply<br>■ X axis Measurement: This pin is used as the input for the A/D converter<br>■ Y axis Measurement: Supplies the voltage to Y+ position input of the touch panel<br>■ Pen Pressure Measurement: Supplies the voltage to Y+ position input of the touch panel.<br>■ Pen Waiting State: OPEN state |
| 4 | XN | I/O | Touch Screen X- plate Voltage supply<br>■ X axis Measurement: Supplies the voltage to X- position input of the touch panel<br>■ Y axis Measurement: OPEN state<br>■ Pen Pressure Measurement: Supplies the voltage to X- position input of the touch panel<br>■ Pen Waiting State: OPEN state |
| 5 | YN | I/O | Touch Screen Y- plate Voltage supply<br>■ X axis Measurement: OPEN state<br>■ Y axis Measurement: Supplies the voltage to Y- position input of the touch panel<br>■ Pen Pressure Measurement: This pin is the input for the A/D converter at Z2 measurement.<br>■ Pen Waiting State: connected to GND. |
| 6 | GND | - | Ground |
| 7 | PENIRQN | O | Pen Interrupt Output<br>This pin is “L” during the pen down on pen interrupt enabled state otherwise this pin is “H”.<br>This pin is “L” during pen interrupt disabled state regardless pen touch. |
| 8 | CAD0 | I | $I^2C$ bus Slave Address bit 0 |
| 9 | SDA | I/O | $I^2C$ serial data |
| 10 | SCL | I | $I^2C$ serial clock |

## ABSOLUTE MAXIMUM RATINGS

(GND = 0V (Note 1))

| Parameter | Symbol | Min | max | Units |
|---|---|---|---|---|
| Power Supplies | VCC | -0.3 | 6.0 | V |
| Input Current (any pins except for supplies) | IIN | - | ±10 | mA |
| Input Voltage | VIN | -0.3 | 6.0(VCC+0.3) | V |
| Touch Panel Drive Current | IOUTDRV | | 50 | mA |
| Ambient Temperature (power supplied) | Ta | -40 | 85 | °C |
| Storage Temperature | Tstg | -65 | 150 | °C |

Note 1.All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

## RECOMMENDED OPERATING CONDITIONS

(GND = 0V (Note 1))

| Parameter | Symbol | Min | typ | max | Units |
|---|---|---|---|---|---|
| Power Supplies | VCC | 2.5 | 2.7 | 3.6 | V |

Note 1. All voltages with respect to ground.

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

## ANALOG CHARACTERISTICS

(Ta = -40°C to 85°C, VCC = 2.7V, $I^2C$ bus SCL=400 KHz, 12 bit mode)

| Parameter | | min | typ | max | Units |
|---|---|---|---|---|---|
| **ADC for Touch Screen** | | | | | |
| Resolution | | | 12 | | Bits |
| No Missing Codes | | 11 | 12 | | Bits |
| Integral Nonlinearity (INL) Error | | | | ±2 | LSB |
| Differential Nonlinearity (DNL) Error | | | ±1 | | LSB |
| Offset Error | | | | ±6 | LSB |
| Gain Error | | | | ±4 | LSB |
| Throughput Rate | | | 8.2 | | ksps |
| Touch Panel Driver On-Resistance<br>XP, YP<br>XN, YN | | | <br>5<br>5 | | <br>Ω<br>Ω |
| XP Pull Up Register (when pen interrupt enable) | | | 10 | | kΩ |
| **Power Supply Current** | | | | | |
| Normal Mode PD0=”0“ Addressed | Fast Mode: SCL=400KHz | | 91 | 200 | μA |
| | Standard Mode: SCL=100KHz | | 68 | 150 | μA |
| Power Down PD0=”0“ Not Addressed | Fast Mode: SCL=400KHz | | 23 | | μA |
| | Standard Mode: SCL=100KHz | | 6 | | μA |
| Full Power Down (Control command PD0= ”0“ SDA=SCL= VCC) | | | 0 | 3 | μA |

## DC CHARACTERISTICS (Logic I/O)

(Ta = -40 to 85°C, VCC = 2.5V to 3.6V)

| Parameter | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| "H" level input voltage | VIH | 0.7xVCC | - | | V |
| "L" level input voltage | VIL | | - | 0.3xVCC | V |
| Input Leakage Current | IILK | -10 | | 10 | µA |
| "H" level output voltage (PENIRQN pin@ Iout = -250µA) | VOH | VCC-0.4 | | | V |
| "L" level output voltage (PENIRQN pin @ Iout = 250µA)<br>(SDA pin @ Iout = 3mA) | VOL | | | 0.4 | V |
| Tri-state Leakage Current<br>All pins except for XP, YP, XN, YN pins<br>XP, YP, XN, YN pins | IOLK | <br>-10<br>-50 | | <br>10<br>50 | <br>µA<br>µA |

## SWITCHING CHARACTERISTICS

(Ta = -40 to 85°C, VCC = 2.5V to 3.6V)

| Parameter ($I^2C$ Timing) | Symbol | min | typ | max | Units |
|---|---|---|---|---|---|
| SCL clock frequency | fSCL | 30 | | 400 | kHz |
| Bus Free Time Between Transmissions | tBUF | 1.3 | | | µs |
| Start Condition Hold Time (prior to first Clock pulse) | tHD:STA | 0.6 | | | µs |
| Clock Low Time | tLOW | 1.3 | | | µs |
| Clock High Time | tHIGH | 0.6 | | | µs |
| Setup Time for Repeated Start Condition | tSU:STA | 1.3 | | | µs |
| SDA Hold Time from SCL Falling (Note 2) | tHD:DAT | 0 | | | µs |
| SDA Setup Time from SCL Rising | tSU:DAT | 0.1 | | | µs |
| Rise Time of Both SDA and SCL Lines | tR | | | 0.3 | µs |
| Fall Time of Both SDA and SCL Lines | tF | | | 0.3 | µs |
| Setup Time for Stop Condition | tSU:STO | 0.6 | | | µs |
| Pulse Width of Spike Noise Suppressed By Input Filter | tSP | 0 | | 50 | ns |
| Capacitive load on bus | Cb | | | 400 | pF |

Note 2. Data must be held for sufficient time to bridge the 300 ns transition time of SCL.

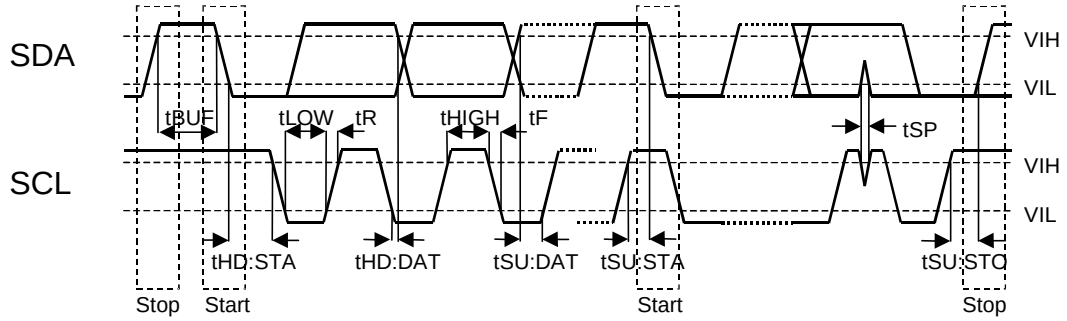



Figure 1. AK4183 Timing Diagram

## ■ A/D Converter for Touch Screen

The AK4183 incorporates a 12-bit successive approximation resistor (SAR) A/D converter for position measurement. The architecture is based on a capacitive redistribution algorithm, and an internal capacitor array functions as the sample/hold (S/H) circuit. The SAR A/D converter output is a straight binary format as shown below:

| Input Voltage | Output Code |
|---|---|
| (ΔVREF-1.5LSB)~ ΔVREF | FFFH |
| (ΔVREF-2.5LSB) ~ (ΔVREF-1.5LSB) | FFEH |
| --------- | --------- |
| 0.5LSB ~ 1.5LSB | 001H |
| 0 ~ 0.5LSB | 000H |

ΔVREF: (VREF+) – (VREF-)

Table 1. Output Code

## ■ The Position Detection of Touch Screen

A position detecting (X, Y position) on the touch panel is selected by the control command via the A2, A1, A0 bits in the control register. The mode of the position detecting is differential mode, the full scale (ΔVREF) is the differential voltage between the non-inverting terminal and the inverting terminal of the measured axis (e.g. X-axis measurement: $\Delta VREF = V_{XP} – V_{XN}$). The voltage difference on the A/D converter (ΔAIN) is the voltage between non-inverting terminals of the non-measured axis and the inverting terminal of the measured axis. (E.g. ΔAIN= (AIN+) - (AIN-) = $V_{YP}$-$V_{XN}$) The voltage difference (ΔAIN) is charged to the internal capacitor array during the sampling period. No current flows into the internal capacitor after the capacitor has been charged completely.
The required settling time to charge the internal capacitor array depends on the source impedance (Rin). If the source impedance is 600 ohm, the settling time needs at least 2.5μs (1 clock cycle period of SCL 400 KHz)
The position on the touch screen is detected by taking the voltage of one axis when the voltage is supplied between the two terminals of another axis. At least two A/D conversions are needed to get the two-dimensional (X/Y axis) position.

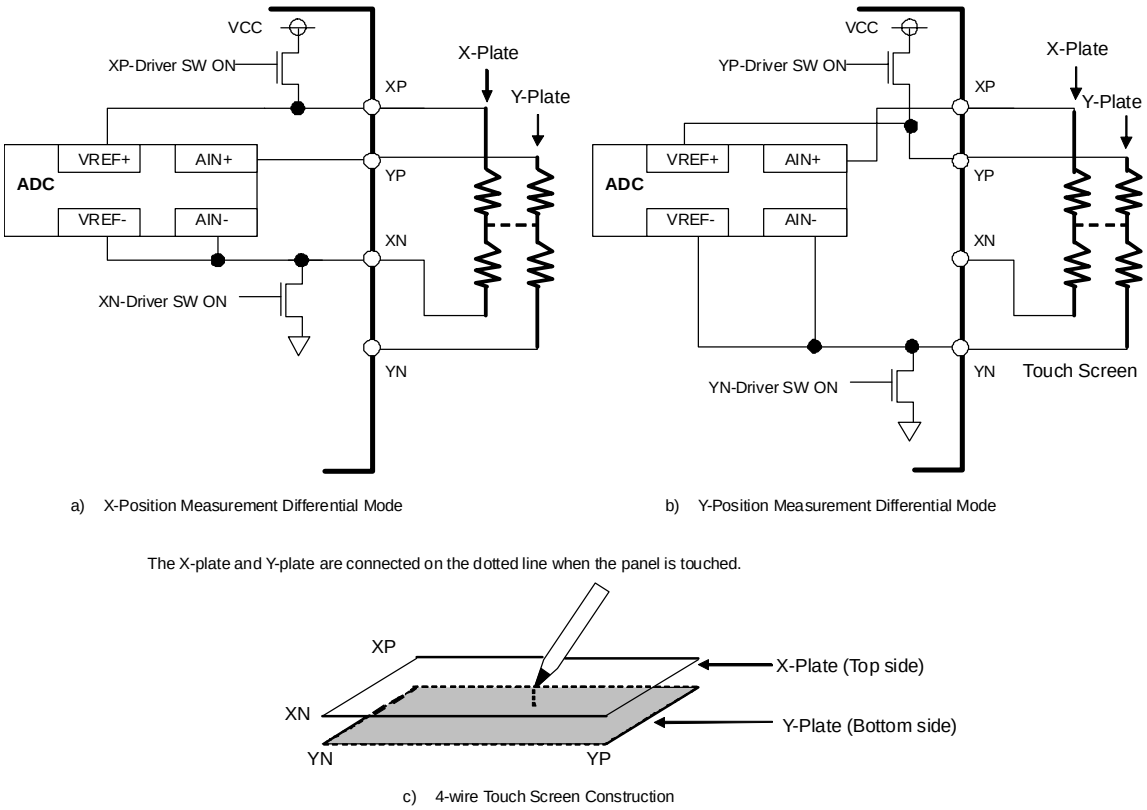



Figure 2. Axis Measurements

The differential mode position detection is typically more accurate than the single-ended mode. As the full scale of single-ended mode is fixed to the VCC, input voltage may exceed the full-scale reference voltage. This problem does not occur in differential mode. In addition to this, the differential mode is less influenced by power supply voltage variation due to the ratio-metric measurement.

## ■ The Pen Pressure Measurement

The touch screen pen pressure can be derived from the measurement of the contact resistor between two plates. The contact resistance depends on the size of the depressed area and the pressure. The area of the spot is proportional to the contact resistance. This resistance (Rtouch) can be calculated using two different methods.

The first method is that when the total resistance of the X-plate sheet is already known. The resistance, Rtouch, is calculated from the results of three conversions, X-position, Z1-Position, and Z2-Position, and then using the following formula:

Rtouch = (Rxplate) * (Xposition/4096) * [(Z2/Z1) – 1]

The second method is that when both the resistances of the X-plate and Y-plate are known. The resistance, Rtouch, is calculated from the results of three conversions, X-position, Y-Position, and Z1-Position, and then using the following formula:

Rtouch = (Rxplate*Xposition/4096)*[(4096/Z1) – 1] – Ryplate*[1 – (Yposition/4096)]

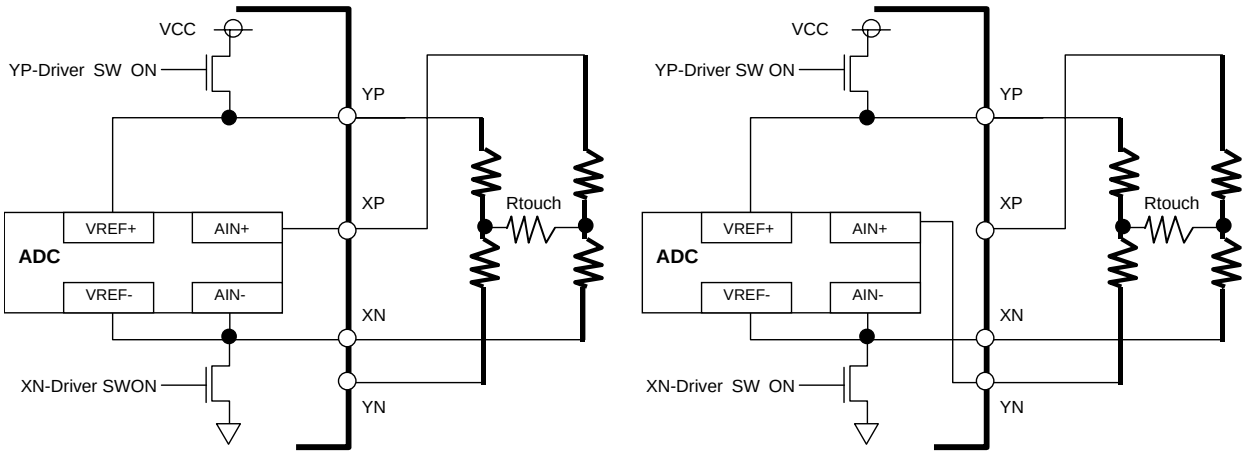



Figure 3. Pen Pressure Measurements

## ■ Digital I/F

The AK4183 operates with uP via $I^2C$ bus and supports the standard mode (100 KHz) and the fast mode (400KHz). Note that the AK4183 operates in those two modes and does not support a High speed mode $I^2C$-bus system (3.4MHz). The AK4183 can operate as the slave device on the $I^2C$ bus network.

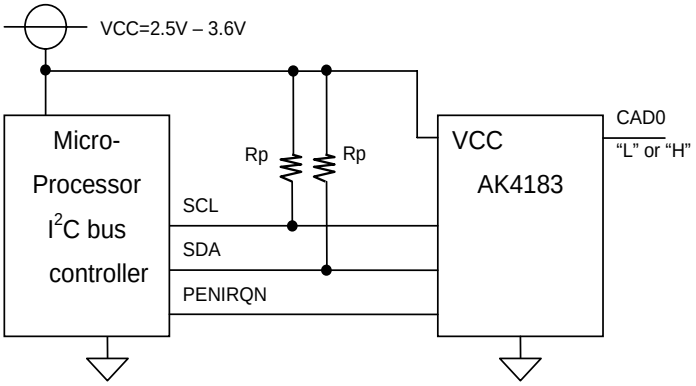



Figure 4. Digital I/F

[Start Condition and Stop Condition]
A HIGH to LOW transition on the SDA line while SCL is HIGH indicates a START condition. All sequences start by the START condition or Repeated Start Condition. Repeated Start condition is the same signal tradition as Start condition.
A LOW to HIGH transition on the SDA line while SCL is HIGH defines a STOP condition. All sequences are terminated by the STOP or Repeated Start condition. Repeated Start is also the Start condition of next transfer so that I2C bus cannot be idle.

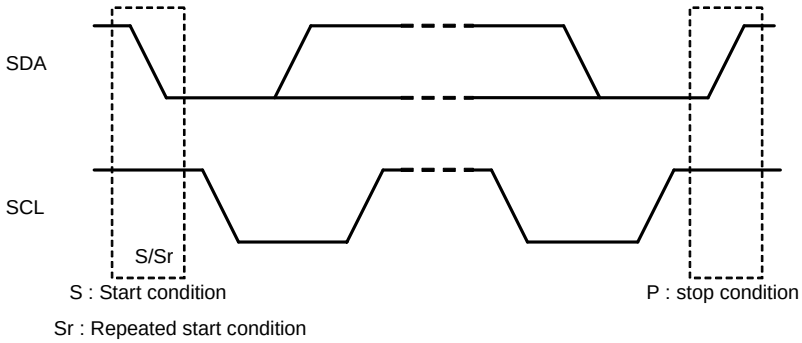



Figure 5. START and STOP Conditions

[Data Transfer]
All commands are preceded by a START condition. After the START condition, a slave address is sent. After the AK4183 recognizes the START condition, the device interfaced to the bus waits for the slave address to be transmitted over the SDA line. If the transmitted slave address matches an address for one of the devices, the designated slave device pulls the SDA line to LOW (ACKNOWLEDGE). The data transfer is always terminated by a STOP condition generated by the master device.

[Data Validity]
The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW except for the START and the STOP condition.

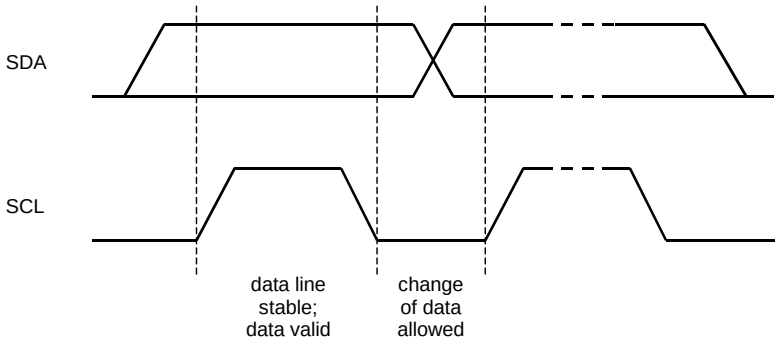



Figure 6. Bit Transfer on the I2C-Bus

[ACKNOWLEDGE]
ACKNOWLEDGE is a software convention used to indicate successful data transfers. The transmitting device will release the SDA line (HIGH) after transmitting eight bits. The receiver must pull down the SDA line during the acknowledge clock pulse so that that it remains stable "L" during "H" period of this clock pulse. The AK4183 will generates an acknowledge after each byte has been received.
In the read mode, the slave, the AK4183 will transmit eight bits of data, release the SDA line and monitor the line for an acknowledge. If an acknowledge is detected and no STOP condition is generated by the master, the slave will continue to transmit data. If an acknowledge is not detected, the slave will terminate further data transmissions and await the STOP condition.

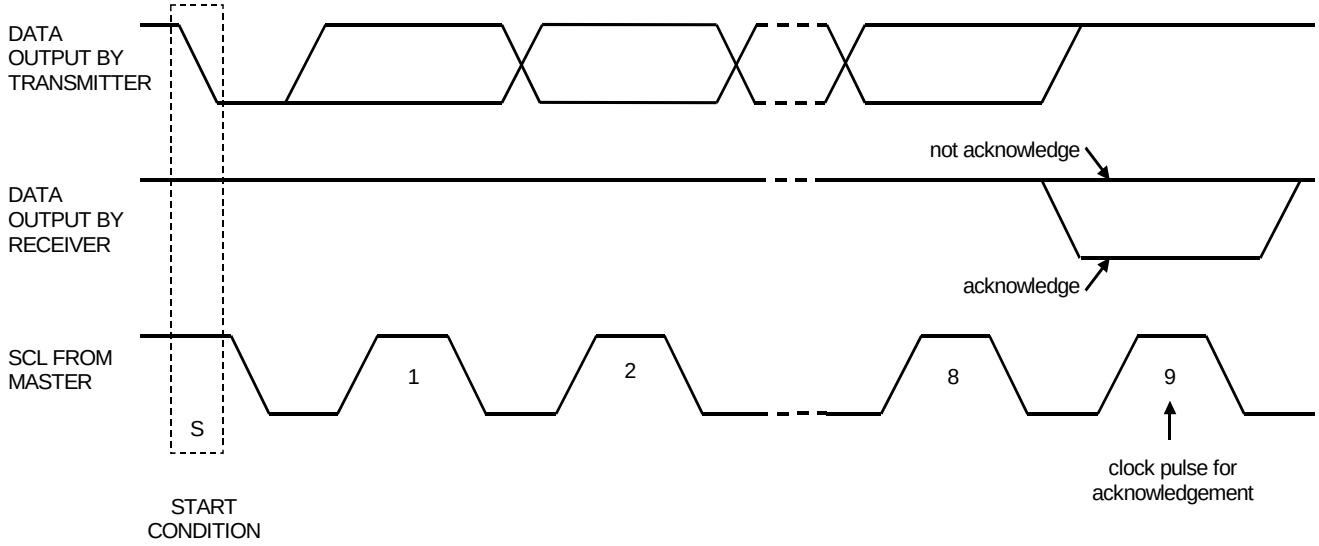



Figure 7. Acknowledge

[Address Byte]
The sequence of writing data is shown Figure 10. The address byte, which includes seven bits of slave address and one bit of R/W bit, is sent after the START condition. If the transmitted slave address matches an address for one of the device, the receiver who has been addressed pulls down the SDA line (acknowledge).
The most significant six bits of the slave address are fixed as "100100". The next one bit is CAD0 (device address bit). This bit identifies the specific device on the bus. The hard-wired input pin (CAD0 pin) sets CAD0 bit. The eighth bit (LSB) of the address byte (R/W bit) defines whether the master requests a write or read operation. A "1" indicates that the read operation is to be executed. A "0" indicates that the write operation is to be executed.

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| 1 | 0 | 0 | 1 | 0 | 0 | CAD0 | R/W |

(CAD0 should match with CAD0 pins)

Figure 8. Address Byte

[WRITE Operations]
The second byte that followed by address byte consists of the control command byte of the AK4183. The operational mode is determined by control command. The bit format is MSB first and 8 bits width. Control command is described in the Table 3. The AK4183 generates an acknowledge after each byte has been received. A control command transfer is terminated by a STOP condition or Repeated Start condition generated by the master. Refer to the Table 3 in detail.

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| S | A2 | A1 | A0 | X1 | PD0 | MODE | X2 |

Figure 9. Control Command Byte

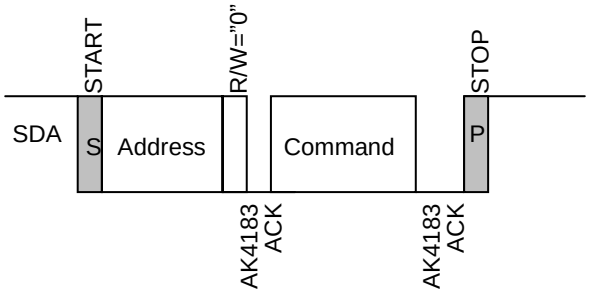



Figure 10. Single Write Transmission Sequence

[READ Operation]
The operation mode is determined by the write command just before read operation.
The AK4183 features two methods of read operation, single read operation and continuous read operation. The continuous read operation is a series of single read operation. Each single read operation in continuous read operation makes the AK4183 updated A/D conversion on each read operation. Write operation does not need to issue before each read operations are executed.

The channel selection of the AK4183 defines by the control command just before READ operation. When the address byte with R/W = "1" read operations are executed. A/D readout format is MSB first, 1byte or 2bytes width. Upper 8bits are valid on 8-bit mode and upper 12 bits are valid, and lower 4 bits are filled with zero on 12-bit mode.

[Single READ mode]
Read operation begins with START condition followed by the address byte with R/W= "1".The address matches the AK4183 generates ACK. And after transmission of the address byte, the master receives upper 8bit A/D data first, and generates ACK. The AK4183 transmits the remaining 4-bit A/D data and followed by 4-bit zero data (12bit mode). Master device receives 8bit A/D data (8bit mode). The master then generates NACK and stop condition or repeated start condition.

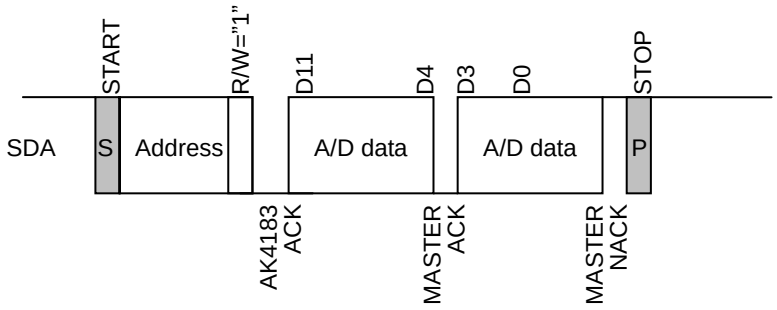



Figure 11. Single A/D data Read Sequence (12-bit mode)

[Continuous Read mode]
This continuous read operation enables the higher sampling rate and lower processor load than a single read operation. Because once control command is sent, it does not need to update control command on each read operation until another control command would like to be rewritten.

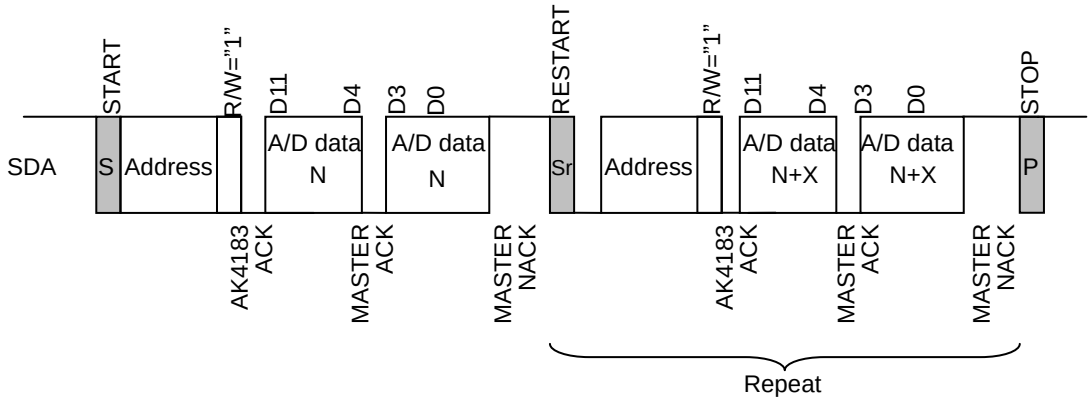



Figure 12 Continuous A/D data Read Sequence

## ■ Power on Sequence

It is recommended that the control command must be sent to fix the internal register when power up. This initiates all registers such as A2-0 bit, PD0 bit, and MODE bit. Once sending command to fix the internal register after first power up, the state of the AK4183 is held on the known-condition of state to ensure that AK4183 is going into desire mode to realize lowest mode. A command with PD0= "0" should be sent so that AK4183 will be set in the lowest power down mode.

## ■ Sleep Mode

AK4183 supports the sleep mode that enables touch panel interface to put open state and disables pen interrupt function. AK4183 goes into the sleep mode when control command is sent to AK4183 as shown Table 2. The selection of the sleep mode is set by "MODE" bit of the control command. The state of both the output of PENIRQN pin and the connection with touch panel interface (XP, YP, XN, and YN) are the following Table 2. AK4183 keeps the sleep mode until next control command is sent.

| Command | MODE bit | PENIRQN | Touch panel |
|---|---|---|---|
| 0111XX1X | 1 | Hi-z | Open |
| 0111XX0X | 0 | "H" output | Open |

Table 2 Sleep Command Setting

The timing of going into the sleep mode is the rising edge of the 16th SCL of the write operation. A/D conversion does not execute when the sleep command is sent. SDA pin is "H" since SDA is pull up.
In order for going to normal mode from sleep mode the command (S= "1") is sent. The timing of going back to normal mode is the rising edge of the 16thSCL. When the sleep command is sent again under the sleep mode the mode continues the same as before. The initial state after power up is in normal mode.

## ■ Control Command

The control command, 8 bits, provided to the AK4183 via SDA, is shown in the following table. This command includes start bit, channel selection bit, power-down bit and resolution bit. The AK4183 latches the serial command at the rising edge of SCL. Refer to the detailed information regarding the bit order, function, the status of driver switch, ADC input as shown in Table 3.

| BIT | Name | Function |
|---|---|---|
| 7 | S | Start Bit. "1" Accelerate and Axis Command, "0": Sleep mode Command |
| 6-4 | A2-A0 | Channel Selection Bits. Analog inputs to the A/D converter and the activated driver switches are selected. Please see the following table for the detail. |
| 3 | X1 | Don't care |
| 2 | PD0 | Power down bit (refer to power-down control) |
| 1 | MODE | Resolution of A/D converter. "0": 12 bit output "1": 8 bit output |
| 0 | X2 | Don't care |

| | Input | | | Status of Driver Switch | | | | ADC input (ΔAIN) | | Reference Voltage (ΔVREF) | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | A2 | A1 | A0 | XP | XN | YP | YN | AIN+ | AIN- | VREF+ | VREF- | Note |
| 0 | 1 | 1 | 1 | | | | | | | | | Sleep |
| 1 | 0 | 0 | 0 | ON | ON | OFF | OFF | YP | XN | XP | XN | Accelerate X-Driver |
| 1 | 0 | 0 | 1 | OFF | OFF | ON | ON | XP | YN | YP | YN | Accelerate Y-Driver |
| 1 | 0 | 1 | 0 | OFF | ON | ON | OFF | XP | XN | YP | XN | Accelerate Y+,X-Driver |
| 1 | 0 | 1 | 1 | OFF | ON | ON | OFF | YN | XN | YP | XN | |
| 1 | 1 | 0 | 0 | ON | ON | OFF | OFF | YP | XN | XP | XN | X-axis |
| 1 | 1 | 0 | 1 | OFF | OFF | ON | ON | XP | YN | YP | YN | Y-axis |
| 1 | 1 | 1 | 0 | OFF | ON | ON | OFF | XP(Z1) | XN | YP | XN | Z1 (Pen Pressure) |
| 1 | 1 | 1 | 1 | OFF | ON | ON | OFF | YN(Z2) | XN | YP | XN | Z2 (Pen Pressure) |

Table 3 Control Command List

## ■ Power-down Control

A/D converter and power-down control of touch driver switch are determined by PD0 bit.

| PD0 | PENIRQN | Function |
|---|---|---|
| 0 | Enabled | Auto power-down Mode<br>A/D converter is automatically powered up at the start of the conversion, and goes to power- down state automatically at the end of the conversion. All touch screen driver switches except for YN switch are turned off and relative pins are open state. Only YN driver switch is turned ON and YN pin is forced to the ground in this case. PEN interrupt function is enabled except for the sampling time and conversion time. |
| 1 | Disabled | ADC ON Mode<br>When X-axis or Y-axis are selected on the write operation with PD0 = "1" A/D converter and touch panel driver are always powered up until next conversion. This mode is effective if more settling time is required to suppress the electrical bouncing of touch plate.<br>PEN interrupt function is disabled and PENIRQN is forced to "L" state |

Table 4 Powers –Down Control

## ■ WRITE Operation Sequence (Figure 13)

The selection of channel input of AK4183 is determined by a command byte. The timing of the driver switch on is 18th falling edge of SCL regardless PD0 bit when accelerate command (A2= "0") is sent. The accelerate command is to accelerate the timing of desired driver SW ON to ensure that AK4183 needs more settling time. As for actually sampling is on the time of READ operation, it becomes possible to take settling time long even when the impedance of the touch screen is large.

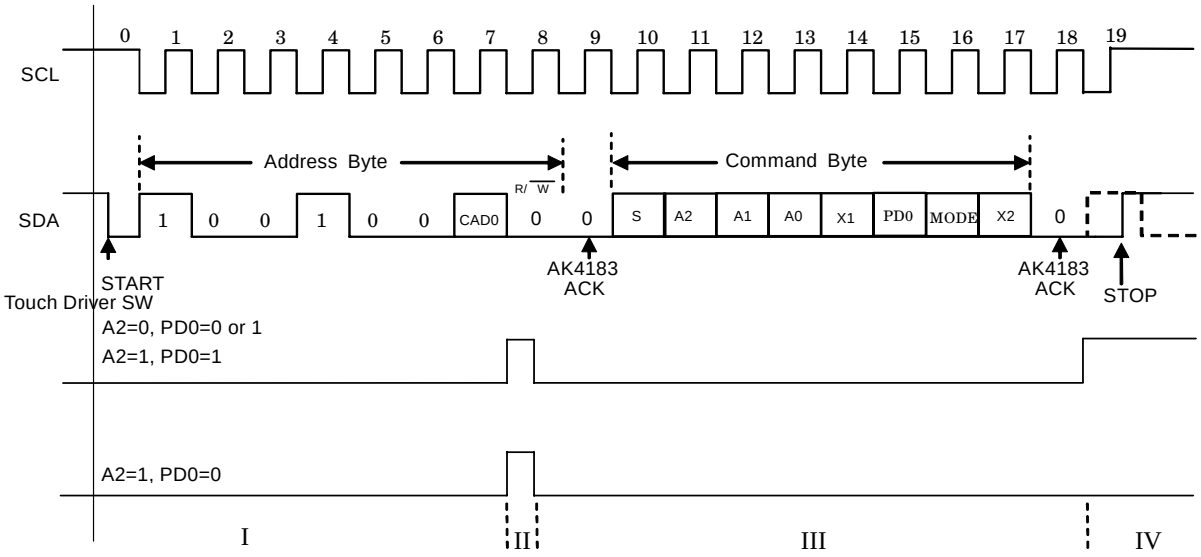



Figure 13 write operation and Driver SW timing

## ■ READ Operation Sequence (Figure 14)

A/D conversion is synchronized with SCL. Sampling time is the one SCL clock period (SCL7↓~ SCL8↓) on the end of writing address byte and then hold. A/D conversion is held on the next 12 SCL period (except MASTER ACK) .The readout sequence is that after command byte has been sent, AK4183 respond with acknowledge if the address matches. The MSB data byte will follow (D11~D4) then issued acknowledge by master. The LSB data byte (D3~D0, followed four “0”) will be followed by NOT acknowledge bit (NACK) from master in order to terminate the read transfer. The master will then issued STOP that ends read operation or Repeated Start condition that keeps write or read operation. The master will issue Repeated Start Condition or START condition followed by read operation again. AK4183 repeats A/D data updated [continuous read operation]. Master must issue STOP condition after terminating the last read out of A/D data.

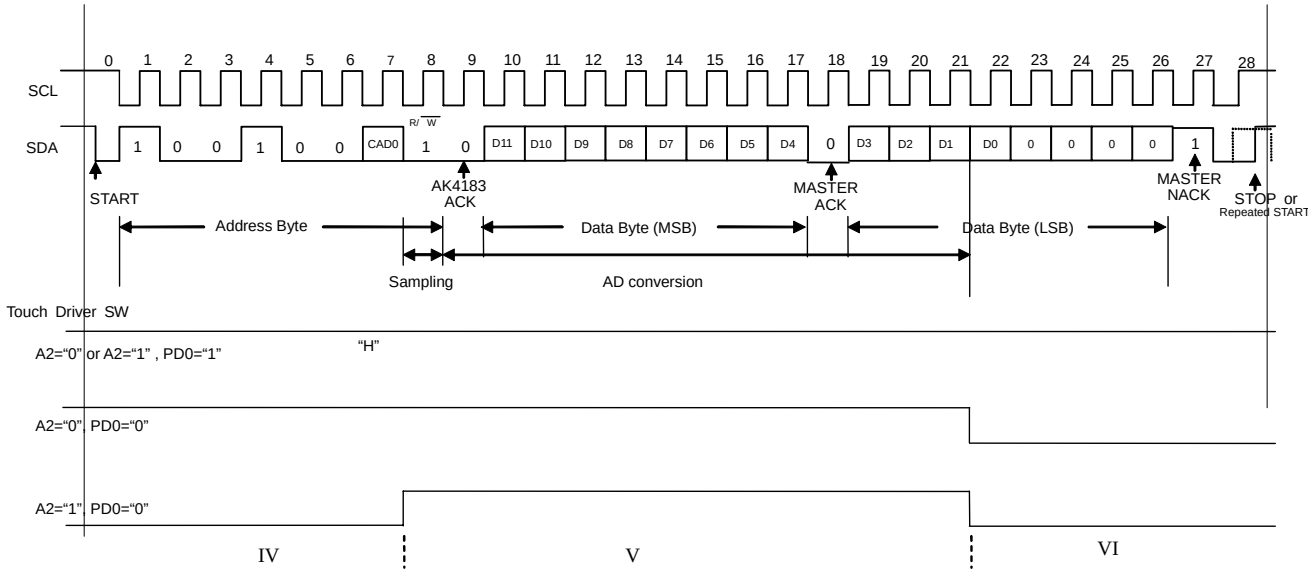



Figure 14 Read data Sequence

## ■ Pen Interrupt

The AK4183 has a pen-interrupt function to detect the pen touch on the touch panel. This function will use as the interrupt of the microprocessor. Pen interrupt function is enabled at power-down state. YN driver is on and this pin is connected to GND at the power down state. And XP pin is pulled up via an internal resister (Ri), typically 10KΩ. If the touch plate is touched by pen or stylus, the current flows via <VCC>-<Ri>-<XP>-<the plates>-<YN>-<GND>. The resistance of the plate is generally 1KΩ or less, PENIQRN pin is force to "L" level. If the pen is released, PENIRQN returns "H" level because two plates are disconnected, and the current does not flow via two plates.
The transition of PENIRQN is related to PD0 bit. PD0 bit is updated as shown below. (Please see "power-down control" for the detail. Once the control command with PD0= "1" is sent the pen-interrupt function is disabled.
The clock number under the write and the read operation refer to Figure 13 and Figure 14.

I. The period from start condition to SCL7↓
The level transition of PENIRQN pin is determined by PD0 bit of the previous command. When the previous command with PD0= "0" the pen-interrupt function will be enabled. PENIRQN pin is low when the panel is touch, PENIRQN pin is "H" when the panel is untouched. When the previous command with PD0= "1" is sent PENIRQN pin is low regardless of pen-touch

II. The period SCL7↓ to SCL8↑ on the write operation
The level of PENIRQN pin is always low regardless of PD0 bit and the state of panel (touched/untouched)

III. The period from SCL8↑ to SCL18↓ on the write operation
The level transition of PENIRQN pin is determined by PD0 bit of the previous command. When the previous command with PD0= "0" the pen-interrupt function will be enabled. PENIRQN pin is low when the panel is touch, PENIRQN pin is "H" when the panel is untouched. When the previous command with PD0= "1" is sent PENIRQN pin is low regardless of pen-touch

IV. The period from SCL18↓ on the write operation to SCL7↓ on the read operation
The level of PENIRQN pin is determined by the A2 bit and PD0 bit of the present command. PENIRQN pin is always low regardless pen-touch when command with A2 = "1" or PD0 = "1" is set. PENIRQN is determined by the pen-touch (touched/untouched) when command with A2= "1" and PD0= "1" is sent.

V. The period from SCL7↓ to SCL21↓ on the write operation
The AD input will sample the hold and the conversion will be done during this period. PENIRQN is always low.

VI. The period after SCL21↓ on the read operation
The level transition of PENIRQN pin is determined by PD0 bit of the present command. When the present command with PD0= "0" is sent the pen-interrupt function will be enabled. PENIRQN pin is low when the panel is touched. PENIRQN pin is "H" when the panel is untouched. When the present command with PD0= "1" are sent PENIRQN pin is low regardless of pen-touch.

It is recommended that the processor will mask the pseudo interrupt while the control command is issued or AD data is sent to processor.

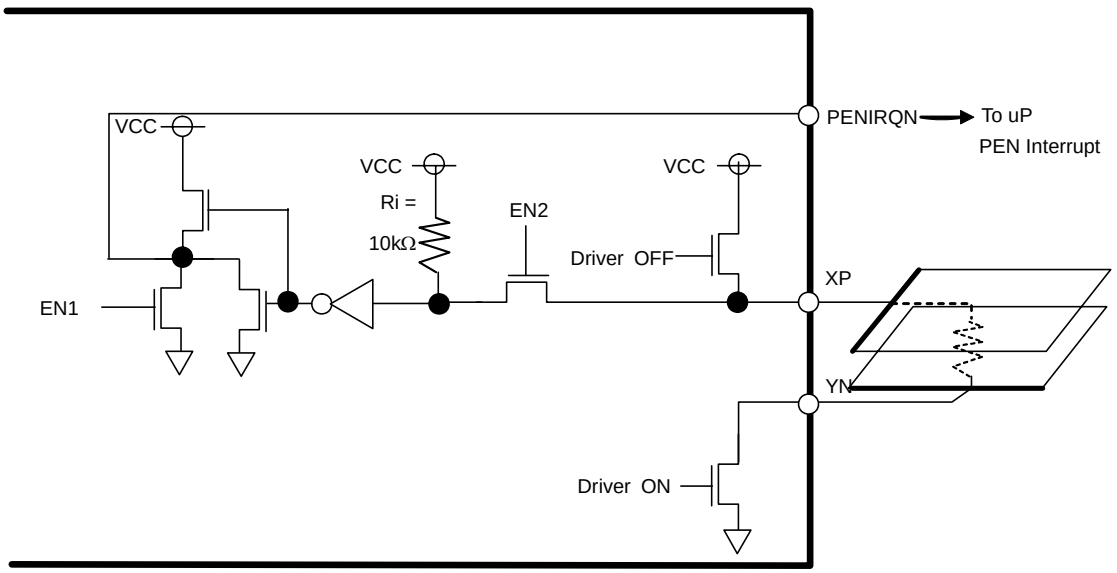
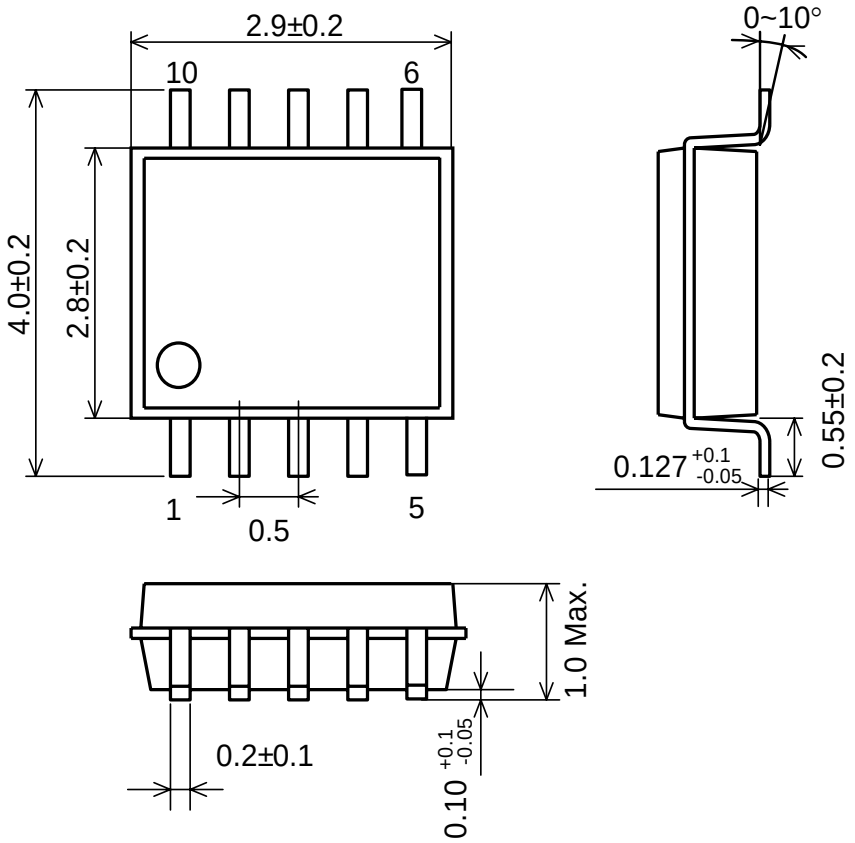



Figure 15 Pen interrupt function block

## PACKAGE

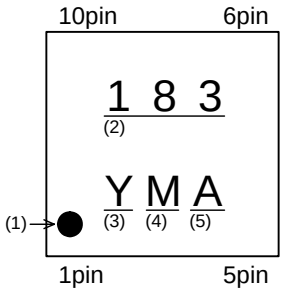
10pin TMSOP 0.5mm pitch (Unit : mm)




### ■ Package & Lead frame material

Package molding compound: Epoxy
Lead frame material: Cu
Lead frame surface treatment: Sn – Bi (Pb free)

## MARKING




(1) #1PinIndicator
(2) Chip No. (AK4183=183)
(3) Year 1 digit
(4) Month 1digit
(5) Manage code (internal)

## REVISION HISTORY

| Date (YY/MM/DD) | Revision | Reason | Page | Contents |
|---|---|---|---|---|
| 08/04/18 | 00 | First Edition | | |
| 08/12/09 | 01 | Product Addition | 2 | AK4183KT (Automotive Version) was added. |