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AK4184A

TSC with Keypad Scanner and GPIO Expander

GENERAL DESCRIPTION

The AK4184A is a 12-bit A/D converter witch operates 125kHz (max) sampling rate with a 4-wire resistive touch screen controller (TSC), including low-on resistance switches, touch pressure measurement capability, a maximum 6 x 5 keypad scanner, eight GPIO ports, and a PWM generator for LED contrast control. The AK4184A operates down to a 2.5V supply voltage, and it tolerates digital I/O interface voltage from 1.6V to AVDD in order to connect to low voltage controllers. The AK4184A supports SPI interface for communication to a host controller. The AK4184A is available in a 41-pin BGA package and it operates over a temperature range of -40°C to +85°C. The AK4184A is suitable for Cellular Phone, DSC, DVC, Smart Phone and MP3 player application systems.

FEATURES

- **SPI Serial Interface**
- **12 bit SAR A/D Converter with S/H Circuit**
- **4-wire Resistive Touch Screen Interface**
- **Sampling Frequency: 125 kHz (max)**
- **Pen Pressure Measurement**
- **6 x 5 Keypad Scanner**
- **8 GPIO Ports**
- **PWM Generator for LED Bias Control**
- **Power Supply:**
  - **AVDD = 2.5V ~ 3.6V**
  - **IOVDD = 1.6V ~ AVDD (Digital I/F)**
- **Low Power Consumption: 400μA**
- **Package: 41pin BGA (4mm x 4mm, pitch 0.5mm)**

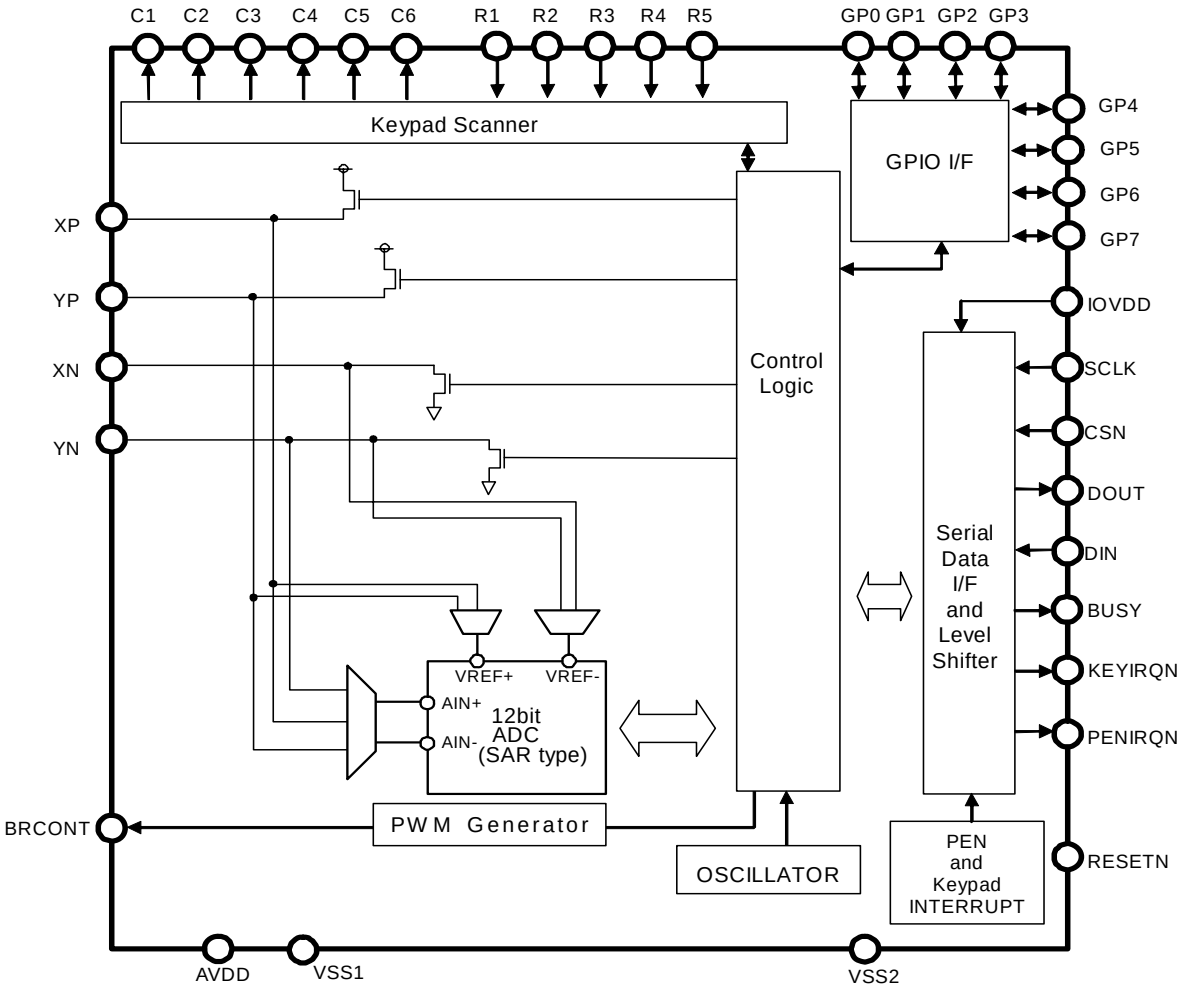
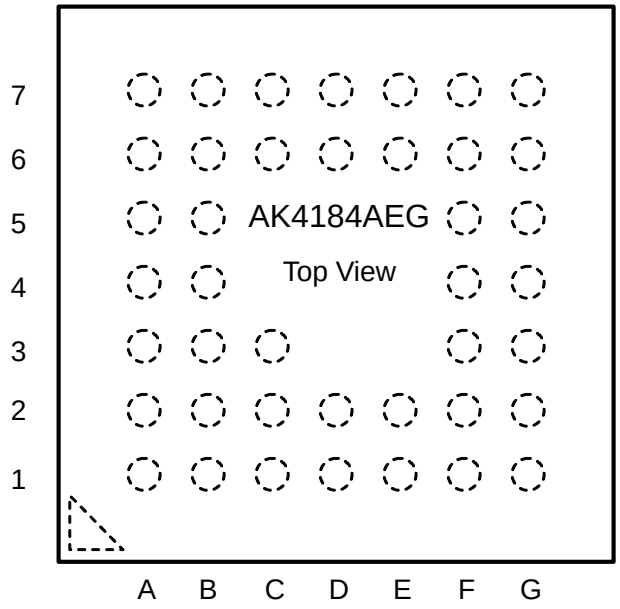


Figure 1. Block Diagram

■ Ordering Guide

AK4184AEG	–40 ~ +85°C	41pin BGA (4mm x 4mm, 0.5mm pitch)
AKD4184A	AK4184A Evaluation board	

■ Pin Layout (BGA 41pin)



7	NC	C3	C5	BRCONT	GP1	GP3	NC
6	C1	C4	C6	GP0	GP2	GP5	GP4
5	R4	C2				GP7	GP6
4	R3	R5				XP	AVDD
3	VSS2	R2	VSS2			XN	YP
2	IOVDD	R1	BUSY	DIN	CSN	PENIRQN	YN
1	NC	KEYIRQN	DOUT	SCLK	RESETN	VSS1	NC
	A	B	C	D	E	F	G

TOP View

PIN/FUNCTION

No.	Pin Name	I/O	Function
A1	NC	-	No Connection No internal bonding. This pin should be open or connected to the ground.
B1	KEYIRQN	O	Keypad Interrupt (Active Low) This pin is "L" on a key press (when the AK4184A is allowed to detect a key press). This pin is "H" after a debounce scan is completed. This is always "H" when the device is in key interrupt disable state.
C2	BUSY	O	BUSY output Keypad scanner: This pin stays "H" when the keypad scanner is on the debounce scan. Touch Screen controller: This pin stays "H" from the end of sampling time to the timing of the MSB data out.
C1	DOUT	O	Serial Data Output Data is clocked at SCLK falling edge. DOUT pin is "L" when this part does not produce data at the CSN="L". This pin is Hi-Z when CSN keeps "H".
D2	DIN	I	Serial Data Input Data is clocked on the rising edge of SCLK. Must keep "L" while not issuing command.
D1	SCLK	I	External Clock Input
E2	CSN	I	Chip Select Input (Active Low) Enables writing data to registers when CSN pin = "L".
E1	RESETN	I	Device Reset (Active Low)
F2	PENIRQN	O	Pen Interrupt Output (Active Low) PENIRQN pin is "L" when touch-screen pressed is detected and the CSN pin is "H". This pin is "H" irrespective of touch screen press when pen interrupt is not enabled. The state is dependent upon power down mode. See ■ Power-down control and ■ Pen Interrupt for reference.
G1	NC	-	No Connection No internal bonding. This pin should be open or connected to the ground.
F1	VSS1	-	Analog Ground
G2	YN	I/O	Touch Screen Y- plate Voltage Supply ■ Y axis measurement: Supplies voltage to the Y- position input ■ X axis measurement: OPEN state ■ Pen Pressure Measurement: This pin is the input for the A/D converter for Z2 measurement. ■ Pen Waiting State: connected to GND.
F3	XN	I/O	Touch Screen X- plate Voltage Supply ■ X axis measurement: Supplies voltage to the X- position input ■ Y axis measurement: OPEN state ■ Pen Pressure Measurement: Supplies the voltage to X- position input of the touch panel ■ Pen Waiting State: OPEN state
G3	YP	I/O	Touch Screen Y+ plate Voltage Supply ■ X axis measurement: Supplies voltage to the X- position input ■ Y axis measurement: OPEN state ■ Pen Pressure measurement voltage supply ■ Pen Waiting State: OPEN state
F4	XP	I/O	Touch Screen X+ plate Voltage Supply ■ X axis measurement: Supplies voltage to the X+ position input ■ Y axis measurement: This pin is used for the input to the A/D converter ■ Pen Pressure measurement: This pin is the input for the A/D converter for Z1 measurement. ■ Pen Waiting State: Pulled up by an internal resistor (typ.50KΩ).
G4	AVDD	-	Analog Power Supply: 2.5V ~ 3.6V

F5	GP7	I/O	GPIO7 pin
G5	GP6	I/O	GPIO6 pin
F6	GP5	I/O	GPIO5 pin
G6	GP4	I/O	GPIO4 pin
G7	NC	-	No Connection No internal bonding. This pin should be open or connected to the ground.
F7	GP3	I/O	GPIO3 pin
E6	GP2	I/O	GPIO2 pin
E7	GP1	I/O	GPIO1 pin
D6	GP0	I/O	GPIO0 pin
D7	BRCONT	O	Pulse width modulated output signal
C6	C6	O	Keypad Column 6
C7	C5	O	Keypad Column 5
B6	C4	O	Keypad Column 4
A7	NC	-	No Connection No internal bonding. This pin should be open or connected to the ground.
B7	C3	O	Keypad Column 3
B5	C2	O	Keypad Column 2
A6	C1	O	Keypad Column 1
B4	R5	I	Keypad Row 5
A5	R4	I	Keypad Row 4
C3	VSS2	-	Digital I/O Ground
A4	R3	I	Keypad Row 3
B3	R2	I	Keypad Row 2
A3	VSS2	-	Digital I/O Ground
B2	R1	I	Keypad Row 1
A2	IOVDD	-	Digital I/O Power Supply: 1.6V ~ AVDD

■ Handling of Unused Pin

The unused I/O pins must be processed appropriately as below.

Classification	Pin Name	Setting
Digital	GP0 ~ GP8, R1 ~ R5	These pins should be open.
	C1 ~ C6, BRCONT	These pins should be open.

ABSOLUTE MAXIMUM RATINGS

(VSS1, VSS2 = 0V: Note 1)

Parameter		Symbol	min	max	Units
Power Supply (Note 2)	Analog	AVDD	-0.3	6.0	V
	Digital I/F	IOVDD	-0.3	6.0	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage (Note 3)		VINA	-0.3	AVDD+0.3 or 6.0	V
Digital Input Voltage (Note 4)		VIND	-0.3	IOVDD+0.3 or 6.0	V
Touch Panel Drive Current		IOUTDRV	-	50	mA
Ambient Temperature (power supplied)		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note 1. All voltages with respect to ground.
Note 2. VSS1 and VSS2 must be connected to the same analog ground plane.
Note 3. XP, YP, XN, YN pins. Max is smaller value between (AVDD+0.3)V or 6.0V.
Note 4. DIN, CSN, SCLK, RESETN, R1 ~ R5, GP0 ~ GP7 pins. Max is smaller value between (IOVDD+0.3)V or 6.0V. Pull-up resistors on BRCONT pin and GP0 ~ GP7 pins should be connected to (IOVDD+0.3) V or less voltage.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMEND OPERATING CONDITIONS

(VSS1, VSS2 = 0V: Note 1)

Parameter	Symbol	min	typ	max	Units
Power Supplies	AVDD	2.5	3.3	3.6	V
Digital I/O Power Supply	IOVDD	1.6	3.3	AVDD	V

Note 1. All voltages are with respect to ground.

WARNING: AKEMD assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

Ta = -40°C to 85°C, AVDD = IOVDD = 3.3V, fs = 125 KHz, fSCLK=5MHz

Parameter	min	typ	max	Units
ADC for Touch Screen				
Resolution	-	12	-	Bits
No Missing Codes	11	12	-	Bits
Integral Nonlinearity (INL) Error	-	-	±2	LSB
Differential Nonlinearity (DNL) Error	-	±1	-	LSB
Offset Error	-	-	±6	LSB
Gain Error	-	-	±4	LSB
Touch Panel Drivers Switch On-Resistance				
XP, YP, RL = 300Ω	-	10	-	Ω
XN, YN, RL = 300Ω	-	10	-	Ω
XP Pull Up Register (when pen interrupt enable)	-	50	-	KΩ
Power Supply Current				
Touch Screen only fs = 125KHz (PD bit = "0")	-	400	680	μA
Touch Screen only fs = 125KHz (PD bit = "1")	-	500	850	μA
Oscillator on, Touch Screen Driver off, A/D power down	-	72	120	μA
Full Power Down (all blocks power down when CSN = "H", RESETN = "H")	-	0	5	μA

DC CHARACTERISTICS (Logic I/O)

Ta = -40°C to 85°C, IOVDD = 1.6V to 3.6V

Parameter	Symbol	min	typ	max	Units
Digital Input (CSN, SCLK, DIN, R1 ~ R5, GP0 ~ GP7 pins)					
"H" level input voltage	VIH	0.8xIOVDD	-	-	V
"L" level input voltage	VIL	-	-	0.2xIOVDD	V
Input Leakage Current	IILK	-10	-	10	μA
Digital Output (DOUT, BUSY, BRCONT, PENIRQN, KEYIRQN pins)					
"H" level output voltage (@ Iout = -250μA)	VOH	IOVDD-0.4	-	-	V
"L" level output voltage (@ Iout = 250μA)	VOL	-	-	0.4	V
Digital Output (GP0 ~ GP7 pins)					
"H" level output voltage (@ Iout = -1.5mA)	VOH	IOVDD-0.4	-	-	V
"L" level output voltage (@ Iout = 1.5mA)	VOL	-	-	0.4	V
Digital Output(C1 ~ C6)					
"H" level output voltage (@ Iout = -1.5mA)	VOH	IOVDD-0.4	-	-	V
Resistance					
Pulldown Resistance (R1 ~ R5 pins)	Rkey	-	16	-	KΩ
Pulldown Resistance (GP0 ~ GP7 pins @ input)	Rgp	-	1000	-	KΩ
Tri-state Leakage Current	IOLK				
All pins except for XP, YP, XN, YN pins		-10	-	10	μA
XP, YP, XN, YN pins		-50	-	50	μA

SWITCHING CHARACTERISTICS

Ta = -40°C to 85°C, AVDD = 2.5V to 3.6V, IOVDD = 1.6V to AVDD, CL = 20pF

Parameter	Symbol	min	typ	max	Units
Internal oscillator frequency	fosc	0.9	1.3	1.7	MHz
Touch Panel (A/D Converter)					
SCLK period	tCP	200	-	1000	ns
Sampling Time (Rin = 600Ω)	tSam	1.5	-	-	µs
Throughput Rate	fs	-	-	125	KHz
Conversion Time	tCONV	24	-	-	tCP
Timing Characteristics					
SCLK Pulse Width Low	tCKL	80	-	-	ns
Pulse Width High	tCKH	80	-	-	ns
CSN "↓" to First SCLK "↓"	tCSS	300	-	-	ns
CSN "↓" to DOUT Tri-State Disabled	tDV	-	-	50	ns
Data Setup Time	tDS	40	-	-	ns
Data Hold Time	tDH	40	-	-	ns
Data Output Delay after SCLK"↓"	tDD	-	-	50	ns
CSN "↑" to DOUT Hi-Z state	tCDZ	-	-	70	ns
CSN "H" Time	tCSW	150	-	-	ns
SCLK "↑" to CSN "↑"	tCSH	50	-	-	ns
Reset Timing					
RESETN Pulse Width (Note 5)	tRST	20	-	-	µs

Note 5. Device is reset by pull RESETN pin to "L".

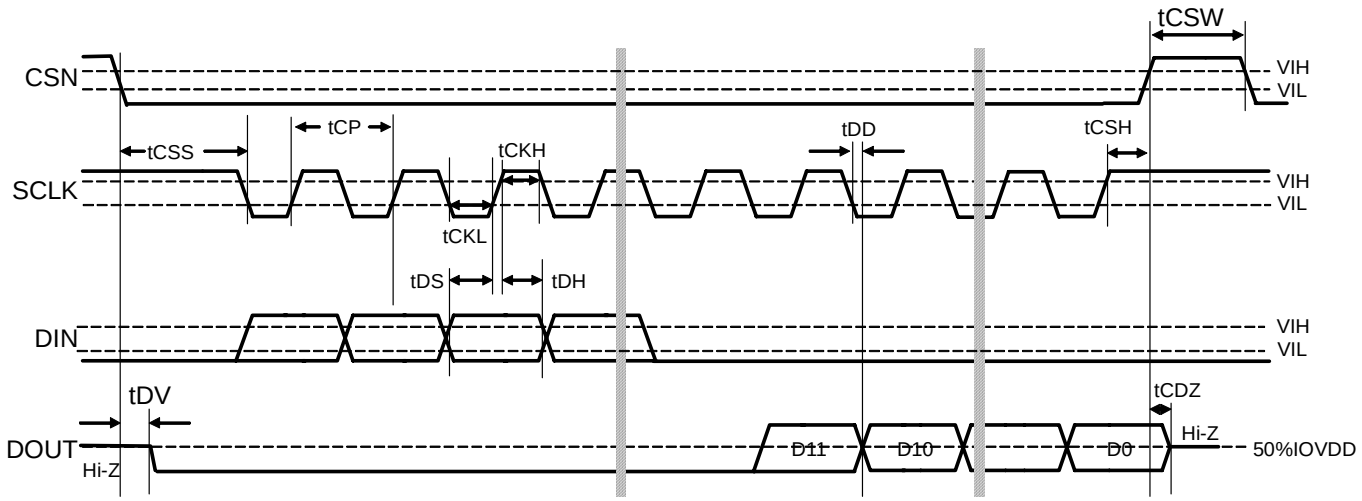


Figure 2. Timing Diagram

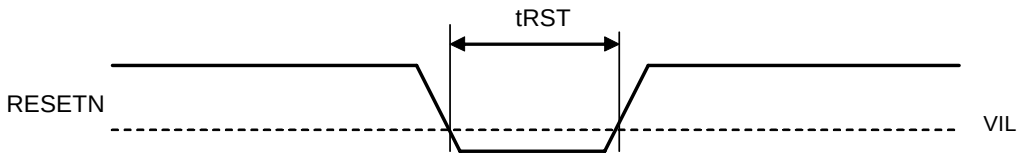


Figure 3. Power-down & Reset Timing

OPERATION OVERVIEW

The AK4184A consists of the following blocks:
- 4-wire resistive touch screen controller interface
- 6 columns by 5 rows keypad interface
- 8 GPIO pins
- PWM control circuit for LED bias control
- Successive approximation resister (SAR) A/D converter
- Pen interrupt and key interrupt circuit
- Oscillation circuit

AK4184A interfaces to the host processor through standard SPI™ serial interface.
SPI™ is the trademark of Motorola.

■ Touch Screen A/D Converter

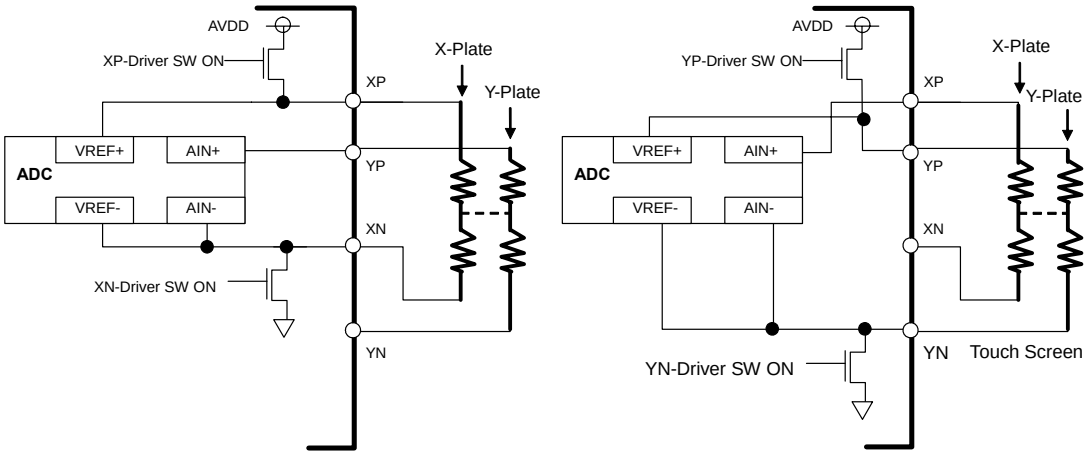
The AK4184A incorporates a 12-bit successive approximation resistor (SAR) A/D converter for determining the touch position and pressure measurement. The architecture is based on a capacitive redistribution algorithm, and an internal capacitor array functions as the sample/hold (S/H) circuit. The SAR A/D converter output is in straight binary format as shown below:

Input Voltage	Output Code
(ΔVREF - 1.5LSB) ~ ΔVREF	FFFH
(ΔVREF - 2.5LSB) ~ (ΔVREF - 1.5LSB)	FFEH
---------	---------
0.5LSB ~ 1.5LSB	001H
0 ~ 0.5LSB	000H

ΔVREF: (VREF+) – (VREF-)
Table 1. Output Code

■ Touch Screen Position Detection

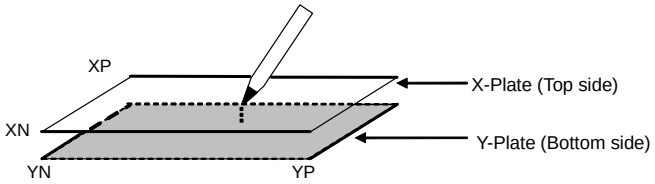
XY-coordinate detection (XY-position) from the touch panel is determined by the control command (A1, A0) bits of the touch screen control command. Coordinate detection is in differential mode. The full scale (ΔVREF) is the differential voltage between the non-inverting terminal and the inverting terminal of the measured axis (e.g. X-axis measurement: $\Delta VREF = V_{XP} - V_{XN}$). The input (ΔAIN) of the A/D converter is the voltage between the non-inverting terminal (V_{XP}) of the non-target axis and the inverting terminal (V_{XN}) of the target axis. (E.g. ΔAIN = (AIN+) - (AIN-) = $V_{YP} - V_{XN}$) The input voltage charges the internal capacitor during the sampling time period. No current flows into the internal capacitors after the capacitor has been fully charged. The required settling time to charge the internal capacitor array needs at least 1.5µs. The maximum throughput of the A/D converter is 125kHz. The position from the touch screen is detected by taking the voltage of one axis when the voltage is supplied between the two terminals of another axis. At least two A/D conversions are needed to get the two-dimensional (X/Y axis) position.



a) X-Position Measurement Differential Mode

b) Y-Position Measurement Differential Mode

The X-Plate and Y-plate are connected on the dotted line when the panel is touched.



c) 4-wire Touch Screen

Figure 4. Axis Measurement

■ Pen Pressure Measurement

Touch screen pen pressure can be derived from the measurement of the contact resistor between two plates. The contact resistance depends on the size of the depressed area and the pressure. The area of the spot is proportional to the contact resistance. This resistance (Rtouch) can be calculated using two different methods.
The first method is when the total resistance of the X-plate sheet is already known. The resistance, Rtouch, is calculated from the results of three A/D conversions: X-position, Z1-Position, and Z2-Position, using the following formula:

Rtouch = (Rxplate) * (Xposition/4096) * [(Z2/Z1) – 1]

The second method is when both the resistances of the X-plate and Y-plate are known. The resistance, Rtouch, is calculated from the results of three A/D conversions: X-position, Y-Position, and Z1-Position, using the following formula:

Rtouch = (Rxplate * Xposition/4096) * [(4096/Z1) – 1] – Ryplate * [1 – (Yposition/4096)]

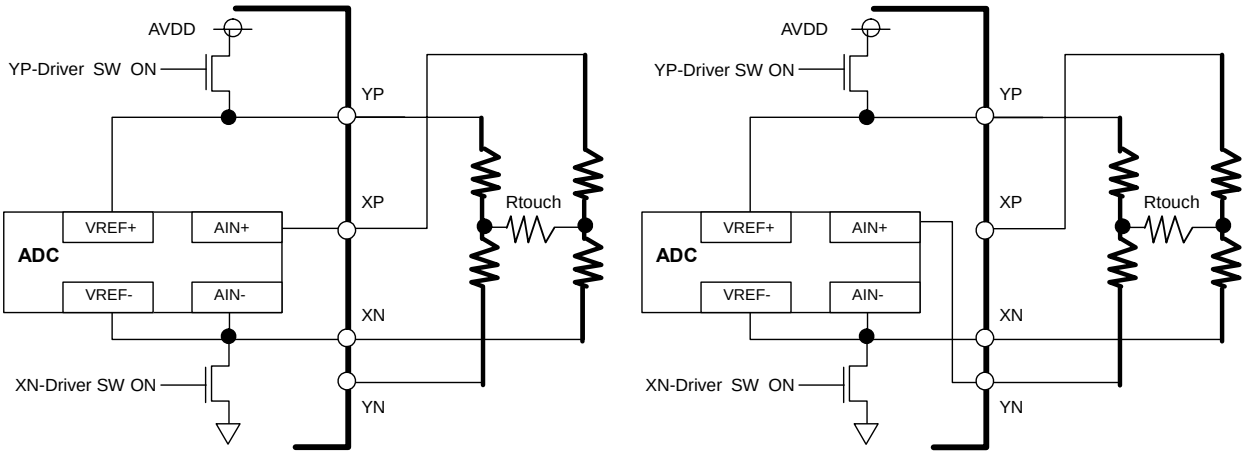


Figure 5. Pen Pressure Measurements

■ Keypad Scanner

The AK4184A keypad scanner is designed to interface to a matrix type keypad with 5 rows x 6 columns (30keys or fewer) to the host controller. The KPMASK1, 2 and KPColumnMask register enable the masking of certain keys or a whole column of the keypad when any keys less than 30 keys or any columns less than 6 columns are not utilized.

■ Keypad Interrupt Detection

When the AK4184A is in key interrupt enabled mode, C1 ~ C6 pins are designed to output "H" and R1 ~ R5 pins are designed to pull to GND via Rkey (Rkey=16kΩ typ, Figure 5). When a key is pressed a related R1 ~ R5 pins go to "H" and the KEYIRQN pin goes "L". The KEYIRQN pin returns "H" after key press scan is completed. The KEYIRQN pin does not go "L" again until the host reads the keypad read register (KPDATA1 or KPDATA2).

■ Keypad Scan Data Read

The AK4184A starts scanning key condition in sequence and writes each keypad state to the registers after a key-press is detected. First the C1 pin goes to "H" (Scan Output1) and the C2 ~ C6 pins are in Hi-Z state. Certain R1 ~ R5 pins are connected to C1 and pulled "H". The R1 ~ R5 pins return to "L" after the key-press is released. The AK4184A reads R1 ~ R5 pins level (Sense Input 1 through 5) and loads the keypad data into the register. When two keys are pressed simultaneously, the associated row pins go "H" at the same time. Then the AK4184A C2 pin goes to "H" (Scan Output2), and reads and loads the R1 ~ R5 pin levels into the register (Sense Input 1 through 5). The same sequence as Scan Output 1 repeats up to Scan Output 6. The AK4184A makes this Scan Output and Sense Input pattern and loads the keypad-data into the register for unmasked columns.
Debounce key scan performs a series of the Scan Output/ Sense Input at the end of the debounce time interval, then the AK4184A loads the key pad data into the resister. µ-Processor starts to read the data register after confirming if the keypad scan completed. New keypad scan does not repeat again until the Host reads the keypad data.

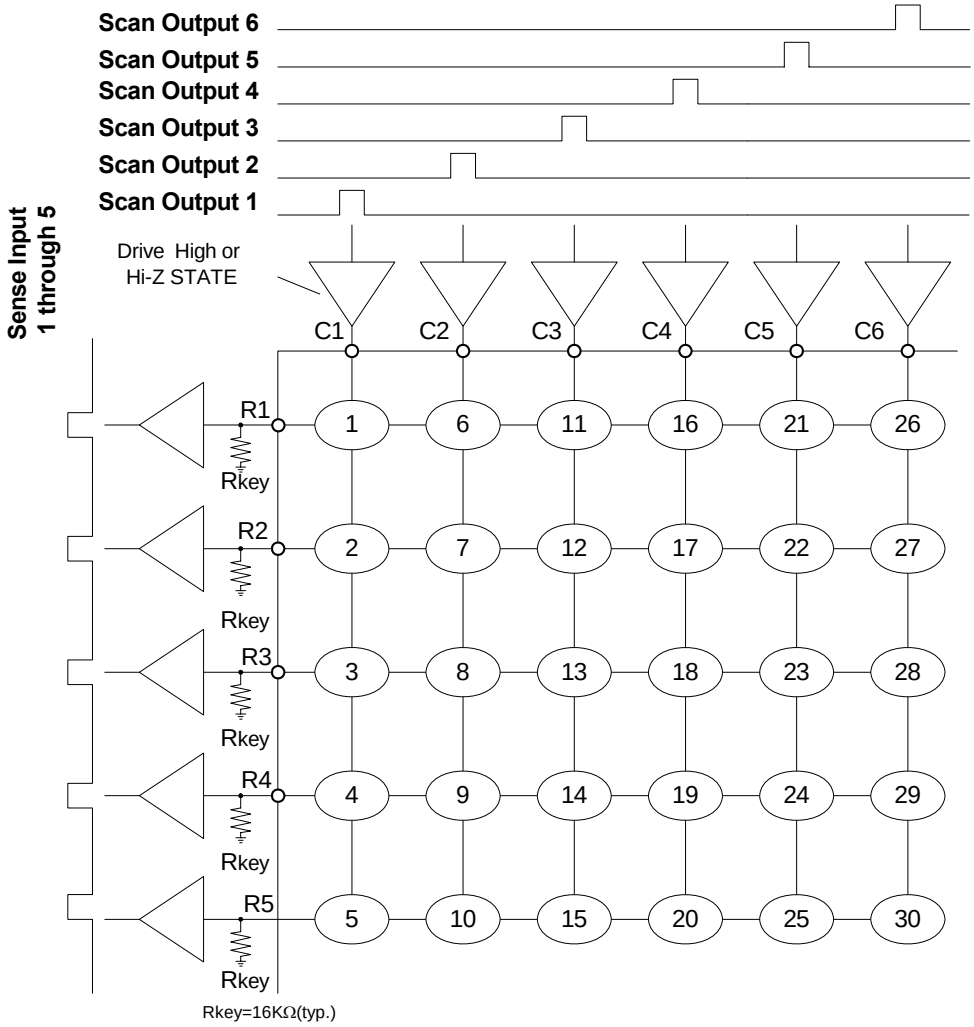


Figure 6. Key Press Detection Circuitry and KEY Number

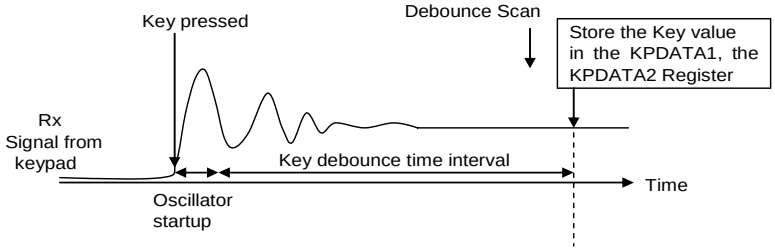


Figure 7. Debounce Time Interval

■ Digital Interface

The AK4184A supports a SPI bus system. The Host processor starts to communicate with the serial clock. The digital interface can be operated from 1.6V, which enables connecting with a low voltage host controller. The full scale level of the digital I/O voltage is specified IOVDD.

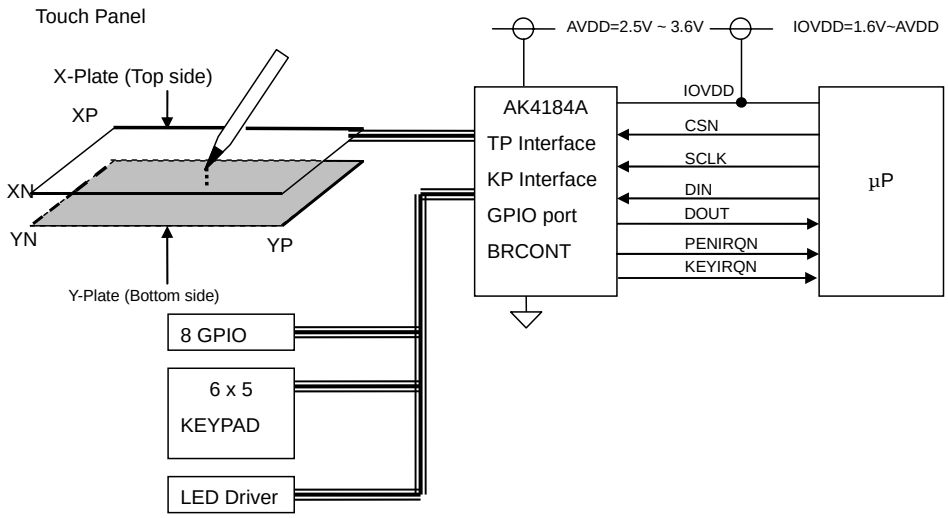


Figure 8. Typical peripheral connection diagram

The AK4184A is controlled by reading from and writing to registers through the 4-wire serial interface (CSN, SCLK, DIN, and DOUT pins). The data is composed of control command, control data, and readout data. The transmitter sends each bit on the falling edge of the SCLK pin and the receiver latches on the rising edge of SCLK. The first 16 bits after the falling edge of the CSN pin contains the control command followed by 16 bits of control data during the write operation, or 16 bits of readout data during the read operation before the rising edge of the CSN. This completes a write or read operation. The max clock speed of the SCLK pin is 5MHz. The register value is reset by pulling RESETN pin to "L".
The control command layout is shown in Table 2. The upper 8-bit word is the touch screen control command. The next lower 8-bits [D7:D0] are filled with "0" when accessing the touch screen block. The lower 8 bit word is composed of other block control commands, which specify control of the Keypad, GPIO, and PWM output. When accessing touch panel functions, the lower 8-bit word [D7:D0] is filled with "0" data. When accessing Keypad, GPIO, or PWM control, the upper 8-bit word [D15:D8] is filled with "0" data.
This command begins with the S bit which specifies access to the touch screen block. The S bit must be set to "1". The touch screen command begins with the A1:A0 bits, which select the measurement axis (X, Y, and Z). The PD bit specifies power down control of the touch screen driver and the A/D converter. When controlling other blocks, the first bit is a W/R bit, which specifies the direction of data flow on the bus. The next bit specifies the page bit of the register, which is the data register and the control register as shown in Table 3. The data of the next 6 bits are the address specified in the register. The page and address of the register is shown in Table 4. The next 16 bits are data that are read from or written to the register in Table 4. 32 SCLK cycles are necessary for both read and write operations.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Touch Screen Control Command Byte								**Other(Keypad, GPIO, LCD bias) Control Command Byte**							
S MSB	A1	A0	PD	x	x	x	x	W/R	PAGE	ADDR[5:0]					LSB

Table 2. Control Command (x: don't care)

PAGE	Description
0	Data Register
1	Control Register

Table 3. Page Address

PAGE	Addr	Register Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	00H	KPDATA1	DERR	KD3[4]	KD3[3]	KD3[2]	KD3[1]	KD3[0]	KD2[4]	KD2[3]	KD2[2]	KD2[1]	KD2[0]	KD1[4]	KD1[3]	KD1[2]	KD1[1]	KD1[0]
0	01H	KPDATA2	SERR	KS2[4]	KS2[3]	KS3[2]	KS3[1]	KS3[0]	KS2[4]	KS2[3]	KS2[2]	KS2[1]	KS2[0]	KS1[4]	KS1[3]	KS1[2]	KS1[1]	KS1[0]
0	02H -FH	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	10H	GPLR	0	0	0	0	0	0	0	0	GPD7	GPD6	GPD5	GPD4	GPD3	GPD2	GPD1	GPD0
0	11H-3FH	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	00H	KEY	KST1	KST0	DBN2	DBN1	DBN0	HLD2	HLD1	HLD0	0	0	0	0	0	0	0	0
1	01H	KPMASK1	0	KM15	KM14	KM13	KM12	KM11	KM10	KM9	KM8	KM7	KM6	KM5	KM4	KM3	KM2	KM1
1	02H	KPMASK2	0	KM30	KM29	KM28	KM27	KM26	KM25	KM24	KM23	KM22	KM21	KM20	KM19	KM18	KM17	KM16
1	03H	KPColumnMask	0	0	0	0	0	0	0	0	0	0	CM6	CM5	CM4	CM3	CM2	CM1
1	04H	KPScanInitiate	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	05H-07H	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	08H	PDCTRL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	KPPD	TPPD
1	09H-0FH	reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	10H	GPSCR	0	0	0	0	0	0	0	0	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0
1	11H	GPDR	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	0	0	0	0	0	0	0	0
1	12H	GPPU	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0	0	0	0	0	0	0	0
1	13H	GPSR	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	0	0	0	0	0	0	0	0
1	14H-17H	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
1	18H	PWMCTL	LPU	0	0	BRV[4]	BRV[3]	BRV[2]	BRV[1]	BRV[0]	0	PACT	0	0	0	DIV2	DIV1	DIV0
1	19H-3FH	Reserved	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 4. AK4184A Register Map

■ System Reset

Upon power-up, all blocks of the AK4184A must be reset by the RESETN pin = "L". This ensures that all internal registers are reset to their initial values (0000H). The touch screen control data is set to X-measurement and auto driver off (A1 bit=A0 bit = PD bit="0"). Internal state is fixed and the pen interrupt function is enabled. If the AVDD and IOVDD are supplied separately, the power up sequence is not critical.

■ Touch Screen Control Command

The control command (4 bits) provided to the AK4184A via DIN is shown in Table 5. This command includes a start bit, channel selection of ADC input, power-down mode of ADC and the next 12bits (written by "0" data). The AK4184A latches the serial command on the rising edge of SCLK. Detail information regarding the bit order, function, status of the driver switch, ADC input and reference voltage are shown in Table 6 and Table 7.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
S	A1	A0	PD	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Touch Screen Command Word Format

Bits	Name	Function
15	S	Start Bit. This bit must be "1"
14:13	A1-A0	Channel Selection Bits. Analog inputs to the A/D converter and the activated driver switches are selected. (Table 7)
12	PD	Power-down Mode (Table 8)
11:0		Reserved

Table 6. The definition of touch screen control data

	Input		Status of Driver Switch				ADC input (ΔAIN)		Reference Voltage (ΔVREF)		
S	A1	A0	XP	XN	YP	YN	AIN+	AIN-	VREF+	VREF-	Note
1	0	0	ON	ON	OFF	OFF	YP	XN	XP	XN	X-axis
1	0	1	OFF	OFF	ON	ON	XP	YN	YP	YN	Y-axis
1	1	0	OFF	ON	ON	OFF	XP(Z1)	XN	YP	XN	Z1 (Pen Pressure)
1	1	1	OFF	ON	ON	OFF	YN(Z2)	XN	YP	XN	Z2 (Pen Pressure)

Table 7. Status of Driver Switch

■ Power-down Control

The power-down state of A/D converter and the touch screen driver switches is controlled by the PD bit.

PD	PENIRQN	Function
0	Enabled	Auto Driver Power Off Mode. When PD bit is "0", the touch screen driver switches and the A/D converter are automatically powered up at the start of sampling, and moves to power- down state automatically at the rising edge of CSN. The AK4184A is always powered down when CSN is "H". All touch screen driver switches except for the YN switch are turned off, and relative pins are in open state. Only the YN driver switch is turned ON, and the YN pin is forced to ground. The pen interrupt function is enabled except when CSN is "L". See "■ Pen Interrupt" for detail.
1	Disabled	ADC ON Mode When PD bit is "1", the touch screen driver switches and the A/D converter are always turned ON. The pen interrupt function is disabled and the PENIRQN pin is always "H", regardless of the pen touch. The touch panel driver turns on before sampling time starts so that the touch panel voltage fed into A/D converter is stable in this mode. The sampling time starts at the falling edge of CSN this is effective if more settling time is required to suppress the electrical bouncing of touch plate.

Table 8. Power-down Control

A/D converter is power-down both when the CSN pin is "H" and controlling with keypad scanner, GPIO block, PWM controller.
A/D converter is power-up when issues touch panel command at the CSN pin is "L".

■ Touch Screen Control Sequence

The timing of sampling and A/D conversion is shown in Figure 8. The AK4184A is controlled through a standard SPI serial interface (CSN, SCLK, DIN, and DOUT pins). BUSY and DOUT are in Hi-Z state when CSN = "H". The AK4184A latches the 4-bit control word serially via DIN on the rising edge of SCLK. DIN must be low until CSN is "H". The S bit must be "1".

The sampling (Sampling1 or Sampling2) time for the A/D converter depends on the PD bit. The SAR-A/D conversion is synchronized with SCLK. The A/D conversion occurs between the falling edge of the sixth SCLK and the 20th SCLK, followed by a 12-bit serial data output. Sampling time is determined by the PD bit.

If a series of the measurements are the same and the previous PD bit is "0", sampling occurs between the falling edge of the third SCLK and the sixth SCLK (Sampling2). When the previous PD bit is "1", sampling occurs between the falling edge of CSN to the falling edge of the sixth SCLK (Sampling1+Sampling2). This is a longer sampling time.

If the measurements switch to another axis, the measurement axis is determined by the current setting of the [A1, A0] bits, irrespective of the PD bit setting. Even through the previous PD bit is "1", the valid sampling time is Sampling2 as shown in Figure 9.

Sampling time depends on SCLK and the source impedance. When the A/D input voltage does not reach the final voltage during Sampling2, continue to measure the same axis with the PD bit = "1" or use a slower SCLK in order to increase the settling time.

The BUSY pin stays "H" from beginning of the A/D conversion to the beginning of MSV data output (20th falling edge of SCLK). BUSY is "L" for the other period. The AK4184A outputs A/D data with MSB first via DOUT from the rising edge of the 21st SCLK.

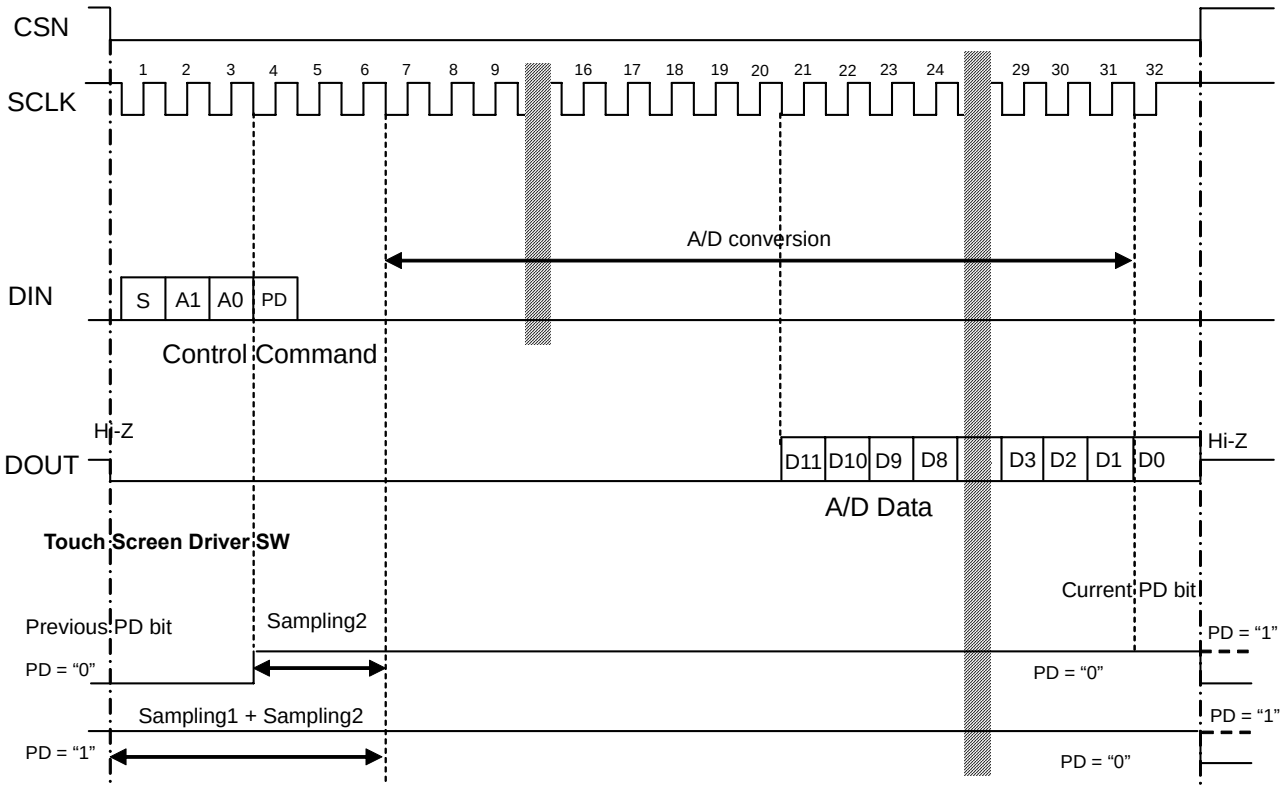


Figure 9. Touch Screen Operation

■ Pen Interrupt

The AK4184A has a pen interrupt function to detect a pen touch. The pen interrupt function is enabled during power-down state. The YN pin is connected to GND during the pen interrupt enabled state. The XP pin is pulled up via an internal resistor (Ri), typically 50kΩ. If the touch plate is pressed by a pen, the current flows via <AVDD> - <Ri> - <XP> - <the plates> - <YN>- <GND>. The resistance of the plate is generally several hundreds, and PENIRQN pin is forced to a "L" level. If the pen is released, the PENIRQN pin returns to a "H" level because two plates are disconnected, and the current doesn't flow between the two plates. The PENIRQN pin is a buffer type. The "H" level is specified by IOVDD.
The operation of PENIRQN is related to PD bit. The pen interrupt function is disabled and stays "H" irrespective of the pen touch when the PD bit is "1". When the PD bit is "0", the PENIRQN pin is forced "H" from the falling edge of the sixth SCLK to the rising edge of CSN. The pen interrupt function is valid when the CSN pin is "H". The PENIRQN pin stays low when the touch panel is pressed, and stays high when the touch panel is not pressed.
The pen interrupt function is determined by the present PD bit setting when the host writes to or reads from the register other than the pen touch block.

The touch panel block is able to power down when the TPPD bit is "1" (Table 25). All the touch panel drivers turn off in this state and the pen interrupt function is not valid. The current through the touch screen does not flow even through the panel is pressed.

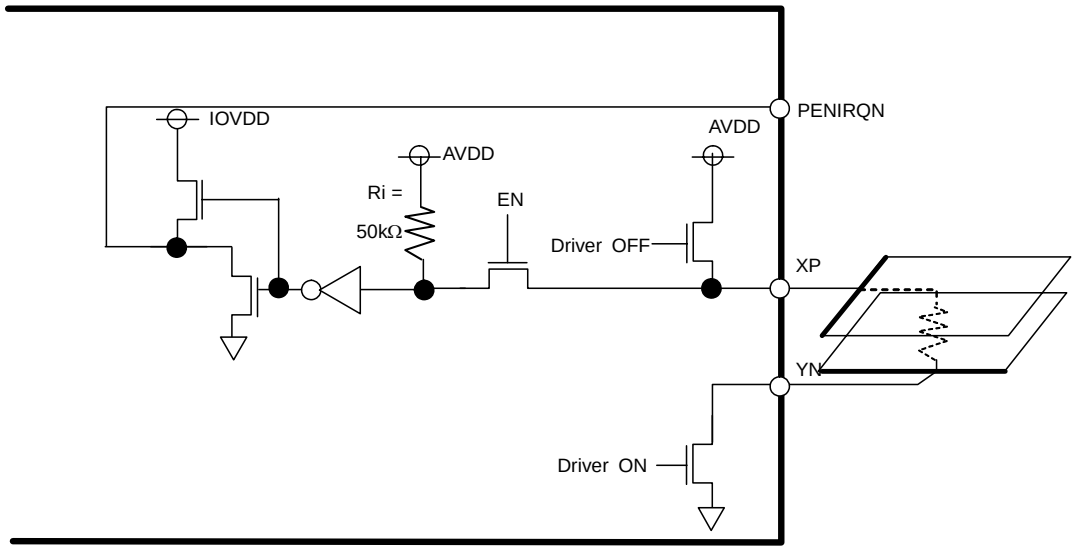


Figure 10. PENIRQ Functional Block Diagram

■ Keypad, GPIO, LED Contrast Control

The control command format for accessing the keypad scanner, GPIO, and LED contrast control is described in Table 10. The sequence of writing to and reading from the registers is shown in Table 12, Table 13. The upper MSB byte (touch screen command) of the control command is set to zero when assessing these blocks. Refer to Table 4 for the control and read data formats.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	W/R	PAGE	ADDR[5:0]					

Table 9. Keypad, GPIO, LED Contrast Control Command Format

Bits	Name	Description
7	W/R	Write/Read bit 0: Write 1: Read
6	PAGE	Page bit (Table 3)
5:0	ADDR	Address bit (Table 4)

Table 10. Control Command

1. Write Operation

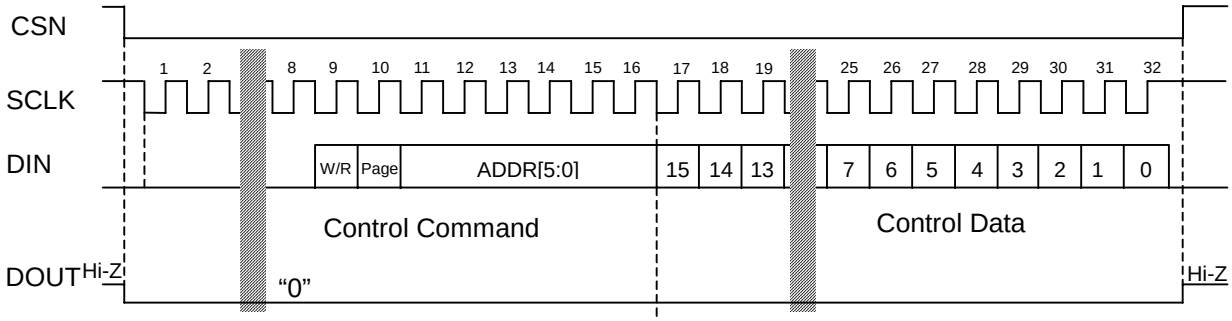


Figure 11. Write Operation

2. Read Operation

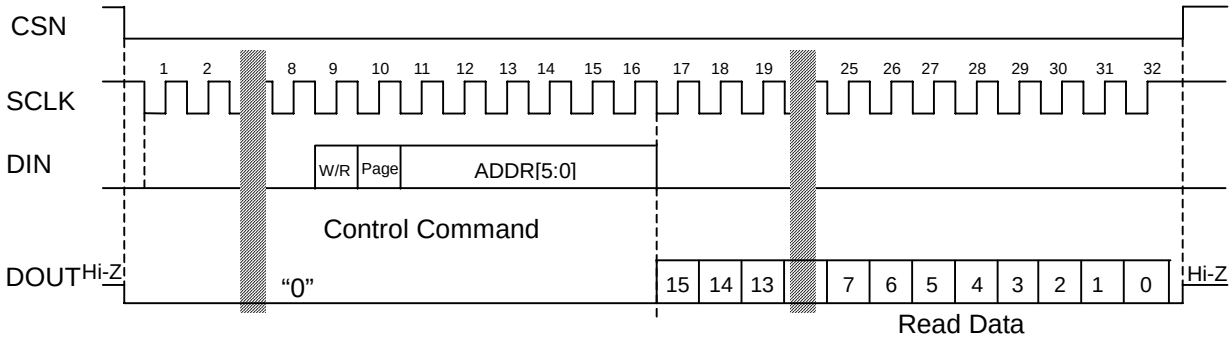


Figure 12. Read Operation

■ Keypad Scanner

The AK4184A has a keypad interface which supports maximum Keypad matrix of six columns by five rows.

■ Keypad Measurement Mode

Setting the KST1 bit = "0" (default) enables the AK4184A to monitor key-press detection and move to key pad measurement mode after keypad detection. The AK4184A provides two different keypad measurement modes by setting the KST0 bit: host scan mode and key press scan mode.

■ Host Scan Mode

When the KST0 bit is "1" the mode is host scan mode, pressing the keypad down makes the AK4184A outputs a keypad interrupt signal (KEYIRQN pin goes low), and then the AK4184A move to the state which waits for a KPScanInitiate (Page1, Address 04H) command from host. The internal oscillator turns off until receiving this command, and the AK4184A does not execute key scan. Keypad scan begin when receiving a KPScanInitiate command. Once receiving this command, the AK4184A turns on the internal oscillator and starts keypad debounce scan.

■ Key press Scan Mode

When the KST0 bit is "0" key press scan mode is enabled. Pressing the keypad down causes the AK4184A to output a keypad interrupt signal (KEYIRQN pin goes low) and the AK4184A starts a keypad debounce scan automatically.

The keypad data register (KPDATA1, KPDATA2) is revised after completing a debounce scan. The KEYIQRN pin goes to "H" and the AK4184A goes to hold state. Key press detect function is disabled during the hold time. When the host processor reads the keypad data register during hold time, the hold time counter is reset and restarted after being read by the host processor. Key press detection is not valid until the host processor reads the keypad data register after hold time is passed. Reading a keypad date is determined by accessing KPDATA1, KPDATA2 register. Reading the KPDATA1 or KPDATA2 registers is required when key press interrupts of the AK4184A become valid. The hold time and the debounce time are controlled through the keypad control register (KEY).

Keypad Debounce Scan initiated by Host (Initial : KST1 bit="0", KST0 bit="1")

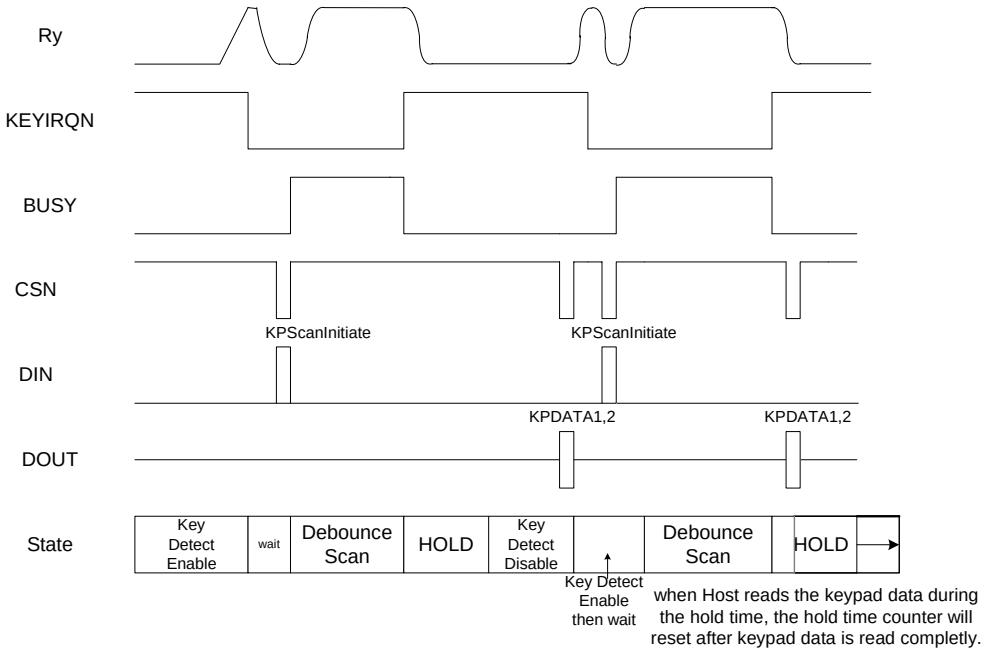


Figure 13. Timing Diagram for keypad debounce scan initiated by Host
(Initial: key interrupt enable, wait for Host instruction)

Keypad Debounce Scan initiated by keypad activity (Initial : KST1 bit="0", KST0 bit="0")

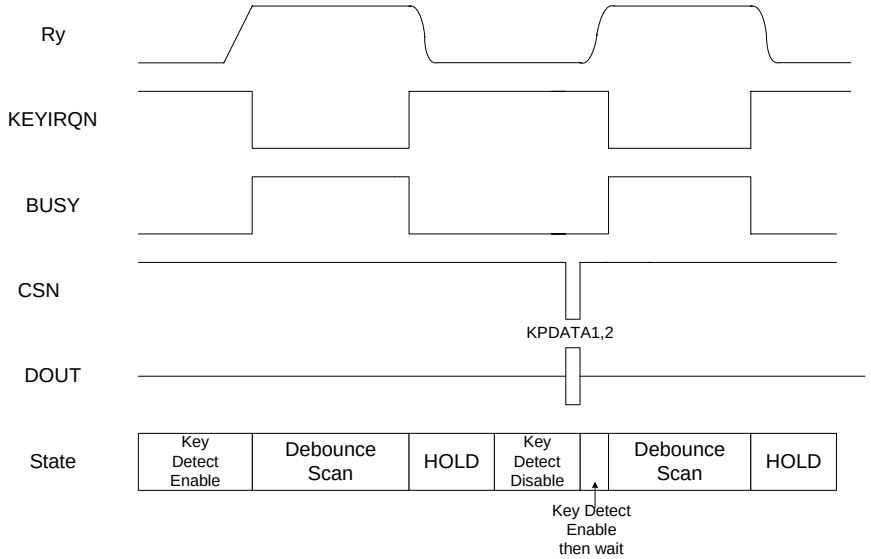


Figure 14. Keypad Debounce Scan initiated by key activity
(Key interrupt enable, key scan initiated by key touch)

■ Keypad Control Register (PAGE 1)

The keypad scanner controller is controlled by the Keypad Control register (Table 12), Keypad Mask register (Table 17) and Keypad Column register (Table 19). This register controls the key press interrupt (host scan mode or key-press scan mode), key-press debounce time interval and hold time. The Keypad Mask register is valid for each key masked after debounce key scan. The Keypad Column Mask register stops a key scan of a selected key column and is disabled for the detection of key press.

Addr	NAME	D15 MSB	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 LSB
00H	KEY	KST1	KST0	DBN[2:0]			HLD[2:0]			0	0	0	0	0	0	0	0

Table 11. Keypad Control Register Format

Bits	Name	Description
15	KST1	Key Interrupt enable signal 0 : enable 1 : disable
14	KST0	Key scan initiated by Host/Key 0 : scan starts by key-press 1 : scan starts by Host command
13:11	DBN	Keypad debounce time interval
10:8	HLD	Keypad hold time control
7:0		Reserved

Table 12. Keypad Control Register (Write)

The KST1 and KST0 bits can be read to determine the state of keypad scanner. The KST1 and KST0 bits and their descriptions are described in Table 13.

KST1	KST0	Description
0	0	Keypad Debounce scan is busy.
0	1	Wait for the command initiated by Host
1	0	No detect
1	1	Data available

Table 13. KST bit (Read)

The keypad debounce time interval is determined by [DBN2:DBN0]. The default setting is 1ms.

DBN2	DBN1	DBN0	Function
0	0	0	Debounce time: 1ms (default)
0	0	1	Debounce time: 2ms
0	1	0	Debounce time: 5ms
0	1	1	Debounce time: 10ms
1	0	0	Debounce time: 20ms
1	0	1	Debounce time: 50ms
1	1	0	Debounce time: 80ms
1	1	1	Debounce time: 100ms

Table 14. Keypad Debounce Time Interval

The keypad hold time is determined by [HLD2:HLD0]. The default setting is 100μs.

HLD2	HLD1	HLD0	Function
0	0	0	Wait 100μs for next Debounce scan (default)
0	0	1	Wait 1 debounce time interval to the next debounce scan
0	1	0	Wait 2 debounce time interval to the next debounce scan
0	1	1	Wait 3 debounce time interval to the next debounce scan
1	0	0	Wait 4 debounce time interval to the next debounce scan
1	0	1	Wait 5 debounce time interval to the next debounce scan
1	1	0	Wait 6 debounce time interval to the next debounce scan
1	1	1	Wait 7 debounce time interval to the next debounce scan

Table 15. Keypad Hold Time Control

■ Keypad Mask Register (PAGE 1)

This register controls the key to be masked after a debounce key scan. The keypad mask register format is described in the following table. This register setting is valid for the data in the KPDATA2 register.

Addr	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
01H	KPMASK1	0	KM15	KM14	KM13	KM12	KM11	KM10	KM9	KM8	KM7	KM6	KM5	KM4	KM3	KM2	KM1
02H	KPMASK2	0	KM30	KM29	KM28	KM27	KM26	KM25	KM24	KM23	KM22	KM21	KM20	KM19	KM18	KM17	KM16

Table 16. Keypad Mark Register Format

KMx	Description
0	Disable keypad data masked (default)
1	Enable keypad data masked

Table 17. Keypad Mask bit

The number of the keypad corresponds to each bit of this register .This relationship is shown in Table 24. KPMASK1, KPMASK2 default setting is 0000H (disable keypad data masked on KPDATA2)

■ Keypad Column Mask Register (PAGE 1)

The Keypad Column Mask Register format is shown in Table 19. This register allows a certain column to be masked from keypad detection.

Addr	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
03H	KPColumnMASK	0	0	0	0	0	0	0	0	0	0	CM6	CM5	CM4	CM3	CM2	CM1

Table 18. Keypad Column Mask Register Format

CMx	Description
0	Enable key press detection for a certain column pin (default)
1	Disable key press detection for a certain column pin

Table 19. Keypad Column Mask bit

■ Keypad Scan Initiate Command (PAGE 1)

When a key is pressed with the KST0 bit = "1", the AK4184A does not start debounce and key scan, the Host Controller sends a keypad scan initiate command to the AK4184A. After receiving the command, the AK4184A starts a debounce scan, and the Host Controller can then read the data [D15:D0] from the keypad data register (KPDATA1, KPDATA2). When receiving the command the Keypad Data Resister (KPDATA1, KPDATA2) is reset to 0000H.

Addr	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
04H	KPScanInitiate	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X

Table 20. Keypad Scan Initiate Command Format

■ Keypad Data Register (PAGE 0)

The keypad data register format is shown below. KD1, KD2, KD3, KS1, KS2 and KS3 represent the number of keys pressed. Table 24 shows a configuration of a 30-key keypad. Data of KD1, KD2, KD3, KS1, KS2 and KS3 returned as zero represents no key pressed. The AK4184A keypad scanner can be read out up to three keys simultaneously. The AK4184A key pad scanner writes the number of keys pressed in the keypad data register. For example: When two keys are pressed at the same time, the contents of the keypad register are filled with KD1, KD2, KS1, and KS2. KD3 and KS3 are the zero data. When more than four keys are pressed at the same time, error bits (DERR bit and SERR bit) are set to "1" and KD1, KD2, KD3, KS1, KS2, and KS3 data are set to 31.

The keypad data can be read out either from the KPDATA1 register or the KPDATA2 register. The KPDATA1 register represents the keypad data masked by the keypad column mask register. KPDATA2 register represents the keypad data masked by both the keypad column mask register and the keypad mask register. KPDATA1 and KPDATA2 register are cleared after these resisters are read.

Addr	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00H	KPDATA1	DERR	KD3[4:0]					KD2[4:0]					KD1[4:0]				
01H	KPDATA2	SERR	KS3[4:0]					KS2[4:0]					KS1[4:0]				

Table 21. Keypad Data Register Format

Bits	Name	Description
15	DERR	Keypad scan data error
14:10	KD3	Keypad scan result 3. can be masked by column mask
9:5	KD2	Keypad scan result 2. can be masked by column mask
4:0	KD1	Keypad scan result 1. can be masked by column mask

Table 22. Keypad Data 1 Register (addr: 00H)

Bits	Name	Description
15	SERR	Keypad status data error
14:10	KS3	Keypad status result 3. can be masked by both keymask and column mask
9:5	KS2	Keypad status result 2. can be masked by both keymask and column mask
4:0	KS1	Keypad status result 1. can be masked by both keymask and column mask

Table 23. Keypad Data 2 Register (addr: 01H)

The corresponding number and its keypad layout are shown on Table 24.

	C1	C2	C3	C4	C5	C6
R1	#1	#6	#11	#16	#21	#26
R2	#2	#7	#12	#17	#22	#27
R3	#3	#8	#13	#18	#23	#28
R4	#4	#9	#14	#19	#24	#29
R5	#5	#10	#15	#20	#25	#30

Table 24. Keypad to Key number Mapping

■ GPIO controller

The AK4184A has eight ports [GP0:GP7] which can be configured as inputs or outputs for general purpose. Figure 15 shows a block diagram of a single GPIO pin. The GPIO Pin Direction register (GPDR) is used to program the GPIO pins as input or output. For a pin configured as output, use the GPIO pin pull-up register (GPPU) to set the pin type to either Open-Drain or CMOS, and use the GPIO Set/ Clear register (GPSCR) to set a pin level high or low.

To validate the state of GP0 ~ GP7 pins, write to the GPIO pin state register (GPSR) to program the pin state as pull-down or Hi-Z and read the GPIO Pin Level register (GPLR) at any time even if the pin is configured as an output. The GPIO pin state is determined by these registers before writing and reading the pin level.
The pin state set by default input, pull-down.

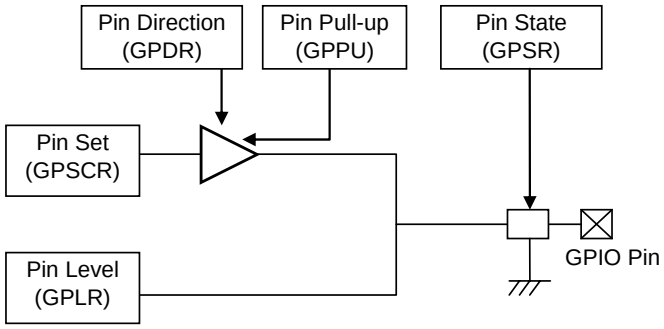


Figure 15. General-Purpose I/O Block Diagram

■ GPIO Pin Set/ Clear Register (PAGE 1)

The GPIO pin set/clear register sets the pin level when the pin is configured as an output (Table 28: IO bit = "1"). GPSCR is a write-only register. The actual pin level is read from the GPLR register.

Addr	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10H	GPSCR	0	0	0	0	0	0	0	0	SC7	SC6	SC5	SC4	SC3	SC2	SC1	SC0

Table 25. GPIO Pin Set/ Clear Register Format

Bits	Name	Description
15:8		Reserved
7:0	SC	Set GPIO Pin level for GPIO pins 0: Set pin level low (default) 1: Set pin level high

Table 26. GPIO Pin Set/Clear Register

■ GPIO Pin Direction Register (PAGE 1)

Whether a pin is input or an output is determined by the GPDR register. The GPDR contains one direction-control bit for each of the eight GPIO pins.

Addr	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
11H	GPDR	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0	0	0	0	0	0	0	0	0

Table 27. GPIO Pin Direction Register Format

Bits	Name	Description
15:8	IO	GPIO Direction select 0: GPIO pin configured as input. (default) 1: GPIO pin configured as output.
7:0		Reserved

Table 28. GPIO Direction Register

■ GPIO Pin Pull-up Register (PAGE 1)

The GPPU register determines the output pin type - either CMOS or Open drain. This register is valid for pins configured as outputs (IO bit = "1" in Table 28). Pull-up resistors on GP0 to GP7 pins must be connected to (IOVDD+0.3) V or lower voltage when the PUx bit is set to "1".

Addr	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
12H	GPPU	PU7	PU6	PU5	PU4	PU3	PU2	PU1	PU0	0	0	0	0	0	0	0	0

Table 29. GPIO Pin Pull-up Register Format

Bits	Name	Description
15:8	PU	GPIO Pullup register select 0: GPIO CMOS outputs (default) 1: GPIO Open drain outputs
7:0		Reserved

Table 30. GPIO Pull-up Register

■ GPIO Pin State Register (PAGE 1)

The GPSR register determines the state of pins which are either pull-down or Hi-Z. This register is valid for pins configured as inputs (IO bit = "0").

Addr	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
13H	GPSR	PS7	PS6	PS5	PS4	PS3	PS2	PS1	PS0	0	0	0	0	0	0	0	0

Table 31. GPIO Pin State Register Format

Bits	Name	Description
15:8	PS	GPIO Pin state select 0: GPIO Pull-down (Rgp=1MΩ typ.) state (default) 1: GPIO pin Hi-Z state
7:0		Reserved

Table 32. GPIO Pin state Register

■ GPIO Pin Level Register (PAGE 0)

The state of each GPIO pin can be determined by reading this register (GPLR). Each bit corresponds to one pin. Use the GPLR read-only registers to determine the current level of a certain pin irrespective of the programmed pin direction. The upper eight bits returns zero when read.

Addr	Name	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
10H	GPLR	0	0	0	0	0	0	0	0	GPD7	GPD6	GPD5	GPD4	GPD3	GPD2	GPD1	GPD0

Table 33. GPIO Pin Level Register Format

Bits	Name	Description
15:8	0	Reserved
7:0	GPD	GPIO Pin Level bits for GPIO pins 0: Pin state is low 1: Pin state is high

Table 34. GPIO Pin Level Register

■ LED contrast control

The AK4184A contains an oscillator and a PWM control circuit for controlling the brightness of an LED by modulating the "on" time. The brightness is determined by the PWM basic frequency (f_{pwm}) and duty cycles. The PWM block divides the internal oscillator frequency (fosc) and modulates this output. The range of PWM frequency (fpwm) is 80Hz minimum. The modulating range is provided by 32 duty cycle steps from the PWM logic controller. The output control is determined by the PACT bit. The duty cycle width of the PWM frequency is controlled by the BRV and DIV bits. The PWM signal stays constant on normal mode until duty cycle, PWM frequency changed.

The output type is possible to select either CMOS or Open Drain, set by the LPU bit. After reset, the PWM block is in power-down state and the BRCONT pin outputs a "L" level.

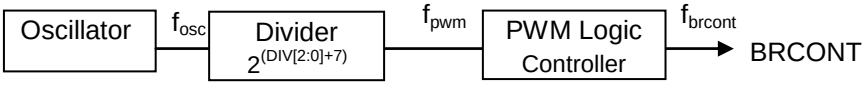


Figure 16. PWM output block

Example BRV [4:0] =11H setting

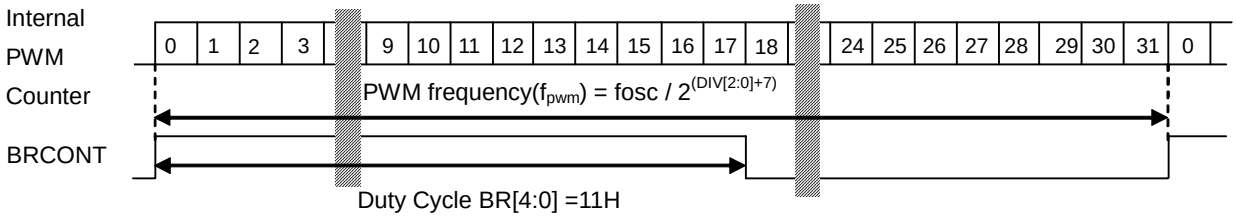


Figure 17. PWM output waveform

■ PWM Control Register (PAGE 1)

Addr	Name	D15 MSB	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 LSB
18H	PWMCTRL	LPU	0	0	BRV[4:0]					0	PACT	0	0	0	DIV[2:0]		

Table 35. PWM Control Register Format

Bits	Name	Description
15	LPU	Output type Open drain / CMOS 0: CMOS type (default) 1: Open Drain type
14:13		Reserved
12:8	BRV	Bright Control Value The period of "H" output level is (control value + 1) cycle in unit of (fpwm/32)
7		Reserved
6	PACT	Oscillator and PWM Logic Controller Power Up 0: Power Down State (default) 1: Normal mode (Oscillator power up and enable output)
5:3		Reserved
2:0	DIV	PWM clock divider index fpwm(typ.)=fosc/$2^{[DIV + 7]}$

Table 36. PWM Control Register

■ Power Down Register (PAGE 1)

The power down register determines the power down control of the keypad scanner block and touch screen block. The power down state in the touch screen block (TPPD bit = "1") holds all of the touch panel driver switches off, so that current cannot flow through the touch panel. The pen interrupt function is disabled and the PENIRQN pin always stays "H", effective for reducing power consumption of the touch screen block.

A power down state in the keypad scanner block (KPPD bit = "1") holds all the C1 ~ C6 pins outputs "L". By setting this bit = "1" stops key scanning and clears the keypad data register (KPDATA1, KPDATA2). The keypad function is restored after the keypad scanner block is powered up. The keypad interrupt is disabled at power-down.

The power down control register format is shown here.

Addr	NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
08H	PDCTRL	0	0	0	0	0	0	0	0	0	0	0	0	0	0	KPPD	TPPD

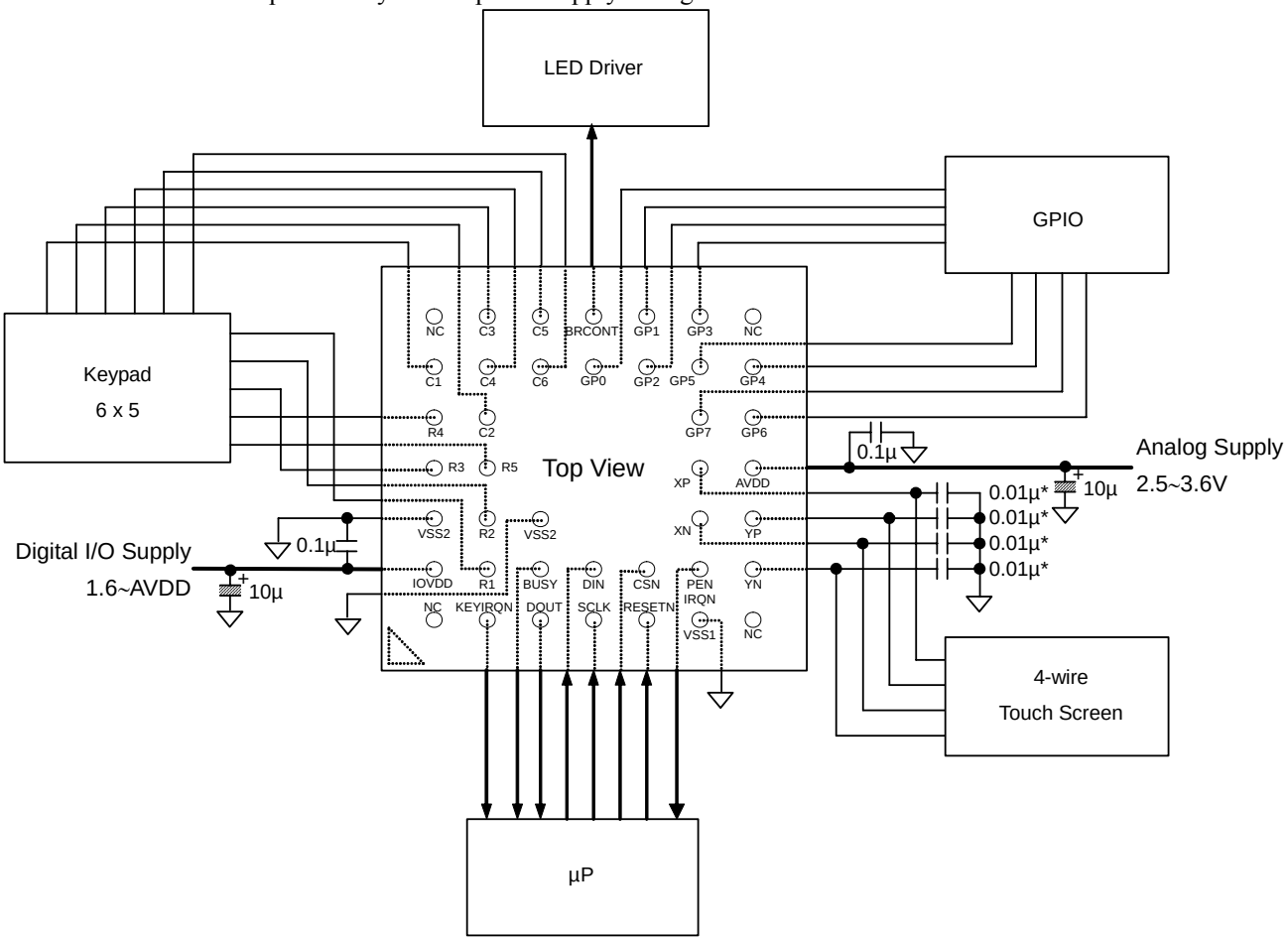
Table 37. Power Down Register Format

Bits	Name	Description
15:2		Reserved
1	KPPD	Enable keypad block power up/down 0: power up (default) 1: power down
0	TPPD	Enable the touch screen control block power up/down 0: power up (default) 1: power down

Table 38. Power Down Register

SYSTEM DESIGN

Figure 18 shows a system connection diagram for the AK4184A. The evaluation board [AKD4184A] is available, which demonstrates the optimum layout and power supply arrangement.



Note:
- VSS1 and VSS2 of the AK4184A must be distributed separately from the ground of external controllers.
- Do not allow digital input pins (CSN, SCLK, DIN pins) to float.
- The DOUT pin is floating except when communicating with the host processor. A 100kΩ pull-down or pull-up register must be connected.

Figure 18. Typical connection diagram

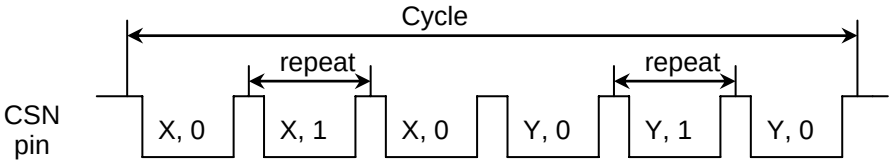
■ Attention to the PCB wiring

The AK4184A requires careful attention to power and grounding. VSS1, VSS2 must be connected to analog ground system analog ground and digital ground must be connected together as close as possible to where the supplies are brought onto the printed circuit board. Decoupling capacitors must be as close to the AK4184A as possible, with the small value ceramic capacitor being the closest.

When an EMI source is close to the touch panel analog signal line, EMI noise reduces analog performance characteristics. Noise canceling capacitors as close as possible to each pin (XP, XN, YP, YN pins) of the AK4184A should be connected to avoid this noise. (Figure 18) In addition, ESD protection devices should be mounted on the printed circuit board for countermeasure for surge and static electricity on the touch panel, GPIO and keypad signal lines.

CONTROL SEQUENCE

■ X-, Y- Coordinate measurements



X: X-measurement, Y: Y-measurement.
0: PD bit = "0" setting, 1: PD bit = "1" setting.

Figure 19. Timing Sequence for detecting X, Y position

■ Keypad Scanner Flowchart

1. Host Scan

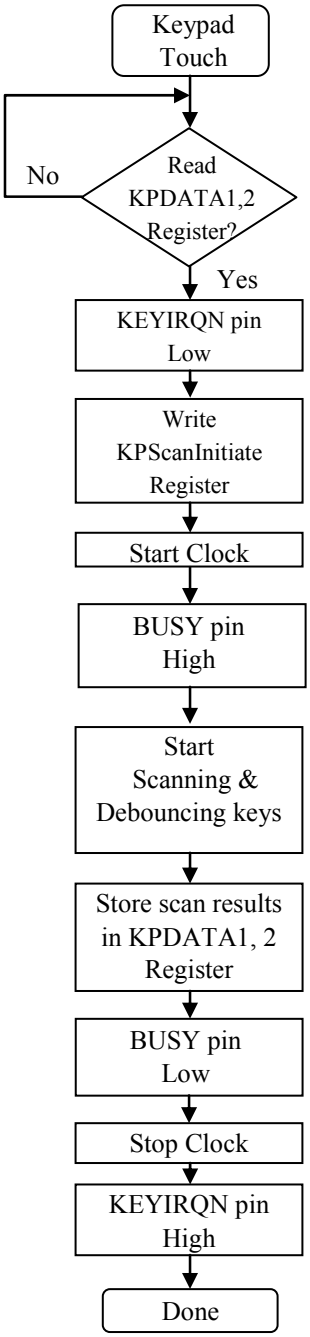


Figure 20. Keypad scanner sequence initiated by Host command

2. Keypress scan mode

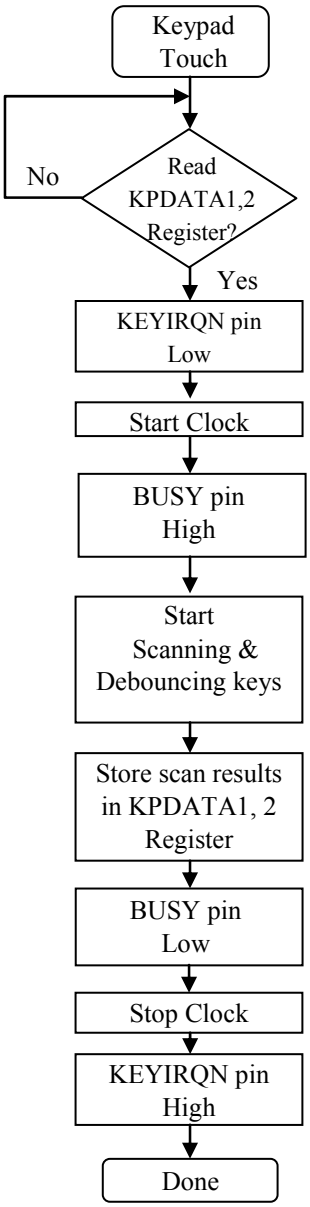
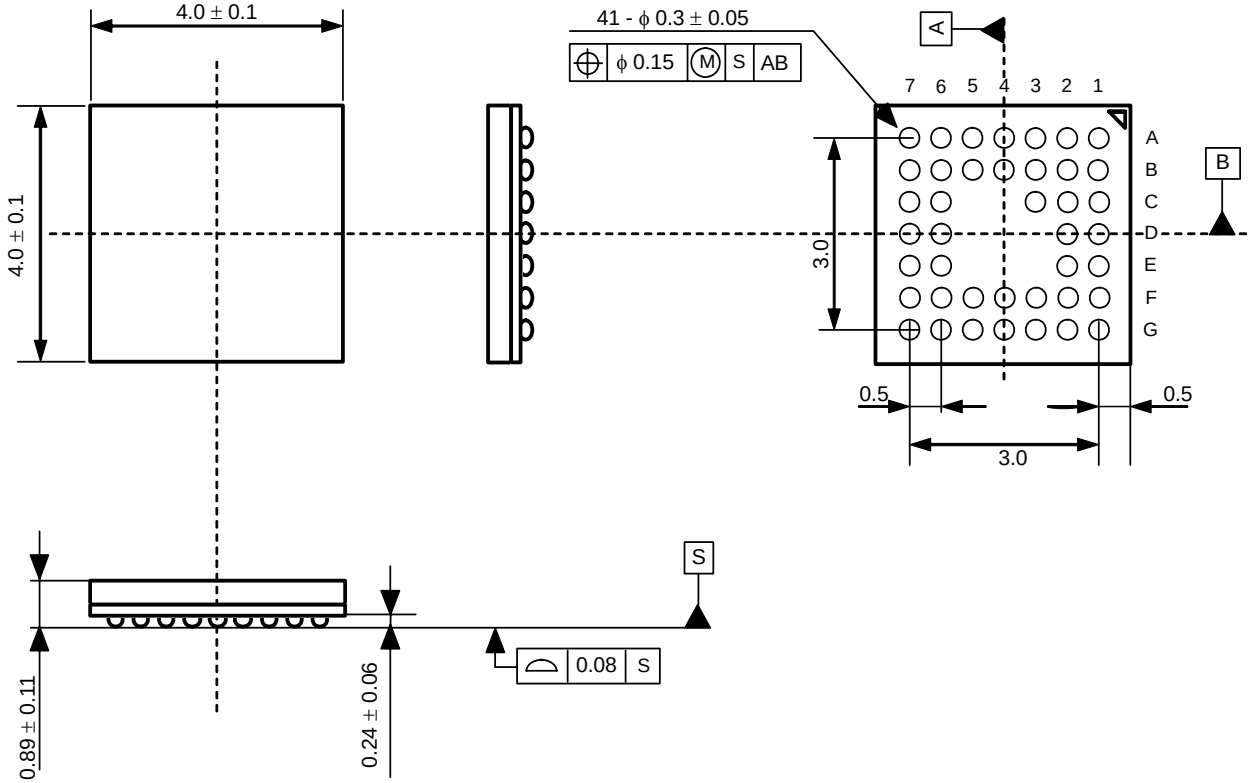


Figure 21. Keypad scanner sequence initiated by key press

PACKAGE

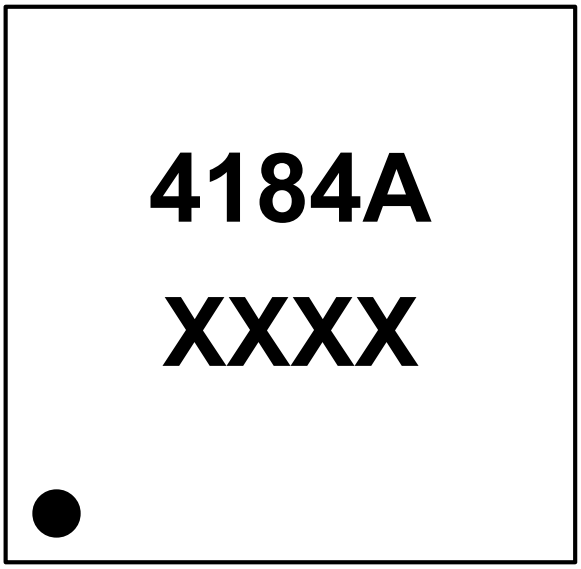
41pin FBGA (Unit: mm)



■ Material & Lead finish

Package molding compound:	Epoxy
Interposer material:	BT resin
Solder ball material:	SnAgCu

MARKING



XXXX: Date code identifier (4 digits)
Pin #A1 indication

REVISION HISTORY

Date (YY/MM/DD)	Revision	Reason	Page	Contents
08/04/16	00	First Edition		

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