

# AK8771

Shipped in packet-tape reel(5000pcs/Reel)

AK8771 is ultra-small Hall effect IC of a single silicon chip composed of Hall element and a signal processing IC.

Bipolar Hall Effect Latch

Supply Voltage 1.6~5.5V

Power down Function

Ultra High Sensitivity Bop:1.8mT

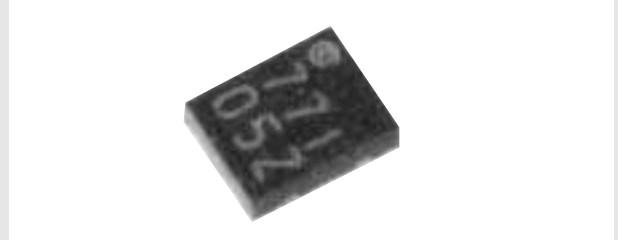
Output CMOS

SON

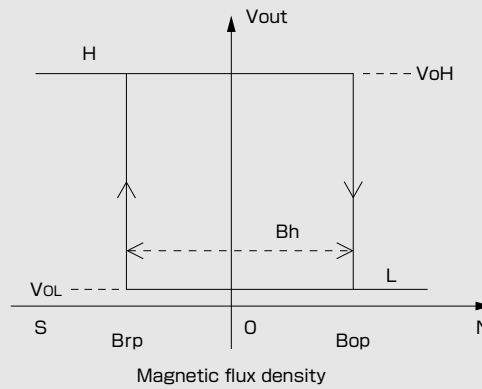
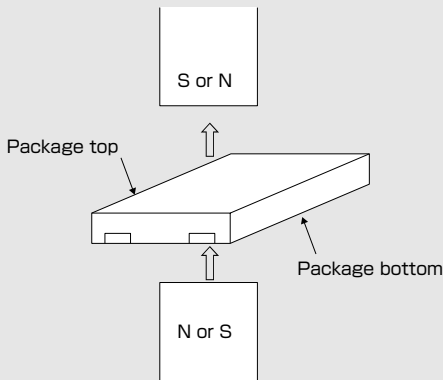
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### ●Features

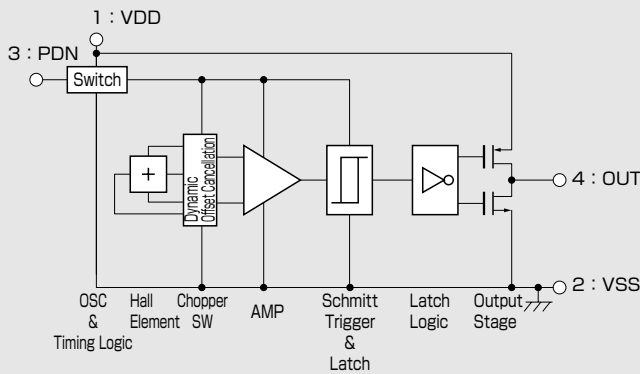
- Precision Bipolar Hall Effect Latch
- Power manageability through "PDN" pin  
Current consumption in Power down mode is less than 1μA
- Ultra small SON package : 1.1×1.4×t0.37mm, Halogen free



### ●Operational Characteristics



### ●Functional Block Diagram



Item	Function
OSC	Generates operating clock
Timing logic	Generates timing signal requires for Chopper SW, AMP and COMP
Hall Element	Hall element fabricated by CMOS process
Chopper SW	Performs chopping in order to cancel the offset voltage of Hall sensor
AMP	Reduce offset voltage and amplifies Hall output voltage
Schmitt Trigger	Hysteresis comparator
Output Stage	CMOS output, During the power down mode, output is latched in its previous state

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### ●Absolute Maximum Ratings

Item	symbol	Min.	Max.	Unit	Note
Power supply voltage	$V_{DD}$	-0.3	+6.5	V	
Output current	$I_{OUT}$	-0.5	+0.5	mA	OUT pin
Input voltage	$V_{IN}$	-0.3	$V_{DD}+0.3^*$	V	PDN pin
Input current	$I_{IN}$	-10	+10	mA	PDN pin
Storage temperature	$T_{STG}$	-55	+125	°C	

\*) Less than +6.5V.

Note) Stress beyond these listed values may cause permanent damage to the device.

### ●Recommended Operating Conditions

Item	symbol	Min.	Typ.	Max.	Unit
Power supply voltage	$V_{DD}$	1.6	3.0	5.5	V
Operating temperature	$T_a$	-30		+85	°C

### ●Electrical Characteristics ( $T_a=25^\circ\text{C}$ $V_{DD}=3.0\text{V}$ )

Item	symbol	Min.	Typ.	Max.	Unit	Note
Current consumption 1	$I_{DD1}$			1	$\mu\text{A}$	PDN=0V
Current consumption 2	$I_{DD2}$		2.5	6	mA	PDN= $V_{DD}$
PDN Input current	$I_{IN}$	-1		1	$\mu\text{A}$	
PDN input H voltage	$V_{IH}$	$0.7V_{DD}$			V	
PDN input L voltage	$V_{IL}$			0.3	V	
High Level output voltage	$V_{OH}$	$V_{DD}-0.4$			V	$I_{out}=-0.5\text{mA}$
Low level output voltage	$V_{OL}$			0.4	V	$I_{out}=+0.5\text{mA}$
PDN mode transition time 1	$T_{PD1}$			100	$\mu\text{s}$	Active→PDN
PDN mode transition time 2	$T_{PD2}$			100	$\mu\text{s}$	PDN→Active

### ●Magnetic Characteristics① ( $T_a=25^\circ\text{C}$ $V_{DD}=3.0\text{V}$ )

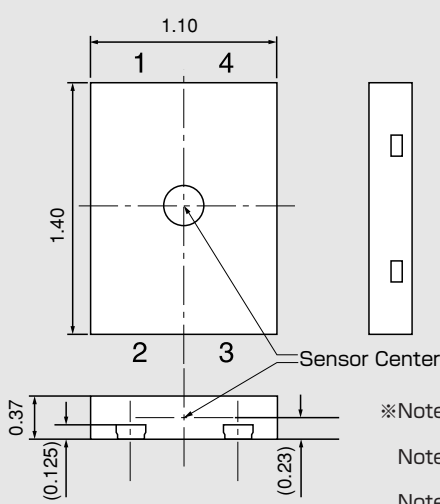
Item	symbol	Min.	Typ.	Max.	Unit
Operating point	$B_{op}$		1.8	4.0	mT
Releasing point	$B_{rp}$	-4.0	-1.8		mT
Hysteresis	$B_h$		3.6		mT

### ●Magnetic Characteristics② ( $T_a=-30^\circ\text{C}\sim 85^\circ\text{C}$ $V_{DD}=1.6\sim 5.5\text{V}$ )

Item	symbol	Min.	Typ.	Max.	Unit
Operating point	$B_{op}$		1.8	4.2	mT
Releasing point	$B_{rp}$	-4.2	-1.8		mT
Hysteresis	$B_h$		3.6		mT

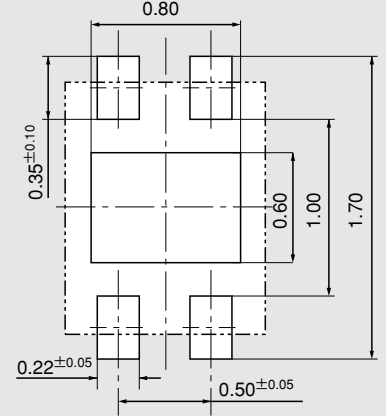
Note) The specifications in Magnetic Characteristics ② are design targets.

●Package (Unit:mm)



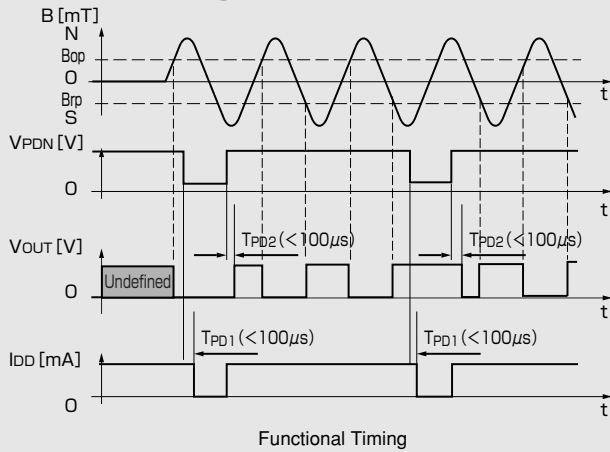
- ※Note 1) Sensitive area position referenced to the center of package within  $\phi 0.3\text{mm}$  circle.
- Note 2) Tolerances of dimension otherwise noted is  $\pm 0.05\text{mm}$ .
- Note 3) Hatched area is plated.
- Note 4) Center pad area (TAB) should be tied to the VSS or floating

●Footprint (for reference)



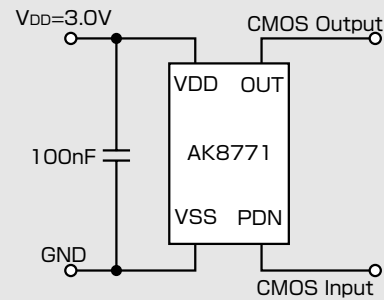
No.	Pin name	Function	Note
1	VDD	Power supply pin	
2	VSS	Ground pin	
3	PDN	Power down pin. H:Device active L:Device power down	CMOS Input. This pin has to be tied to "H" level when external power control is not used.
4	OUT	Output pin	CMOS Output

●Function Timing Chart

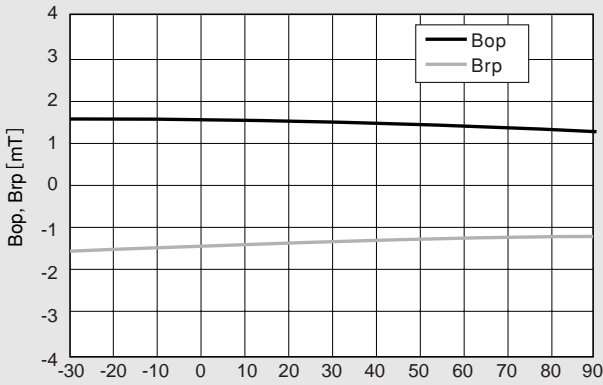


- Note1) During power down mode, output is latched in its previous state.
- Note2) When VDD is supplied, the time from reaching VDD=1.6V to the update of the output state is equal to TPD2.

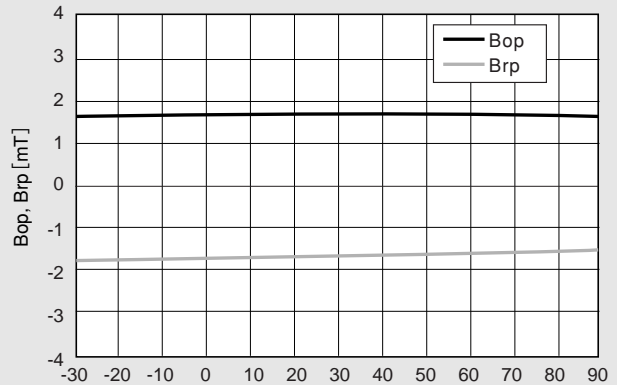
●Application Circuit



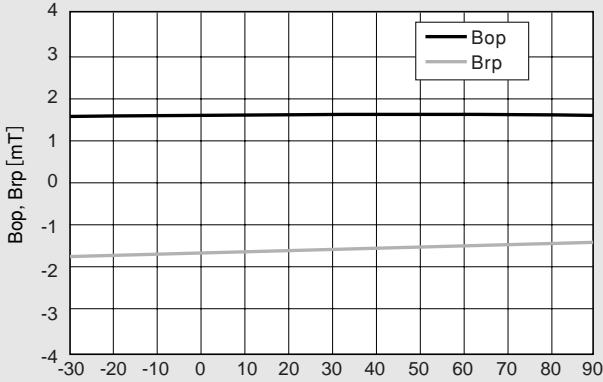
● Typical Characteristic Data (for reference)



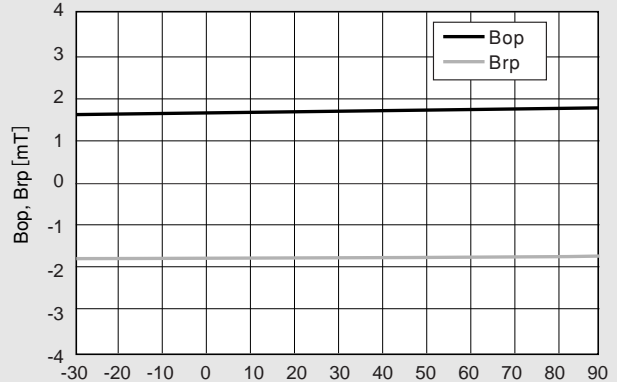
Ambient Temperature Ta [°C]  
Bop, Brp vs. Ta(VDD=1.6V)



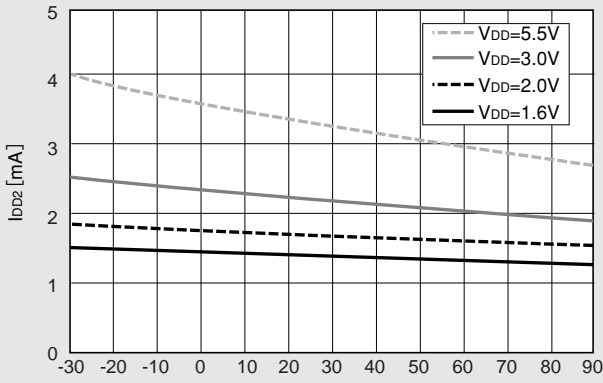
Ambient Temperature Ta [°C]  
Bop, Brp vs. Ta(VDD=3.0V)



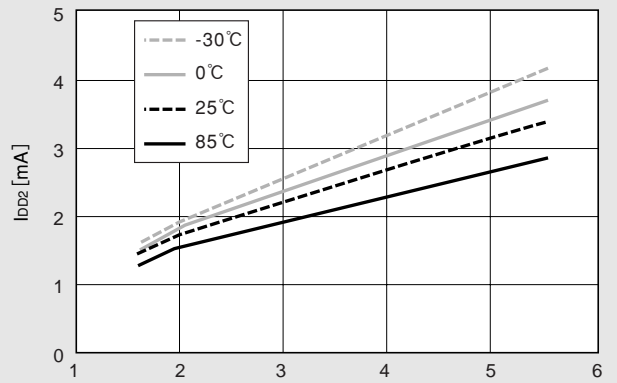
Ambient Temperature Ta [°C]  
Bop, Brp vs. Ta(VDD=2.0V)



Ambient Temperature Ta [°C]  
Bop, Brp vs. Ta(VDD=5.5V)



Ambient Temperature Ta [°C]  
IDD2 vs. Ta(in various VDD)



VDD [V]  
IDD2 vs. VDD Ta(in various Ta)

C  
00  
k  
n  
o  
p

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April 4, 2012