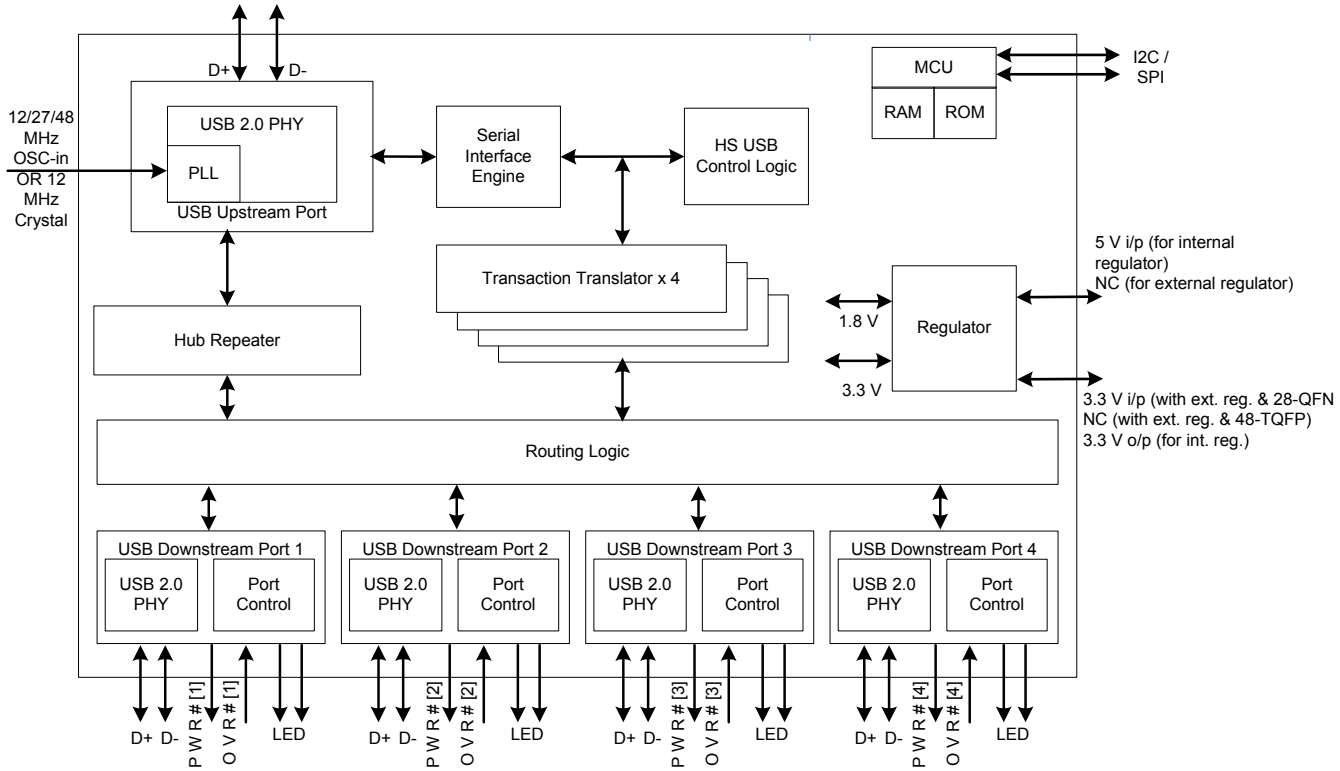
CY7C65642

HX2VL – Very Low Power USB 2.0 TetraHub™ Controller

Features

- High-performance, low-power USB 2.0 hub, optimized for low-cost designs with minimum bill-of-material (BOM).
- USB 2.0 hub controller
  - Compliant with USB2.0 specification
  - Up to four downstream ports support
  - Downstream ports are backward compatible with FS, LS
  - Multiple translator (TT), one per downstream port for maximum performance.
- Very low-power consumption
  - Supports bus-powered and self-powered modes
  - Auto switching between bus-powered and self-powered
  - Single MCU with 2 K ROM and 64 byte RAM
  - Lowest power consumption.
- Highly integrated solution for reduced BOM cost
  - Internal regulator – single power supply 5 V required.
  - Provision of connecting 3.3 V with external regulator.
  - Integrated upstream pull-up resistor
  - Integrated pull-down resistors for all downstream ports
  - Integrated upstream/downstream termination resistors
  - Integrated port status indicator control
  - 12-MHz +/-500 ppm external crystal with drive level 600 µW (integrated PLL) clock input with optional 27/48-MHz oscillator clock input.
  - Internal power failure detection for ESD recovery
- Downstream port management
  - Support individual and ganged mode power management
  - Overcurrent detection
  - Two status indicators per downstream port
  - Slew rate control for EMI management
- Maximum configurability
  - VID and PID are configurable through external EEPROM
  - Number of ports, removable/non-removable ports are configurable through EEPROM and I/O pin configuration
  - I/O pins can configure gang/individual mode power switching, reference clock source and polarity of power switch enable pin
  - Configuration options also available through mask ROM
- Available in space saving 48-pin TQFP (7 × 7 mm) and 28-pin QFN (5 × 5 mm) packages
- Supports 0 °C to +70 °C temperature range

Block Diagram



Contents

Introduction

HX2VL is Cypress's next generation family of high- performance, very low-power USB 2.0 hub controllers. HX2VL has integrated upstream and downstream transceivers; a USB serial interface engine (SIE); USB hub control and repeater logic; and transaction translator (TT) logic. Cypress has also integrated external components such as voltage regulator and pull-up/pull-down resistors, reducing the overall BOM required to implement a USB hub system.

The CY7C65642 is a part of the HX2VL portfolio with four downstream ports and an independent TT dedicated for each downstream port. This device option is for low-power but high-performance applications that require up to four downstream ports. The CY7C65642 is available in 48-pin TQFP and 28-pin QFN package options.

All device options are supported by Cypress's world class reference design kits, which include board schematics, BOM, Gerber files, Orcad files, and thorough design documentation.

HX2VL Architecture

The Block Diagram on page 1 shows the HX2VL TetraHub™ architecture.

USB Serial Interface Engine

The SIE allows HX2VL to communicate with the USB host. The SIE handles the following USB activities independently of the Hub Control Block.

- Bit stuffing and unstuffing
- Checksum generation and checking
- TOKEN type identification
- Address checking.

HS USB Control Logic

'Hub Control' block co-ordinates enumeration, suspend and resume. It generates status and control signals for host access to the hub. It also includes the frame timer that synchronizes the hub to the host. It has status/control registers which function as the interface to the firmware in the MCU.

Hub Repeater

The hub repeater manages the connectivity between upstream and downstream facing ports that are operating at the same speed. It supports full and high-speed connectivity. According to the USB 2.0 specification, the hub repeater provides the following functions:

- Sets up and tears down connectivity on packet boundaries
- Ensures orderly entry into and out of 'Suspend' state, including proper handling of remote wakeups.

MCU

The HX2VL has MCU with 2 K ROM and 64 byte RAM. The MCU operates with a 12 MHz clock to decode USB commands from host and respond to the host. It can also handle GPIO settings to provide higher flexibility to the customers and control the read interface to the EEPROM which has extended configuration options.

Transaction Translator

The TT translates data from one speed to another. A TT takes high-speed split transactions and translates them to full or low-speed transactions when the hub is operating at high-speed (the upstream port is connected to a high speed host controller) and has full or low- speed devices attached. The operating speed of a device attached on a downstream port determines whether the routing logic connects a port to the TT or to hub repeater. When the upstream host and downstream device are functioning at different speeds, the data is routed through the TT. In all other cases, the data is routed through the repeater. For example, If a full or low-speed device is connected to the high-speed host upstream through the hub, then the data transfer route includes TT. If a high-speed device is connected to the high-speed host upstream through the hub, the transfer route includes the repeater. When the hub is connected to a full-speed host controller upstream, then high-speed peripheral does not operate at its full capability. These devices only work at full speed. Full and low-speed devices connected to this hub operate at their normal speed.

Port Control

The downstream 'Port Control' block handles the connect/disconnect and over current detection as well as the power enable and LED control. It also generates the control signals for the downstream transceivers.

Applications

Typical applications for the HX2VL device family are:

- Docking stations
- Standalone hubs
- Monitor hubs
- Multi-function printers
- Digital televisions
- Advanced port replicators
- Keyboard hubs
- Gaming consoles

Functional Overview

The Cypress CY7C65642 USB 2.0 Hubs are low-power hub solutions for USB which provide maximum transfer efficiency with no TT multiplexing between downstream ports. The CY7C65642 USB 2.0 Hubs integrate 1.5 kΩ upstream pull-up resistors for full speed operation and all downstream 15 kΩ pull-down resistors and series termination resistors on all upstream and downstream D+ and D– pins. This results in optimization of system costs by providing built-in support for the USB 2.0 specification.

System Initialization

On power up, CY7C65642 has an option to enumerate from the default settings in the mask ROM or from reading an external EEPROM for configuration information. At the most basic level, this EEPROM has the Vendor ID (VID) and the Product ID (PID), for the customer's application. For more specialized applications, other configuration options can be specified. See EEPROM Configuration Options on page 12 for more details. CY7C65642 verifies the checksum before loading the EEPROM contents as the descriptors.

Enumeration

CY7C65642 enables the pull-up resistor on D+ to indicate its presence to the upstream hub, after which a USB Bus Reset is expected. After a USB Bus Reset, CY7C65642 is in an unaddressed, unconfigured state (configuration value set to'0'). During the enumeration process, the host sets the hub's address and configuration. After the hub is configured, the full hub functionality is available.

Multiple Transaction Translator Support

After TetraHub is configured in a high speed system, it is in single TT mode. The host may then set the hub into multiple TT mode by sending a SetInterface command. In multiple TT mode, each full speed port is handled independently and thus has a full 12 Mbps bandwidth available. In Single TT mode, all traffic from the host destined for full or low-speed ports are forwarded to all of those ports. This means that the 12 Mbps bandwidth is shared by all full and low-speed ports.

Upstream Port

The upstream port includes the transmitter and the receiver state machine. The transmitter and receiver operate in high speed and full speed depending on the current hub configuration. The transmitter state machine monitors the upstream facing port while the Hub Repeater has connectivity in the upstream direction. This machine prevents babble and disconnect events on the downstream facing ports of this hub from propagating and causing the hub to be disabled or disconnected by the hub to which it is attached.

Downstream Ports

The CY7C65642 supports a maximum of four downstream ports, each of which may be marked as usable or removable in the EEPROM configuration, see EEPROM Configuration Options on page 12. Additionally, it can also be configured by pin strapping, see Pin Configuration Options on page 13.

Downstream D+ and D– pull-down resistors are incorporated in CY7C65642 for each port. Before the hubs are configured, the ports are driven Single Ended Zero, ((SE0) where both D+ and D– are driven low) and are set to the unpowered state. When the hub is configured, the ports are not driven and the host may power the ports by sending a SetPortPower command for each port. After a port is powered, any connect or disconnect event is detected by the hub. Any change in the port state is reported by the hubs back to the host through the Status Change Endpoint (endpoint 1). On receipt of SetPortReset request for a port with a device connected, the hub does as follows:

- Performs a USB Reset on the corresponding port
- Puts the port in an enabled state
- Enables babble detection after the port is enabled.

Babble consists of a non idle condition on the port after EOF2. If babble is detected on an enabled port, that port is disabled. A ClearPortEnable request from the host also disables the specified port.

Downstream ports can be individually suspended by the host with the SetPortSuspend request. If the hub is not suspended, a remote wakeup event on that port is reflected to the host through a port change indication in the Hub Status Change Endpoint. If the hub is suspended, a remote wakeup event on this port is forwarded to the host. The host may resume the port by sending a ClearPortSuspend command.

Power Switching

The CY7C65642 includes interface signals for external port power switches. Both ganged and individual (per-port) configurations are supported by pin strapping, see Pin Configuration Options on page 13.

After enumerating, the host may power each port by sending a SetPortPower request for that port. Power switching and overcurrent detection are managed using respective control signals (PWR#[n] and OVR#[n]) which are connected to an external power switch device. Both High/Low enabled power switches are supported and the polarity is configured through GPIO setting, see Pin Configuration Options on page 13.

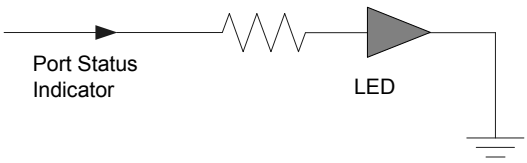
Overcurrent Detection

The OVR#[n] pins of the CY7C65642 series are connected to the respective external power switch's port overcurrent indication (output) signals. After detecting an overcurrent condition, hub reports overcurrent condition to the host and disables the PWR#[n] output to the external power device. OVR#[n] has a setup time of 20 ns. It takes 3 to 4 ms from overcurrent detection to deassertion of PWR#[n]

Port Indicators

The USB 2.0 port indicators are also supported directly by CY7C65642. According to the specification, each downstream port of the hub optionally supports a status indicator. The presence of indicators for downstream facing ports is specified by bit 7 of the wHubCharacteristics field of the hub class descriptor. The default CY7C65642 descriptor specifies that the port indicators are supported. The CY7C65642 port indicators has two modes of operation: automatic and manual.

On power up the CY7C65642 defaults to automatic mode, where the color of the Port Indicator (green, amber, off) indicates the functional status of the CY7C65642 port. The LEDs are turned off when the device is suspended.



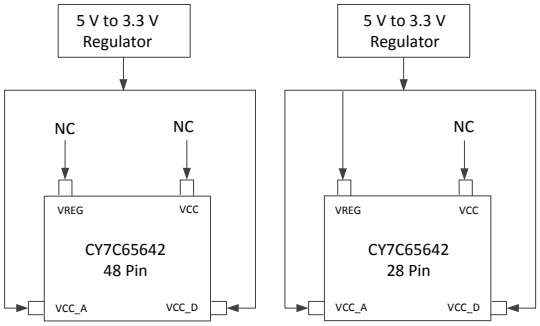
Note Pin-strapping GREEN#[1] and GREEN#[2] enables proprietary function that may affect the normal functionality of HX2VL. Configuring Port #1 and #2 as non-removable by pin-strapping should be avoided

Power Regulator

CY7C65642 requires 3.3 V source power for normal operation of internal core logic and USB physical layer (PHY). The integrated low-drop power regulator converts 5 V power input from USB cable (Vbus) to 3.3 V source power. The 3.3 V power output is guaranteed by an internal voltage reference circuit when the input voltage is within the 4 V–5.5 V range. The regulator's maximum current loading is 150 mA, which provides tolerance margin over CY7C65642's normal power consumption of below 100 mA. The on chip regulator has a quiescent current of 28 µA.

External Regulation Scheme

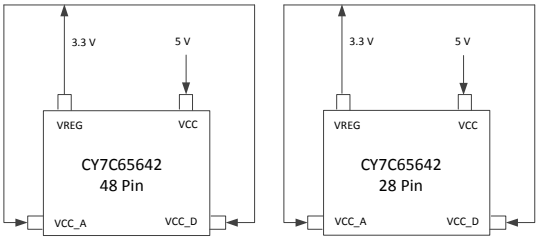
CY7C65642 supports both external regulation and internal regulation schemes. When an external regulation is chosen, then for the 48-pin package, VCC and VREG are to be left open with no connection. The external regulator output 3.3 V has to be connected to VCC_A and VCC_D pins. This connection has to be done externally, on board. For the 28-Pin package, the 3.3 V output from the external regulator has to be connected to VREG, VCC_A and VCC_D. The V_{CC} pin has to be left open with no connection. From the external input 3.3 V, 1.8 V is internally generated for the chip's internal usage.



External Regulation Scheme

Internal Regulation Scheme

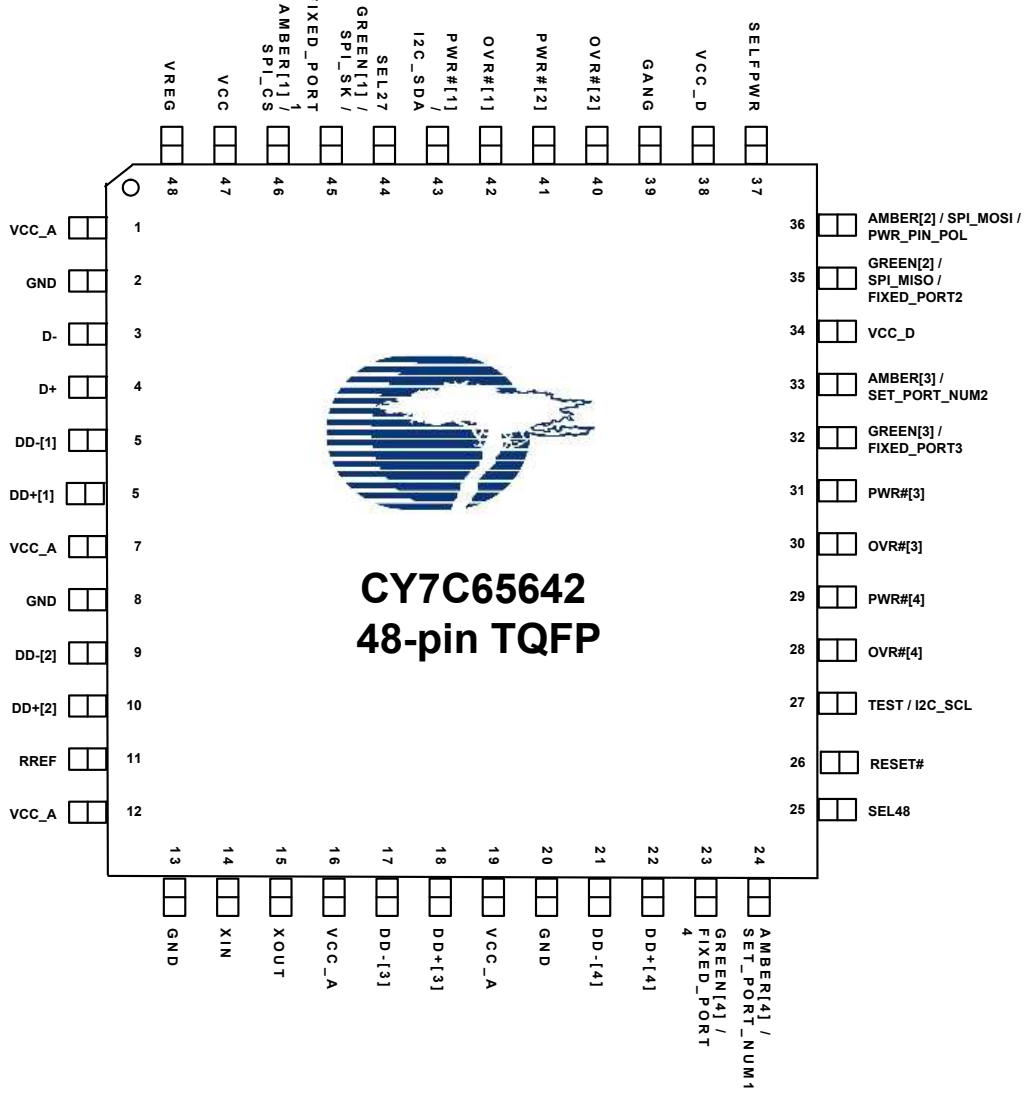
When the built-in internal regulator is chosen, then the VCC pin has to be connected to a 5 V, in both 48-pin and 28-pin packages. Internally, the built-in regulator generates a 3.3 V and 1.8 V for the chip's internal usage. Also a 3.3 V output is available at VREG pin, that has to be connected externally to VCC_A and VCC_D.



Internal Regulation Scheme

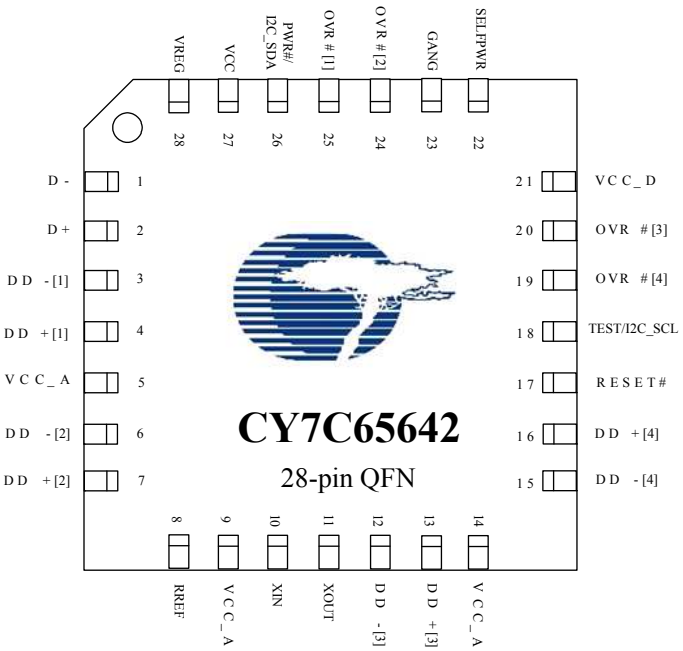
Pin Configurations

Figure 1. 48-pin TQFP (7 × 7 × 1.4 mm) pinout



Pin Configurations *(continued)*

Figure 2. 28-pin QFN (5 × 5 × 0.8 mm) pinout



Pin Definitions

48-pin TQFP Package

Pin Name	Pin No.	Type [1]	Description
Power and Clock			
VCC_A	1	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	7	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	12	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	16	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_A	19	P	**V_{CC_A}**. 3.3 V analog power to the chip.
VCC_D	34	P	**V_{CC_D}**. 3.3 V digital power to the chip.
VCC_D	38	P	**V_{CC_D}**. 3.3 V digital power to the chip.
VCC	47	P	**V_{CC}**. 5 V input to the internal regulator; NC if using external regulator
VREG	48	P	**V_{REG}**. 5–3.3 V regulator o/p during internal regulation; NC if using external regulator.
GND	2	P	**GND**. Connect to ground with as short a path as possible.
GND	8	P	**GND**. Connect to ground with as short a path as possible.
GND	13	P	**GND**. Connect to ground with as short a path as possible.
GND	20	P	**GND**. Connect to ground with as short a path as possible.
XIN	14	I	12-MHz crystal clock input, or 12/27/48MHz clock input
XOUT	15	O	12-MHz Crystal OUT. (NC if external clock is used).
SEL48 / SEL27	25 / 44	I	**Clock source selection inputs**. 00: Reserved 01: 48-MHz OSC-in 10: 27-MHz OSC-in 11: 12-MHz Crystal or OSC-in
RESET#	26	I	**Active LOW Reset**. External reset input, default pull high 10 kΩ; When RESET = low, whole chip is reset to the initial state
SELFPWR	37	I	**Self Power**. Input for selecting self/bus power. 0 is bus powered, 1 is self powered.
GANG	39	I/O	**GANG**. Default is input mode after power-on-reset. Gang Mode: Input:1 -> Output is 0 for normal operation and 1 for suspend Individual Mode: Input:0 -> Output is 1 for normal operation and 0 for suspend Refer to gang / individual power switching modes in Pin Configuration Options on page 13 for details.
RREF	11	I/O	649 Ω resistor must be connected between RREF and Ground.
System Interface			
Test I^2C_SCL	27	I(R_{DN}) I/O(R_{DN})	**Test**. 0: Normal Operation and 1: Chip will be put in test mode. **I^2C_SCL**. Can be used as I^2C clock pin to access I^2C EEPROM.
Upstream Port			
D–	3	I/O/Z	**Upstream D– Signal**.
D+	4	I/O/Z	**Upstream D+ Signal**.

Note
1. Pin Types: I = Input, O = Output, P = Power/Ground, Z = High Impedance, R_{DN} = Pad internal Pull Down Resistor, R_{UP} = Pad internal Pull Up Resistor.

Pin Definitions *(continued)*

48-pin TQFP Package

Pin Name	Pin No.	Type [1]	Description
Downstream Port 1			
DD–[1]	5	I/O/Z	**Downstream D– Signal**.
DD+[1]	6	I/O/Z	**Downstream D+ Signal**.
AMBER[1] SPI_CS	46	$O(R_{DN})$ $O(R_{DN})$	**LED**. Driver output for amber LED. port indicator support. **SPI_CS**. Can be used as chip select to access external SPI EEPROM.
GREEN[1] [2] SPI_SK FIXED_PORT1	45	$O(R_{DN})$ $O(R_{DN})$ $I(R_{DN})$	**LED**. Driver output for green LED. Port indicator support. **SPI_SK**. Can be used as SPI Clock to access external SPI EEPROM. **FIXED_PORT1**. At POR used to set Port1 as non removable port. Refer Pin Configuration Options on page 13.
OVR#[1]	42	$I(R_{UP})$	**Overcurrent Condition Detection Input**. Active LOW Overcurrent Condition Detection Input.
PWR#[1] I^2C_SDA	43	O/Z I/O	**Power Switch Driver Output**. Default is Active LOW. **I^2C_SDA**. Can be used as I^2C Data pin, connected with I^2C EEPROM.
Downstream Port 2			
DD–[2]	9	I/O/Z	**Downstream D– Signal**.
DD+[2]	10	I/O/Z	**Downstream D+ Signal**.
AMBER[2] SPI_MOSI PWR_PIN_POL	36	$O(R_{DN})$ $O(R_{DN})$ $I(R_{DN})$	**LED**. Driver output for Amber LED. Port Indicator Support. **SPI_MOSI**. Can be used as Data Out to access external SPI EEPROM. **PWR_PIN_POL**. Used for power switch enable pin polarity setting. Refer Pin Configuration Options on page 13.
GREEN[2] [2] SPI_MISO FIXED_PORT2	35	$O(R_{DN})$ $I(R_{DN})$ $I(R_{DN})$	**LED.** Driver output for Green LED. Port Indicator Support. **SPI_MISO.** Can be used as Data In to access external SPI EEPROM. **FIXED_PORT2.** At POR used to set Port2 as non removable port. Refer Pin Configuration Options on page 13.
OVR#[2]	40	$I(R_{UP})$	**Overcurrent Condition Detection Input**. Active LOW Overcurrent Condition Detection Input.
PWR#[2]	41	O/Z	**Power Switch Driver Output**. Default is Active LOW
Downstream Port 3			
DD–[3]	17	I/O/Z	**Downstream D– Signal**.
DD+[3]	18	I/O/Z	**Downstream D+ Signal**.
AMBER[3] SET_PORT_NUM2	33	$O(R_{DN})$ $I(R_{DN})$	**LED**. Driver output for Amber LED. Port indicator support. **SET_PORT_NUM2**. Used to set port numbering along with SET_PORT_NUM1. Refer Pin Configuration Options on page 13.
GREEN[3] FIXED_PORT3	32	$O(R_{DN})$ $I(R_{DN})$	**LED.** Driver output for Green LED. Port indicator support. **FIXED_PORT3**. At POR used to set Port3 as non removable port. Refer Pin Configuration Options on page 13.
OVR#[3]	30	$I(R_{UP})$	**Overcurrent Condition Detection Input**. Active LOW Overcurrent Condition Detection Input.
PWR#[3]	31	O/Z	**Power Switch Driver Output**. Default is Active LOW.

Note
2. Pin-strapping GREEN[1] and GREEN[2] enables proprietary function that may affect the normal functionality of HX2VL. Configuring Port #1 and #2 as non-removable by pin-strapping should be avoided.

Pin Definitions *(continued)*

48-pin TQFP Package

Pin Name	Pin No.	Type [1]	Description
Downstream Port 4			
DD–[4]	21	I/O/Z	**Downstream D– Signal**.
DD+[4]	22	I/O/Z	**Downstream D+ Signal**.
AMBER[4] SET_PORT_NUM1	24	$O(R_{DN})$ $I(R_{DN})$	**LED**. Driver output for Amber LED. Port Indicator Support. **SET_PORT_NUM1**. Used to set port numbering along with SET_PORT_NUM2. Refer "Pin Configuration Options" on page 13
GREEN[4] FIXED_PORT4	23	$O(R_{DN})$ $I(R_{DN})$	**LED**. Driver output for Green LED. Port Indicator Support. **FIXED_PORT4**. At POR used to set Port4 as non removable port. Refer Pin Configuration Options on page 13.
OVR#[4]	28	$I(R_{UP})$	**Overcurrent Condition Detection Input**. Active LOW Overcurrent Condition Detection Input.
PWR#[4]	29	O/Z	**Power Switch Driver Output**. Default is Active LOW.

Pin Definitions

28-pin QFN Package

Pin Name	Pin No.	Type [3]	Description
Power and Clock			
VCC_A	5	P	V_{CC_A}. 3.3 V analog power to the chip.
VCC_A	9	P	V_{CC_A}. 3.3 V analog power to the chip.
VCC_A	14	P	V_{CC_A}. 3.3 V analog power to the chip.
VCC_D	21	P	V_{CC_D}. 3.3 V digital power to the chip.
VCC	27	P	V_{CC}. 5 V input to the internal regulator; NC if using external regulator
VREG	28	P	V_{CC}. 5–3.3 V regulator o/p during internal regulation; 3.3 V i/p if using external regulator.
XIN	10	I	12-MHz crystal clock input, or 12-MHz clock input
XOUT	11	O	12-MHz Crystal OUT. (NC if external clock is used).
RESET#	17	I	**Active LOW Reset**. External reset input, default pull high 10k Ohm; When RESET = low, whole chip is reset to the initial state
SELFPWR	22	I	**Self Power**. Input for selecting self/bus power. 0 is bus powered, 1 is self powered.
GANG	23	I/O	**GANG** Default is input mode after power-on-reset. Gang Mode: Input:1 -> Output is 0 for normal operation and 1 for suspend Individual Mode: Input:0 -> Output is 1 for normal operation and 0 for suspend Refer to gang / individual power switching modes in Pin Configuration Options on page 13 for details.
RREF	8	I/O	649-Ω resistor must be connected between RREF and Ground
System Interface			
Test I2C_SCL	18	$O(R_{DN})$ $I/O(R_{DN})$	**Test**. 0: Normal Operation & 1: Chip will be put in test mode **I2C_SCL**. I^2C Clock pin.
PWR# [4] I2C_SDA	26	I/O	**Power switch driver output**. Default is active low **I2C_SDA**. I^2C Data pin.

Notes
3. Pin Types: I = Input, O = Output, P = Power/Ground, Z = High Impedance, R_{DN} = Pad internal Pull Down Resistor, R_{UP} = Pad internal Pull Up Resistor.
4. PWR#/I2C_SDA can be used as either PWR# or I2C_SDA but not as both. If EEPROM is connected then the pin will act as I2C_SDA, it will not switch to PWR# mode (as it does in 48-pin TQFP package).

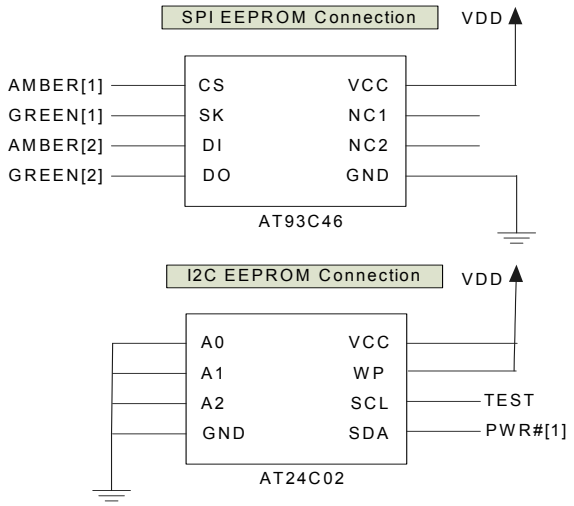
Pin Definitions *(continued)*

28-pin QFN Package

Pin Name	Pin No.	Type [3]	Description
Upstream Port			
D–	1	I/O/Z	**Upstream D– Signal**.
D+	2	I/O/Z	**Upstream D+ Signal**.
Downstream Port 1			
DD–[1]	3	I/O/Z	**Downstream D– Signal**.
DD+[1]	4	I/O/Z	**Downstream D+ Signal**.
OVR#[1]	25	I(R_{UP})	**Overcurrent Condition Detection Input.** Active LOW Overcurrent Condition Detection Input.
Downstream Port 2			
DD–[2]	6	I/O/Z	**Downstream D– Signal**.
DD+[2]	7	I/O/Z	**Downstream D+ Signal**.
OVR#[2]	24	I(R_{UP})	**Overcurrent Condition Detection Input**. Active LOW Overcurrent Condition Detection Input.
Downstream Port 3			
DD–[3]	12	I/O/Z	**Downstream D– Signal**.
DD+[3]	13	I/O/Z	**Downstream D+ Signal**.
OVR#[3]	20	I(R_{UP})	**Overcurrent Condition Detection Input**. Active LOW Overcurrent Condition Detection Input.
Downstream Port 4			
DD–[4]	15	I/O/Z	**Downstream D– Signal**.
DD+[4]	16	I/O/Z	**Downstream D+ Signal**.
OVR#[4]	19	I(R_{UP})	**Overcurrent Condition Detection Input**. Active LOW Overcurrent Condition Detection Input.
GND	PAD	P	**Ground pin for the chip**. It is the solderable exposed pad beneath the chip. Refer to the Figure 4 on page 19.

EEPROM Configuration Options

Systems using CY7C65642 have the option of using the default descriptors to configure the hub. Otherwise, it must have an external EEPROM for the device to have a unique VID, and PID. The CY7C65642 can communicate with an SPI (microwire) EEPROM like 93C46 or I^2C EEPROM like 24C02. Example EEPROM connections are shown as follows:



Note The 28-pin QFN package includes only support for I^2C EEPROM like ATMEL/24C02N_SU27 D, MICROCHIP/4LC028 SN0509, SEIKO/S24CS02AVH9. The 48-pin TQFP package includes both I^2C and SPI EEPROM connectivity options. In this case, user can use either SPI or I^2C connectivity at a time for communicating to EEPROM. The 48-pin package supports ATMEL/AT93C46DN-SH-T, in addition to the above mentioned families. HX2VL can only read from SPI EEPROM. So field programming of EEPROM will be supported only for I^2C EEPROM. The default VID and PID are 0x04B4 and 0x6572.

CY7C65642 verifies the check sum after power on reset and if validated loads the configuration from the EEPROM. To prevent this configuration from being overwritten, AMBER[1] is disabled when the SPI EEPROM is present.

Byte	Value
00h	VID_LSB
01h	VID_MSB
02h	PID_LSB
03h	PID_MSB
04h	ChkSum
05h	Reserved - FEh
06h	Removable ports
07h	Port number
08h	Maximum power
09h–0Fh	Reserved – FFh (except 0Bh which is FEh)
10h	Vendor string length
11h–3Fh	Vendor string (ASCII code)
40h	Product string length
41h–6Fh	Product string (ASCII code)
70 h	Serial number length
71h–80h	Serial number string

Byte 0: VID (LSB)

Least Significant Byte of Vendor ID

Byte 1: VID (MSB)

Most Significant Byte of Vendor ID

Byte2: PID (LSB)

Least Significant Byte of Product ID

Byte 3: PID (MSB)]

Most Significant Byte of Product ID

Byte 4: ChkSum

CY7C65642 will ignore the EEPROM settings if ChkSum is not equal to VID_LSB + VID_MSB + PID_LSB + PID_MSB +1

Byte 5: Reserved

Set to FEh

Byte 6: RemovablePorts

RemovablePorts[4:1] are the bits that indicate whether the device attached to the corresponding downstream port is removable (set to 0) or non-removable (set to 1). Bit 1 corresponds to Port 1, Bit 2 to Port 2 and so on. Default value is 0 (removable). These bit values are reported appropriately in the HubDescriptor:DeviceRemovable field.

Bits 0,5,6,7 are set to 0.

Byte 7: Port Number

Port Number indicates the number of downstream ports. The values must be 1 to 4. Default value is 4.

Byte 8: Maximum Power

This value is reported in the Configuration Descriptor: bMax-Power field and is the current in 2 mA increments that is required from the upstream hubs. The allowed range is 00h (0mA) to FAh(500mA). Default value is 32h (100mA)

Byte 9–15: Reserved

Set to FFh (except 11 which is FEh)

Byte 16: Vendor String Length

Length of the Vendor String

Byte 17 - 63: Vendor String

Value of Vendor String in ASCII code.

Byte 64: Product String Length

Length of the Product String

Byte 65- 111: Product String

Value of Product String in ASCII code

Byte 112: Serial Number Length

Length of the Serial Number

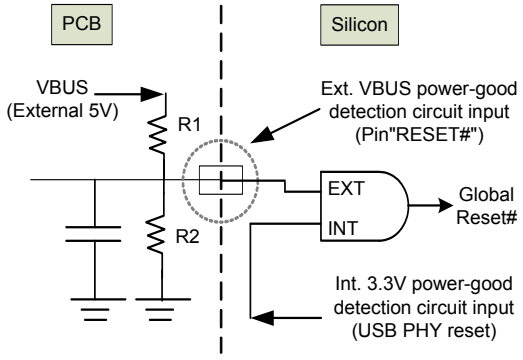
Byte 113 onwards: Serial Number String

Serial Number String in ASCII code.

Pin Configuration Options

Power ON Reset

The power on reset can be triggered by external reset or internal circuitry. The internal reset is initiated, when there is an unstable power event for silicon's internal core power (3.3 V ± 10%). The internal reset is released 2.7 µs ± 1.2% after supply reaches power good voltage (2.5 V to 2.8 V). The external reset pin, continuously senses the voltage level (5 V) on the upstream VBUS as shown in the figure. In the event of USB plug/unplug or drop in voltage, the external reset is triggered. This reset trigger can be configured using the resistors R1 and R2. Cypress recommends that the reset time applied in external reset circuit should be longer than that of the internal reset time.



Gang/Individual Power Switching Mode

A single pin is used to set individual / gang mode as well as output the suspend flag. This is done to reduce the pin count. The individual or gang mode is decided within 20 µs after power on reset. It has a setup time of 1ns. 50 to 60ms after reset, this pin is changed to output mode. CY7C65642 outputs the suspend flag, once it is globally suspended. Pull-down resistor of greater than 100K is needed for Individual mode and a pull-up resistor greater than 100K is needed for Gang mode. Figure below shows the suspend LED indicator schematics. The polarity of LED must be followed, otherwise the suspend current will be over the spec limitation (2.5 mA).

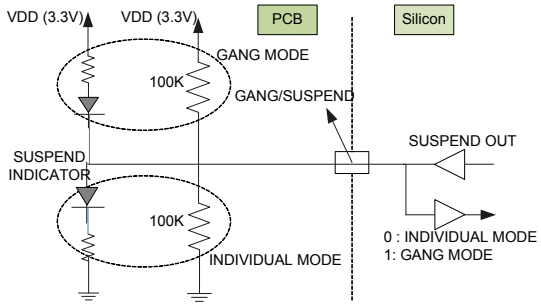


Table 1. Features supported in 48-pin and 28-pin packages

Supported Features	48-pin	28-pin
Port number configuration	Yes	No
Non-removable port configuration	Yes	No
Reference clock configuration	Yes	No
Power switch enable polarity	Yes	No
LED Indicator	Yes	No

Power Switch Enable Pin Polarity

The pin polarity is set active-high by pin-strapping the PWR_PIN_POL pin to 1 and Active-Low by pin-strapping the PWR_PIN_POL pin to 0. Thus, both kinds of power switches are supported. This feature is not supported in 28-pin QFN package.

Port Number Configuration

In addition to the EEPROM configuration, as described above, configuring the hub for 2/3/4 ports is also supported using pin-strapping SET_PORT_NUM1 and SET_PORT_NUM2, as shown in following table.Pin strapping option is not supported in the 28-pin QFN package.

SET_PORT_NUM2	SET_PORT_NUM1	# Ports
1	1	1 (Port 1)
1	0	2 (Port 1/2)
0	1	3 (Port 1/2/3)
0	0	4 (All ports)

Non Removable Ports Configuration

In embedded systems, downstream ports that are always connected inside the system, can be set as non-removable (always connected) ports, by pin-strapping the corresponding FIXED_PORT# pins 1~4 to High, before power on reset. At POR, if the pin is pull high, the corresponding port is set to non-removable. This is not supported in the 28-pin QFN package.

Reference Clock Configuration

This hub can support, optional 27/48-MHz clock source. When on-board 27/48-MHz clock is present, then using this feature, system integrator can further reduce the BOM cost by eliminating the external crystal. This is available through GPIO pin configuration shown below. This is not supported in the 28-pin QFN package.

SEL48	SEL27	Clock Source
0	1	48-MHz OSC-in
1	0	27-MHz OSC-in
1	1	12-MHz X'tal/OSC-in

Absolute Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature ..... –60 °C to +100 °C

Ambient temperature ..... 0 °C to +70 °C

5 V supply voltage to ground potential .....–0.5 V to +6.0 V

3.3 V supply voltage to ground potential .....–0.5 V to +3.6 V

Voltage at open drain input pins (OVR#1-4, SELFPWR, RESET#) .....–0.5 V to +5.5 V

3.3 V Input Voltage for Digital I/O .....–0.5 V to +3.6 V

FOSC (oscillator or crystal frequency) ..... 12 MHz ± 0.05%

Operating Conditions

Ambient temperature ..... 0 °C to +70 °C

Ambient max junction temperature ..... 0 °C to +125 °C

5 V supply voltage to ground potential .....4.75 V to +5.25 V

3.3 V supply voltage to ground potential .....3.15 V to +3.6 V

Input voltage for USB signal pins .....0.5 V to +3.6 V

Voltage at open drain input pins .....–0.5 V to +5.0 V

Thermal characteristics 48-pin TQFP ..... 78.7 °C/W

Thermal characteristics 28-pin QFN ..... 33.3 °C/W

Electrical Characteristics

DC Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max		Unit
					External regulator	Internal regulator	
P_D	Power dissipation	Excluding USB signals	–	–	432		mW
V_{IH}	Input high voltage	–	2	–	–		V
V_{IL}	Input low voltage	–	–	–	0.8		V
I_I	Input leakage current	Full speed / low speed ($0 < V_{IN} < V_{CC}$)	–10	–	+10		µA
		High speed mode ($0 < V_{IN} < V_{CC}$)	–5	0	+5		µA
V_{OH}	Output voltage high	I_{OH} = 8 mA	2.4	–	–		V
V_{OL}	Output low voltage	I_{OL}= 8 mA	–	–	0.4		V
R_{DN}	Pad internal pull-down resistor	–	81	103	181		KΩ
R_{UP}	Pad internal pull-up resistor	–	81	103	181		KΩ
C_{IN}	Input pin capacitance	Full speed / low speed mode	–	–	20		pF
		high speed mode	4	4.5	5		pF
I_{SUSP}	Suspend current	–	–	0.786	1.043	1.3	mA
I_{CC}	**Supply Current**						
	4 Active ports	Full speed host, full speed devices	–	88.7	103.9	105.4	mA
		High speed host, high speed devices	–	81.9	88.2	89.3	mA
		High speed host, full speed devices	–	88.2	101.2	102.3	mA
	3 Active ports	Full speed host, full speed devices	–	79.1	91.6	93	mA
		High speed host, high speed devices	–	72.9	78.5	78.6	mA
		High speed host, full speed devices	–	75.9	88.7	88.8	mA
	2 Active ports	Full speed host, full speed devices	–	68.1	78.4	78.6	mA
		High speed host, high speed devices	–	61.9	67.6	69.6	mA
		High speed host, full speed devices	–	64.9	75.4	76.1	mA
	1 Active ports	Full speed host, full speed devices	–	57.1	66.3	66.7	mA
		High speed host, high speed devices	–	51.9	57.6	59.3	mA
		High speed host, full speed devices	–	54.7	61.1	62.5	mA
	No Active ports	Full speed host	–	42.8	48.9	50.3	mA
		High speed host	–	44.2	49.1	50.6	mA

AC Electrical Characteristics

USB Transceiver is USB 2.0 certified in low, full and high speed modes.

Both the upstream USB transceiver and all four downstream transceivers have passed the USB-IF USB 2.0 Electrical Certification Testing.

The 48-pin TQFP package can support communication to EEPROM using either I^2C or SPI. The 28-pin QFN package can support only I^2C communication to EEPROM.

AC characteristics of these two interfaces to EEPROM are summarized in tables below:

AC Characteristics of SPI EEPROM interface

Parameter	Parameter	Min	Typ	Max	Units
t_{CSS}	CS setup time	3.0	–	–	µs
t_{CSH}	CS hold time	3.0	–	–	
t_{SKH}	SK high time	1.0	–	–	
t_{SKL}	SK low time	2.2	–	–	
t_{DIS}	DI setup time	1.8	–	–	
t_{DIH}	DI hold time	2.4	–	–	
t_{PD1}	Output delay to ‘1’	–	–	1.8	
t_{PD0}	Output delay to ‘0’	–	–	1.8	

AC Characteristics of I^2C EEPROM interface

Parameter	Parameter	1.8 V–5.5 V		2.5 V–5.5 V		Units
		Min	Max	Min	Max	
f_{SCL}	SCL clock frequency	0.0	100	0.0	400	KHz
t_{LOW}	Clock LOW Period	4.7	–	1.2	–	us
t_{HIGH}	Clock HIGH Period	4.0	–	0.6	–	us
$t_{SU:STA}$	Start condition setup time	4.7	–	0.6	–	us
$t_{SU:STO}$	Stop condition setup time	4.7	–	0.6	–	us
$t_{HD:STA}$	Start condition hold time	4.0	–	0.6	–	us
$t_{HD:STO}$	Stop condition hold time	4.0	–	0.6	–	us
$t_{SU:DAT}$	Data in setup time	200.0	–	100.0	–	ns
$t_{HD:DAT}$	Data in hold time	0	–	0	–	ns
t_{DH}	Data out hold time	100	–	50	–	ns
t_{AA}	Clock to output	0.1	4.5	0.1	–	us
t_{WR}	Write cycle time	–	10	–	5	ns

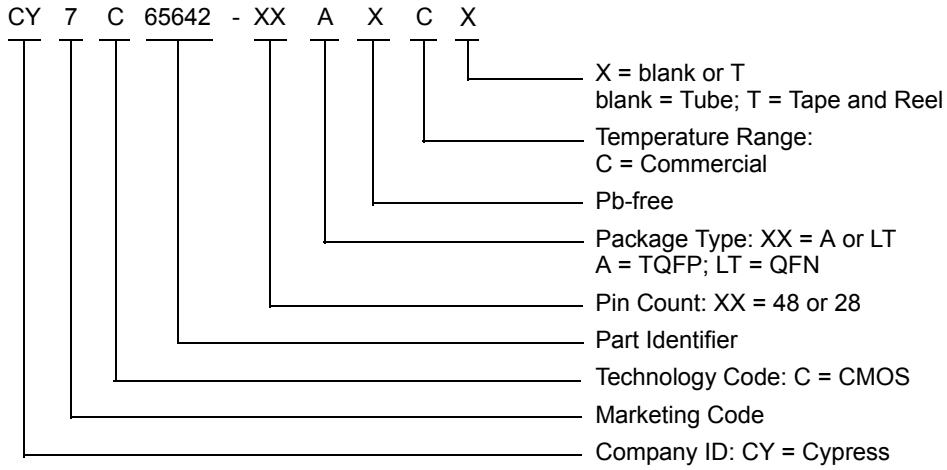
Thermal Resistance

Parameter	Description	48-pin TQFP Package	28-pin QFN Package	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	78.7	33.3	°C/W
Θ_{JC}	Thermal resistance (junction to case)	35.3	18.4	°C/W

Ordering Information

Ordering Code	Package Type
CY7C65642-48AXC	48-pin TQFP Bulk
CY7C65642-48AXCT	48-pin TQFP Tape and Reel
CY7C65642-28LTXC	28-pin QFN Bulk

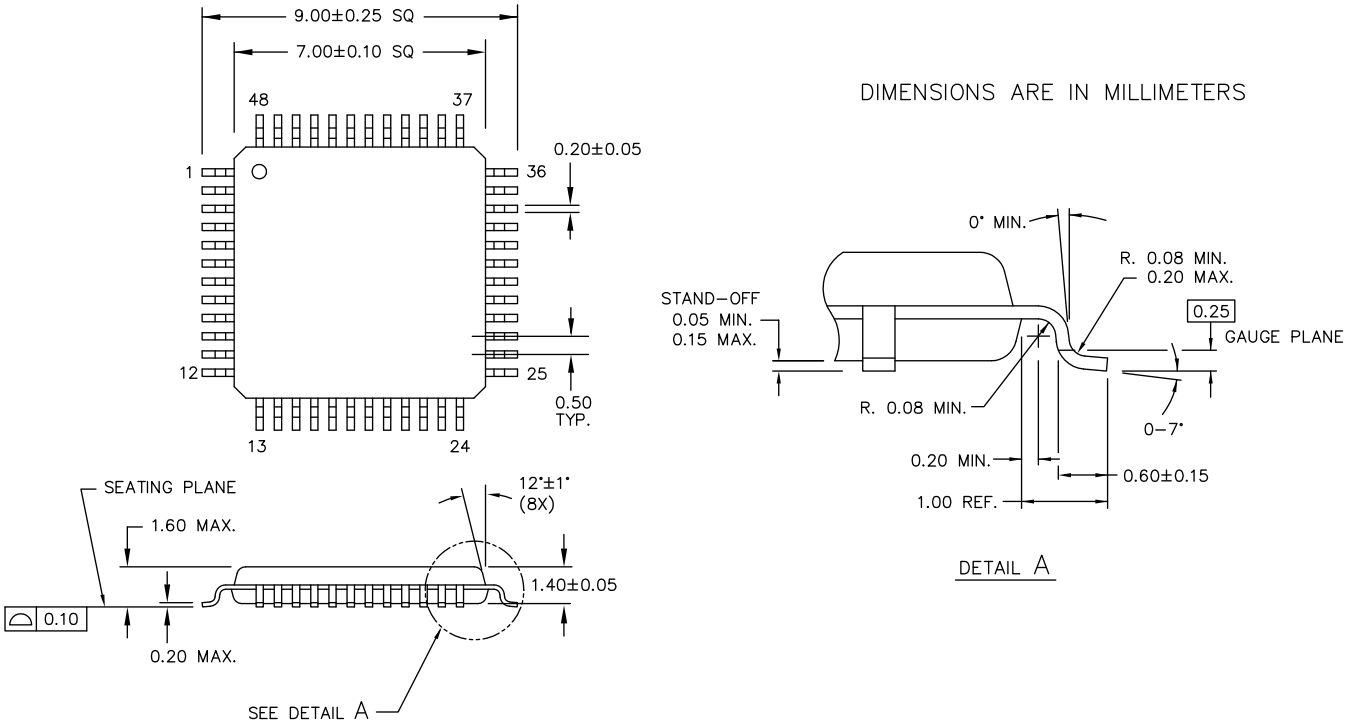
Ordering Code Definitions



Package Diagrams

The CY7C65642 is available in following packages:

Figure 3. 48-pin TQFP (7 × 7 × 1.4 mm) A48 Package Outline, 51-85135

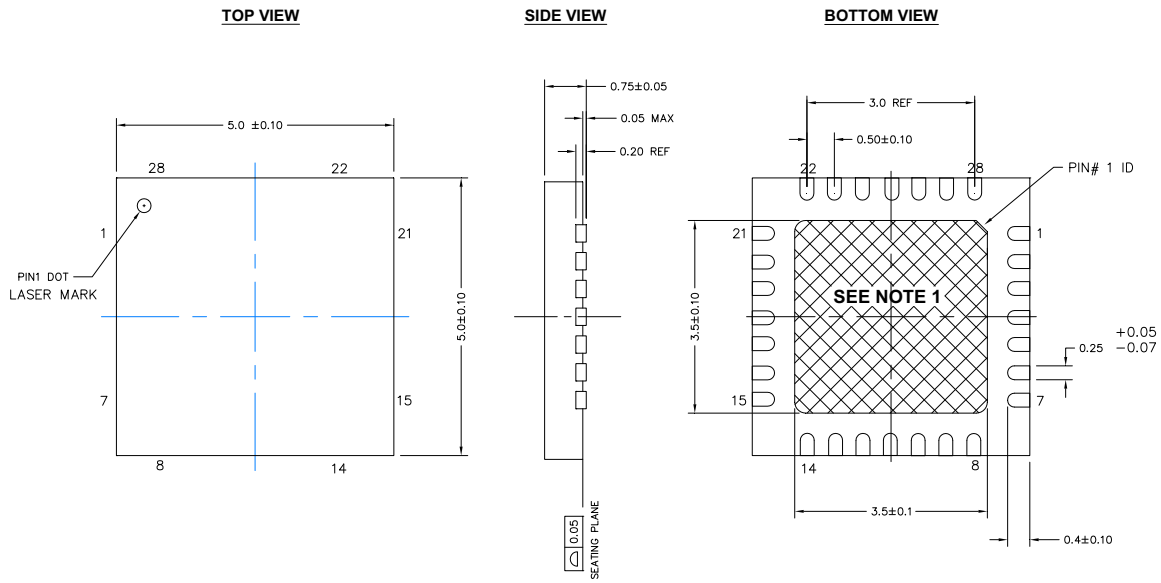


51-85135 *B

Package Diagrams *(continued)*

The CY7C65642 is available in following packages:

Figure 4. 28-pin QFN (5 × 5 × 0.8 mm), LT28A (3.5 × 3.5 E-Pad), Sawn Package Outline, 001-64621



NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. PACKAGE WEIGHT: ~0.05gr
4. DIMENSIONS ARE IN MILLIMETERS

001-64621 **

Acronyms

Acronym	Description
AC	alternating current
ASCII	american standard code for information interchange
EEPROM	electrically erasable programmable read only memory
EMI	electromagnetic interference
ESD	electrostatic discharge
GPIO	general purpose input/output
I/O	input/output
LED	light emitting diode
LSB	least significant bit
MSB	most significant bit
PCB	printed circuit board
PLL	phase-locked loop
POR	power on reset
PSoC®	Programmable System-on-Chip™
QFN	quad flat no leads
RAM	random access memory
ROM	read only memory
SIE	serial interface engine
TQFP	thin quad flat pack
TT	transaction translator
USB	universal serial bus

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
µA	microampere
µs	microsecond
µW	microwatt
mA	milliampere
mm	millimeter
ms	millisecond
mW	milliwatt
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
ppm	parts per million
V	volt
W	watt

Document History Page

Document Title: CY7C65642, HX2VL – Very Low Power USB 2.0 TetraHub™ Controller Document Number: 001-65659				
Rev.	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3176751	SWAK	02/18/2011	New data sheet.
*A	3250883	SWAK / AASI	06/29/2011	Updated Functional Overview (Updated Port Indicators (Added a Note "Pin-strapping GREEN#[1] and GREEN#[2] enables proprietary function that may affect the normal functionality of HX2VL. Configuring Port #1 and #2 as non-removable by pin-strapping should be avoided."). Updated Pin Configurations (Updated Figure 1 (Pin of the 48-pin TQFP package was named SELF_PWR. It is changed to SELFPWR.)). Updated Pin Definitions (Updated description of XIN pin to "12-MHz crystal clock input, or 12-MHz clock input" (since 28-pin package does not support 27 and 48 MHz), updated description of XOUT pin to "12-MHz Crystal OUT. (NC if external clock is used)", changed value from 680 Ω to 650 Ω in description of RREF pin, changed description of OVR# pins from "Default is Active LOW" to "Active LOW Overcurrent Condition Detection Input" (since the polarity is not configurable), changed all seven occurrences of "Refer "48-pin TQFP Pin Configuration" on page 5" to "Refer Pin Configuration Options on page 13", added Note 2 and referred the same Note in GREEN#[1] and GREEN#[2] pins). Updated Pin Definitions (Updated description of XIN pin to "12-MHz crystal clock input, or 12-MHz clock input" (since 28-pin package does not support 27 and 48 MHz), updated description of XOUT pin to "12-MHz Crystal OUT. (NC if external clock is used)", changed description of OVR# pins from "Default is Active LOW" to "Active LOW Overcurrent Condition Detection Input" (since the polarity is not configurable)). Updated Functional Overview (Updated Power Regulator (Changed regulator's maximum current loading from 200 mA to 150 mA)). Updated Pin Configuration Options (Updated Power Switch Enable Pin Polarity (Replaced first two occurrences of the word "setting" with "pin-strapping")). Updated Electrical Characteristics (Updated DC Electrical Characteristics (Updated maximum value of I_{SUSP} parameter to 903 µA, updated maximum values of I_{CC} parameter)).
*B	3327505	AASI	07/27/2011	Changed status from Preliminary to Final. Updated Pin Definitions (Minor edits). Updated Ordering Information (Updated part numbers) and Ordering Code Definitions.
*C	3525169	AASI	02/16/2012	Updated Pin Configurations (Updated Figure 1 (Renamed SPI_DI to SPI_MOSI, renamed SPI_DO to SPI_MISO respectively for clarity)). Updated Pin Definitions (Renamed SPI_DI to SPI_MOSI, renamed SPI_DO to SPI_MISO respectively for clarity). Updated Pin Definitions (Updated description of PWR# of 28-pin package (To describe the alternate function I2C_SDA)).
*D	3637477	AASI	07/02/2012	Updated EEPROM Configuration Options (Changed the value of Byte 5 to FEh to match with the tabular column). Updated Electrical Characteristics (Updated DC Electrical Characteristics (Splitted the Max column into two columns namely External regulator and Internal regulator for I_{SUSP} and I_{CC} parameters and updated the corresponding values)). Added Thermal Resistance. Updated Ordering Information (Updated part numbers). Updated in new template.

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