Failsafe™ 2.5 V/3.3 V Zero Delay Buffer

Features

- Internal DCXO for continuous glitch-free operation
- Zero input-output propagation delay
- 100 ps typical output cycle-to-cycle jitter
- 110 ps typical output-output skew
- 1 MHz to 200 MHz reference input
- Supports industry standard input crystals
- 200 MHz (commercial), 166 MHz (industrial) outputs
- 5 V-tolerant inputs
- Phase-locked loop (PLL) bypass mode
- Dual reference inputs
- 28-pin SSOP
- Split 2.5 V or 3.3 V output power supplies
- 3.3 V core power supply
- Industrial temperature available

Functional Description

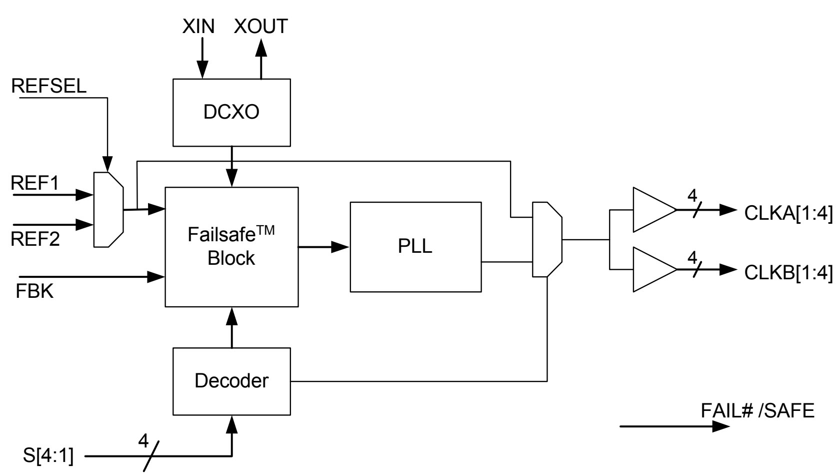
The CY23FS08 is a FailSafe™ Zero Delay Buffer with two reference clock inputs and eight phase-aligned outputs. The device provides an optimum solution for applications where continuous operation is required in the event of a primary clock failure.

Continuous, glitch-free operation is achieved by using a DCXO, which serves as a redundant clock source in the event of a reference clock failure by maintaining the last frequency and phase information of the reference clock.

The unique feature of the CY23FS08 is that the DCXO is in fact the primary clocking source, which is synchronized (phase-aligned) to the external reference clock. When this external clock is restored, the DCXO automatically resynchronizes to the external clock.

The frequency of the crystal connected to the DCXO, must be chosen to be an integer factor of the frequency of the reference clock. This factor is set by four select lines: S[4:1]. see Table 2. The CY23FS08 has three split power supplies; one for core, another for Bank A outputs, and the third for Bank B outputs. Each output power supply, except VDDC can be connected to either 2.5 V or 3.3 V. VDDC is the power supply pin for internal circuits and must be connected to 3.3 V.

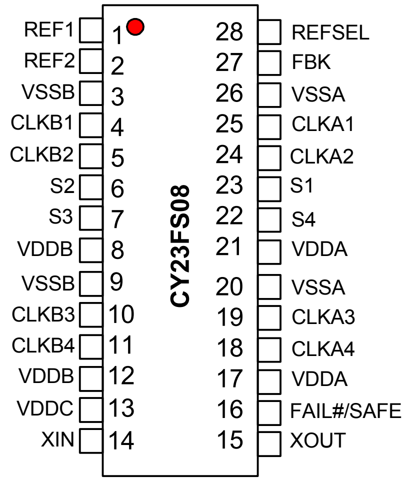
Logic Block Diagram



Contents

Pinouts

Figure 1. Pin Configuration



28-pin SSOP

Table 1. Pin Definitions

Pin Number	Pin Name	Description
1,2	REF1,REF2	**Reference clock inputs.**[4] 5 V tolerant.
4,5,10,11	CLKB[1:4]	**Bank B clock outputs**.[1, 2]
25,24,19,18	CLKA[1:4]	**Bank A clock outputs.**[1, 2]
27	FBK	**Feedback input to the PLL**.[1]
23,6,7,22	S[1:4]	**Frequency select pins/PLL and DCXO bypass**.[3]
14	XIN	**Reference crystal input**.
15	XOUT	**Reference crystal output**.
16	FAIL#/SAFE	**Valid reference indicator**. A high level indicates a valid reference input.
13	VDDC	**3.3 V power supply for the internal circuitry**.
8,12	VDDB	**2.5 V or 3.3 V power supply for Bank B outputs**.
3,9	VSSB	**Ground**.
17,21	VDDA	**2.5 V or 3.3 V power supply for Bank A outputs**.
20,26	VSSA	**Ground**.
28	REFSEL	**Reference select**. Selects the active reference clock from either REF1 or REF2. When REFSEL = 1, REF1 is selected. When REFSEL = 0, REF2 is selected.

Table 2. Configuration Table

S[4:1]	XTAL (MHz)		REF(MHz)		OUT(MHz)		REF:OUT Ratio	REF:XTAL Ratio	Out:XTAL Ratio
	Min	Max	Min	Max	Min	Max			
0000			PLL and DCXO Bypass mode						
1000	8.33	30	16.67	60.00	8.33	30.00	÷2	2	1
1110	9.50	30	57.00	180.00	28.50	90.00	÷2	6	3

Notes
1. For normal operation, connect either one of the eight clock outputs to the FBK input.
2. Weak pull downs on all CLK outputs.
3. Weak pull ups on these inputs.
4. Weak pull downs on these inputs.

Table 2. Configuration Table (continued)

S[4:1]	XTAL (MHz)		REF(MHz)		OUT(MHz)		REF:OUT Ratio	REF:XTAL Ratio	Out:XTAL Ratio
	Min	Max	Min	Max	Min	Max			
0101	8.50	30	6.80	24.00	1.70	6.00	÷4	4/5	1/5
1011	8.33	30	25.00	90.00	6.25	22.50	÷4	3	3/4
0011	8.33	30	2.78	10.00	2.78	10.00	×1	1/3	1/3
1001	8.33	30	8.33	30.00	8.33	30.00	×1	1	1
1111	8.00	25	32.00	100.00	32.00	100.00	×1	4	4
1100	8.00	25	64.00	200.00	64.00	200.00	×1	8	8
0001	8.33	30	1.04	3.75	2.08	7.50	×2	1/8	1/4
0110	8.33	30	4.17	15.00	8.33	30.00	×2	1/2	1
1101	8.33	30	16.67	60.00	33.33	120.00	×2	2	4
0100	8.33	30	4.17	15.00	16.67	60.00	×4	1/2	2
1010	8.33	30	12.50	45.00	50.00	180.00	×4	3/2	6
0010	8.33	30	1.39	5.00	11.11	40.00	×8	1/6	4/3
0111	8.33	30	6.25	22.50	50.00	180.00	×8	3/4	6

FailSafe Function

The CY23FS08 is targeted at clock distribution applications that requires or may require continued operation if the main reference clock fails. Existing approaches to this requirement have used multiple reference clocks with either internal or external methods to switch between references. The problem with this technique is that it leads to interruptions (or glitches) when transitioning from one reference to another, often requiring complex external circuitry or software to maintain system stability. The technique implemented in this design completely eliminates any switching of references to the PLL, greatly simplifying system design.

The CY23FS08 PLL is driven by the crystal oscillator, which is phase-aligned to an external reference clock so that the output of the device is effectively phase-aligned to reference via the external feedback loop. This is accomplished by using a digitally controlled capacitor array to pull the crystal frequency over an approximate range of ±300 ppm from its nominal frequency.

In this mode, if the reference frequency fails (that is, stops or disappears), the DCXO maintains its last setting and a flag signal (FAIL#/SAFE) is set to indicate failure of the reference clock.

The CY23FS08 provides four select bits, S1 through S4 to control the reference to crystal frequency ratio. The DCXO is internally tuned to the phase and frequency of the external reference only when the reference frequency divided by this ratio is within the DCXO capture range. If the frequency is out of range, a flag is set on the FAIL#/SAFE pin notifying the system that the selected reference is not valid. If the reference moves in range, then the flag is cleared, indicating to the system that the selected reference is valid.

Figure 2. Fail#/Safe Timing for Input Reference Failing Catastrophically

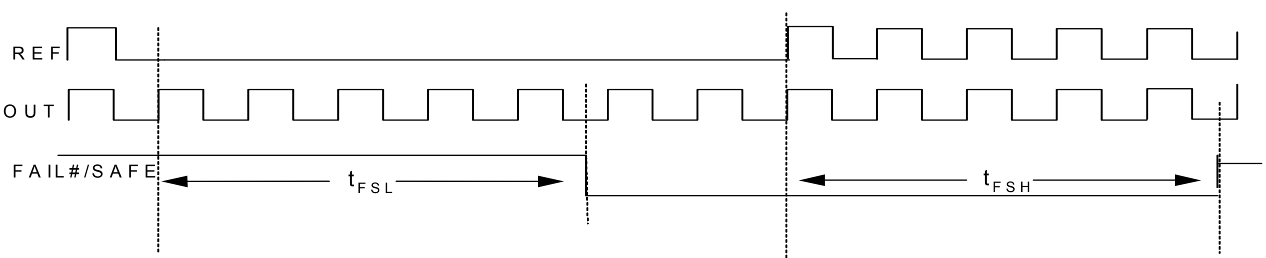


Figure 3. Fail#/Safe Timing Formula

$$t_{FSL(max)} = 2(t_{REF} \times n) + 25ns$$

$$n = \frac{F_{REF}}{F_{XTAL}} = 4 \text{ (in above example)}$$

$$t_{FSH(min)} = 12(t_{REF} \times n) + 25ns$$

Table 3. Failsafe Timing Table

Parameter	Description	Conditions	Min	Max	Unit
t_{FSL}	Fail#/Safe Assert Delay	Measured at 80% to 20%, Load = 15 pF		See Figure 3	ns
t_{FSH}	Fail#/Safe Deassert Delay	Measured at 80% to 20%, Load = 15 pF	See Figure 3		ns

Figure 4. FailSafe Timing Diagram: Input Reference Slowly Drifting Out of FailSafe Capture Range

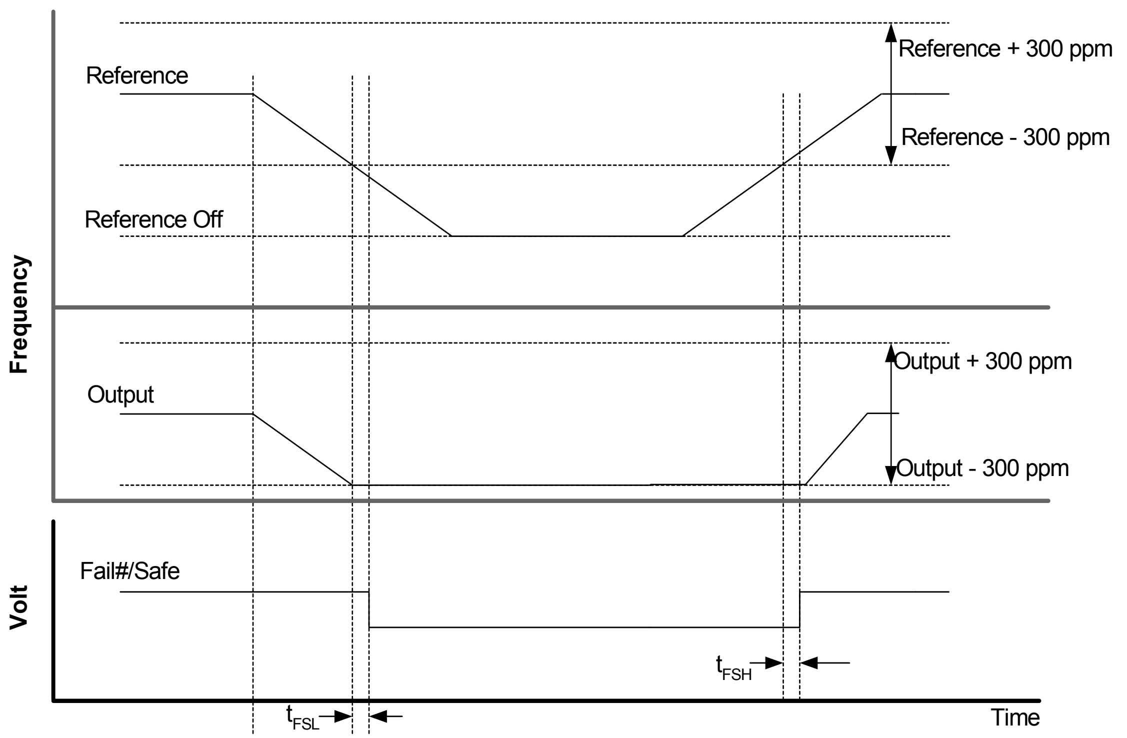
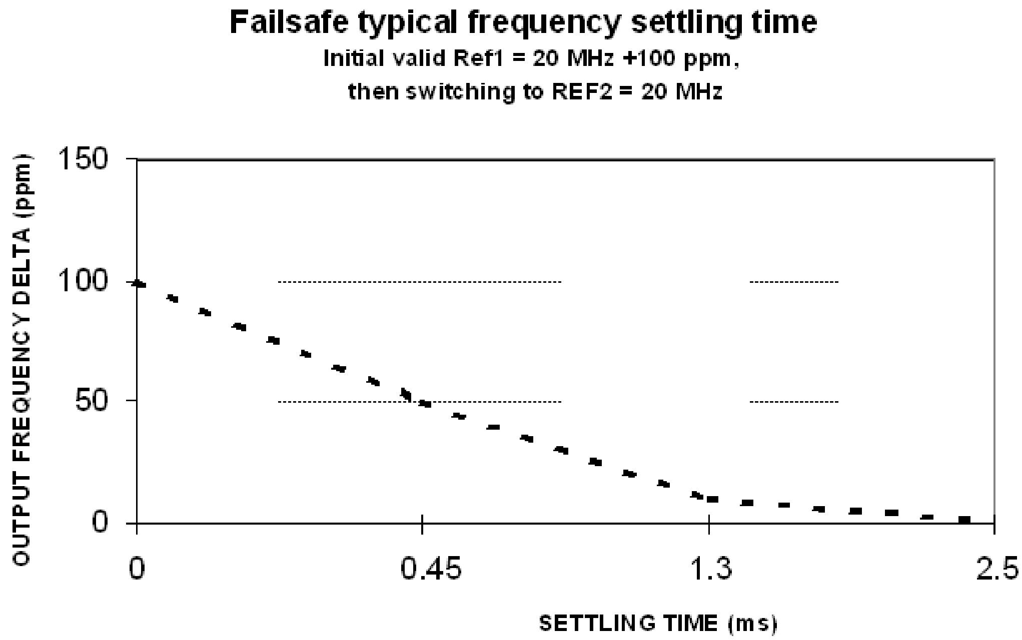


Figure 5. FailSafe Reference Switching Behavior



Because of the DCXO architecture, the CY23FS08 has a much lower bandwidth than a typical PLL-based clock generator. This is shown in Figure 6. This low bandwidth makes the CY23FS08 also useful as a jitter attenuator. The loop bandwidth curve is also known as the jitter transfer curve.

Figure 6. FailSafe Effective Loop Bandwidth (min)

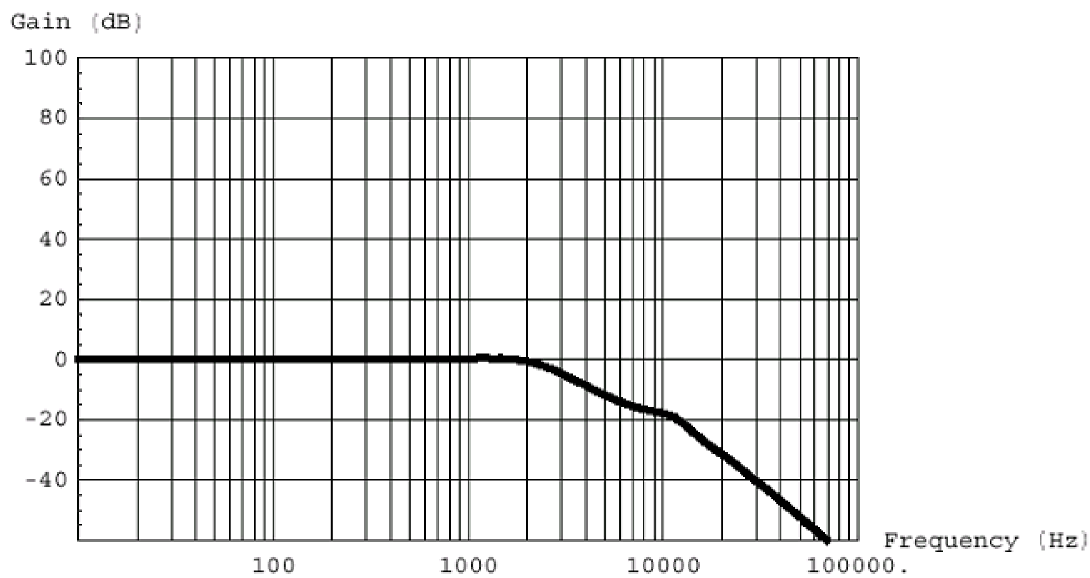


Figure 7. Duty Cycle

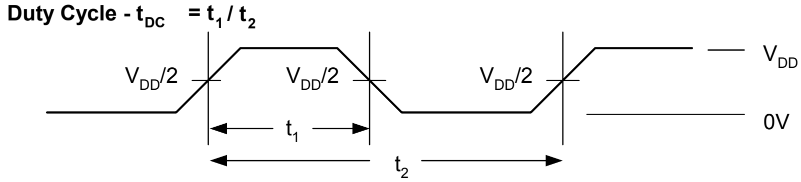


Figure 8. Input Slew Rate

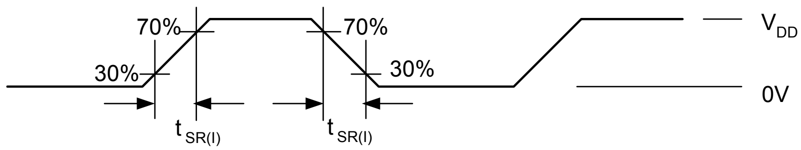


Figure 9. Output Slew Rate

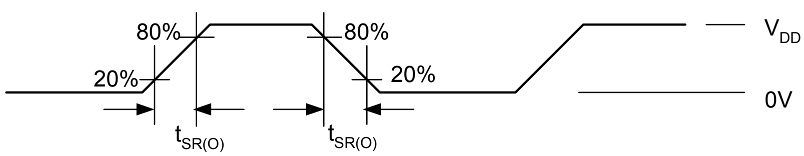


Figure 10. Output to Output Skew and Intrabank Skew

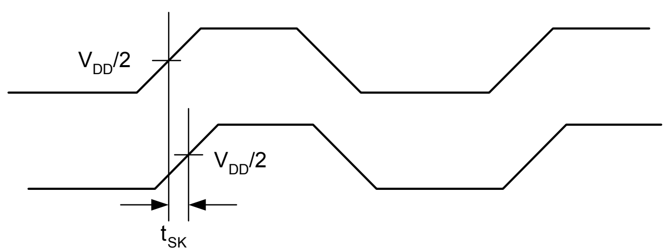


Figure 11. Part to Part Skew

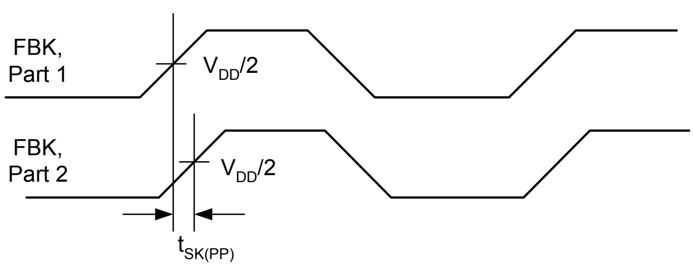
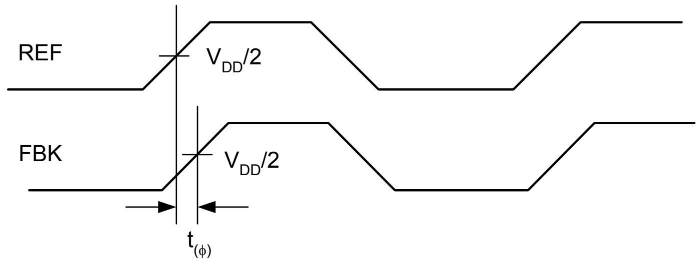


Figure 12. Phase Offset



XTAL Selection Criteria and Application Example

Selecting the appropriate XTAL ensures the FailSafe device is able to span an appropriate frequency of operation. Also, the XTAL parameters determine the holdover frequency stability. Critical parameters are given here. Cypress recommends that you choose:

- Low C0/C1 ratio (240 or less) so that the XTAL has enough range of pullability.
- Low temperature frequency variation
- Low manufacturing frequency tolerance
- Low aging

C0 is the XTAL shunt capacitance (3 pF to 7 pF typ).

C1 is the XTAL motional capacitance (10 fF to 30 fF typ).

The capacitive load as “seen” by the XTAL is across its terminals. It is named $C_{LOADMIN}$ (for minimum value), and $C_{LOADMAX}$ (for maximum value).These are used for calculating the pull range.

Note that the C_{LOAD} range “center” is approximately 20 pF, but we may not want a XTAL calibrated to that load. This is because the pullability is not linear, as represented in the equation below. Plotting the pullability of the XTAL shows this expected behavior as shown in Figure 13. In this example, specifying a XTAL calibrated to 14 pF load provides a balanced ppm pullability range around the nominal frequency.

Example:

$C_{LOADMIN}$ = (12 pF IC input cap + 0 pF pulling cap + 6 pF trace cap on board) / 2 = 9 pF

$C_{LOADMAX}$ = (12 pF IC input cap + 48 pF pulling cap + 6 pF trace cap on board) / 2 = 33 pF

Pull Range = $(fC_{LOADMIN} – fC_{LOADMAX}) / fC_{LOADMIN} = (C1 / 2) * [(1 / (C0 + C_{LOADMIN})) – (1 / (C0 + C_{LOADMAX}))]$

Pull Range in ppm = $(C1 / 2) * [(1 / (C0 + C_{LOADMIN})) – (1 / (C0 + C_{LOADMAX}))] * 10^6$

Figure 13. Frequency vs. C_{LOAD} Behavior for Example XTAL

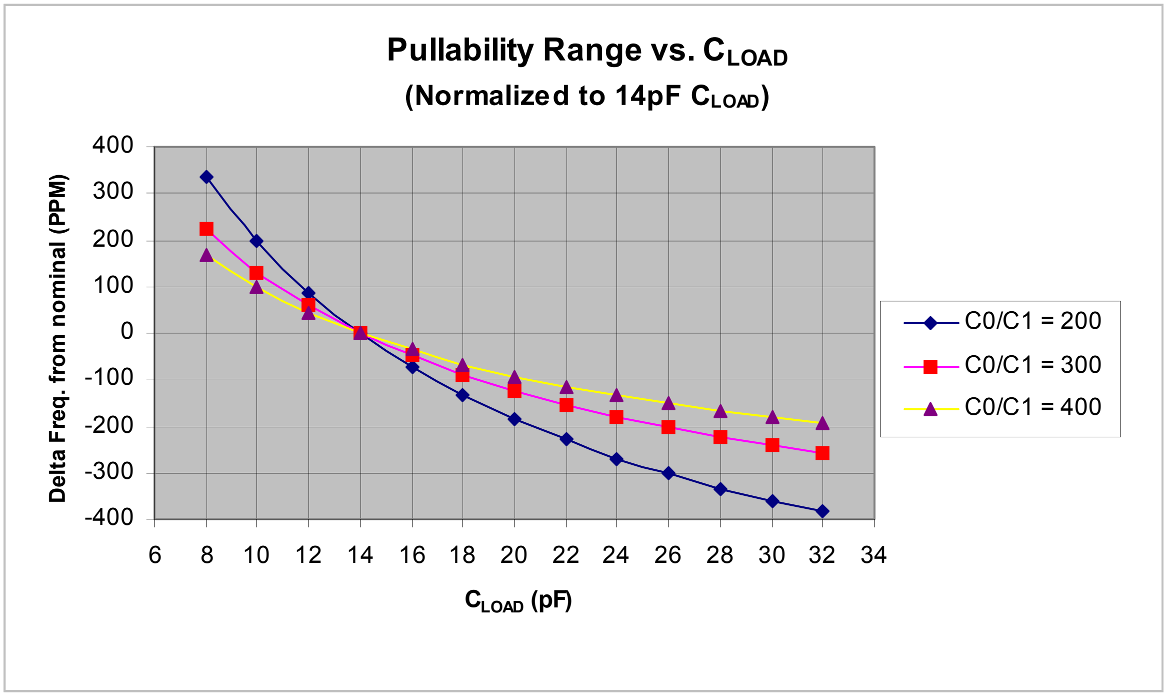


Table 4. Pullability Range from XTAL with Different C0/C1 Ratio

C0/C1 Ratio	$C_{LOADMIN}$	$C_{LOADMAX}$	Pullability Range	
200	8	32	–385	333
300	8	32	–256	222
400	8	32	–192	166

Calculated value of the pullability range for the XTAL with C0/C1 ratio of 200, 300, and 400 are shown in Table 4. For this calculation $C_{LOADMIN}$ = 8 pF and $C_{LOADMAX}$ = 32 pF is used. Using a XTAL that has a nominal frequency specified at load capacitance of 14 pF, almost symmetrical pullability range is obtained.

Next, it is important to calculate the pullability range including error tolerances. This is the **capture range** of the input reference frequency that the FailSafe device and XTAL combination can reliably span.

Calculating the **capture range** involves subtracting error tolerances as follows:

Parameter .... f error (ppm)

Manufacturing frequency tolerance 15

Temperature stability 30

Aging 3

Board/trace variation 5

Total 53

Example: Capture Range for XTAL with C0/C1 Ratio of 200

Negative Capture Range= –385 ppm + 53 ppm = –332 ppm

Positive Capture Range = 333 ppm – 53 ppm = +280 ppm

It is important to note that the XTAL with lower C0/C1 ratio has wider **pullability/capture range** as compared to the higher C0/C1 ratio. This helps to select the appropriate XTAL for use in the FailSafe application.

Absolute Maximum Conditions

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Parameter	Description	Condition	Min	Max	Unit
V_{DD}	Supply Voltage		–0.5	4.6	V
V_{IN}	Input Voltage	Relative to V_{SS}	–0.5	V_{DD} + 0.5	VDC
T_S	Temperature, Storage	Non Functional	–65	150	°C
T_J	Temperature, Junction	Functional	–	125	°C
ESD_{HBM}	ESD Protection (Human Body Model)	MIL-STD-883, Method 3015	2000	–	V
$Ø_{JC}$	Dissipation, Junction to Case	Mil-Spec 883E Method 1012.1	36.17		°C/W
$Ø_{JA}$	Dissipation, Junction to Ambient	JEDEC (JESD 51)	100.6		°C/W
UL–94	Flammability Rating	At 1/8 in.	V–0		
MSL	Moisture Sensitivity Level		1		

Multiple Supplies: The voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is NOT required.

Recommended Pullable Crystal Specifications[5]

Parameter	Name	Comments	Min	Typ	Max	Unit
F_{NOM}	Nominal crystal frequency	Parallel resonance, fundamental mode, AT cut	8.00	–	30.00	MHz
C_{LNOM}	Nominal load capacitance		–	14	–	pF
R_1	Equivalent series resistance (ESR)	Fundamental mode	–	–	25	Ω
R_3/R_1	Ratio of third overtone mode ESR to fundamental mode ESR	Ratio used because typical R_1 values are much less than the maximum spec	3	–	–	
DL	Crystal drive level	No external series resistor assumed	–	0.5	2	mW
F_{3SEPLI}	Third overtone separation from $3*F_{NOM}$	High side	300	–	–	ppm
F_{3SEPLO}	Third overtone separation from $3*F_{NOM}$	Low side	–	–	–150	ppm
C0	Crystal shunt capacitance		–	–	7	pF
C0/C1	Ratio of shunt to motional capacitance		180	–	250	
C1	Crystal motional capacitance		14.4	18	21.6	fF

Operating Conditions

Parameter	Description	Min	Max	Unit
V_{DDC}	3.3 V Supply Voltage	3.135	3.465	V
V_{DDA}, V_{DDB}	2.5 V Supply Voltage Range	2.375	2.625	V
	3.3 V Supply Voltage Range	3.135	3.465	V
T_A	Ambient Operating Temperature, Commercial	0	70	°C
	Ambient Operating Temperature, Industrial	–40	85	°C
C_L	Output Load Capacitance (Fout ≤ 100 MHz)	–	30	pF
	Output Load Capacitance (Fout > 100 MHz)	–	15	pF
C_{IN}	Input Capacitance (except XIN)	–	7	pF
C_{XIN}	Crystal Input Capacitance (all internal caps off)	10	13	pF
t_{PU}	Power up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	0.05	500	ms

Note

5. Ecliptek crystals ECX-5788-13.500M, ECX-5807-19.440M, ECX-5872-19.53125M, ECX-6362-18.432M, ECX-5808-27.000M, ECX-5884-17.664M, ECX-5883-16.384M, ECX-5882-19.200M, ECX-5880-24.576M meet these specifications.

DC Electrical Characteristics

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V_{IL}	Input Low Voltage	CMOS Levels, 30% of V_{DD}	–	–	0.3×V_{DD}	V
V_{IH}	Input High Voltage	CMOS Levels, 70% of V_{DD}	0.7×V_{DD}	–	–	V
I_{IL}	Input Low Current	$V_{IN} = V_{SS}$ (100k pull up only)	–	–	50	μA
I_{IH}	Input High Current	$V_{IN} = V_{DD}$ (100k pull down only)	–	–	50	μA
I_{OL}	Output Low Current	V_{OL} = 0.5 V, V_{DD} = 2.5 V	–	18	–	mA
		V_{OL} = 0.5 V, V_{DD} = 3.3 V	–	20	–	mA
I_{OH}	Output High Current	$V_{OH} = V_{DD}$ – 0.5 V, V_{DD} = 2.5 V	–	18	–	mA
		$V_{OH} = V_{DD}$ – 0.5 V, V_{DD} = 3.3 V	–	20	–	mA
I_{DDQ}	Quiescent Current	All Inputs grounded, PLL and DCXO in bypass mode, Reference Input = 0	–	–	250	μA

Switching Characteristics

Parameter[7]	Description	Test Conditions	Min	Typ	Max	Unit
f_{REF}	Reference Frequency	Commercial Grade	1.04	–	200	MHz
		Industrial Grade	1.04	–	166.7	MHz
f_{OUT}	Output Frequency	15 pF Load, Commercial Grade	1.70	–	200	MHz
		15 pF Load, Industrial Grade	1.70	–	166.7	MHz
f_{XIN}	DCXO Frequency		8.0	–	30	MHz
t_{DC}	Duty Cycle	Measured at $V_{DD}/2$	47	–	53	%
$t_{SR(I)}$	Input Slew Rate	Measured on REF1 Input, 30% to 70% of V_{DD}	0.5	–	4.0	V/ns
$t_{SR(O)}$	Output Slew Rate	Measured from 20% to 80% of V_{DD} = 3.3V, 15 pF Load	0.8	–	4.0	V/ns
		Measured from 20% to 80% of V_{DD} =2.5V, 15 pF Load	0.4	–	3.0	V/ns
$t_{SK(O)}$	Output to Output Skew	All outputs equally loaded, measured at $V_{DD}/2$	–	110	200	ps
$t_{SK(IB)}$	Intrabank Skew	All outputs equally loaded, measured at $V_{DD}/2$	–	–	75	ps
$t_{SK(PP)}$	Part to Part Skew	Measured at $V_{DD}/2$	–	–	500	ps
$t_{(\phi)}$[6]	Static Phase Offset	Measured at $V_{DD}/2$	–	–	250	ps
$t_{D(\phi)}$[6]	Dynamic Phase Offset	Measured at $V_{DD}/2$	–	–	500	ps
$t_{J(CC)}$	Cycle-to-Cycle Jitter	Load = 15 pF, $f_{OUT} \geq$ 6.25 MHz	–	100	200	ps
			–	18	35	ps_{RMS}
t_{LOCK}	Lock Time	At room temperature with 18.432 MHz Crystal	–	70	–	ms

Ordering Information

Part Number	Package Type	Product Flow
Pb-free		
CY23FS08OXI	28-pin SSOP	Industrial, –40 °C to 85 °C
CY23FS08OXIT	28-pin SSOP – Tape and Reel	Industrial, –40 °C to 85 °C
CY23FS08OXC	28-pin SSOP	Commercial, 0 °C to 70 °C
CY23FS08OXCT	28-pin SSOP – Tape and Reel	Commercial, 0 °C to 70 °C

Notes
6. The $t_{(\phi)}$ reference feedback input delay is guaranteed for a maximum 4:1 input edge ratio between the two signals as long as $t_{SR(I)}$ is maintained.
7. Parameters guaranteed by design and characterization, not 100% tested in production.

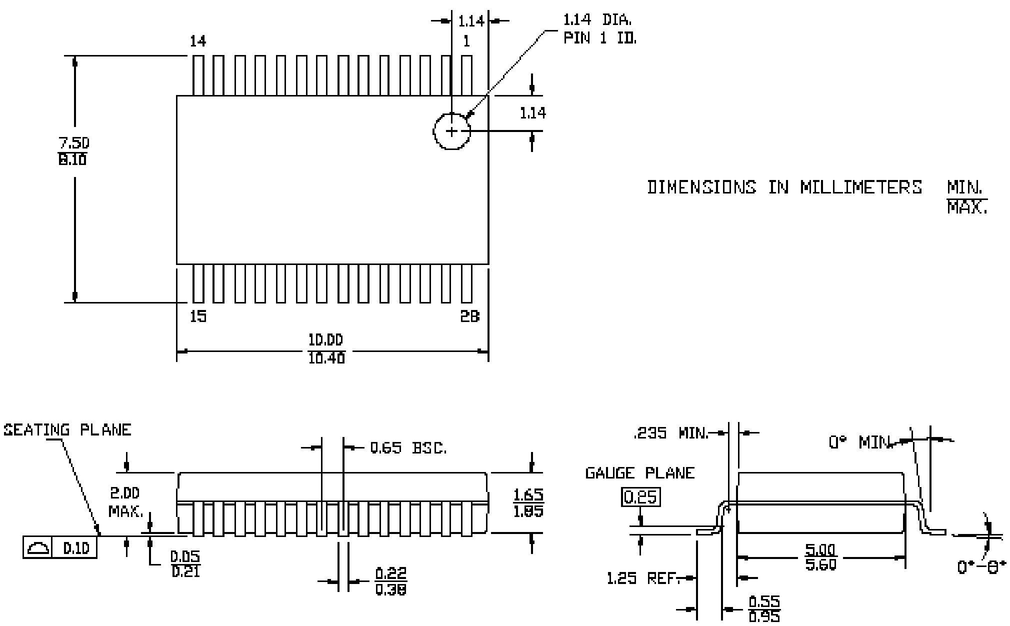
Ordering Code Definition

CY23FS08 OX X (T)

- (T) — Package type: T = tape and reel, blank = tube
- X — Temperature code: C = Commercial, I = Industrial
- OX — Package: 28-pin SSOP, Pb-free
- CY23FS08 — Device number

Package Diagram

Figure 14. 28-pin (5.3 mm) Shrunk Small Outline Package SP28



51-85079 *D

Acronyms

Acronym	Description
DCXO	digitally controlled crystal oscillator
ESD	electrostatic discharge
PLL	phase locked loop
RMS	root mean square
SSOP	shrunk small outline package
XTAL	crystal

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	micro Amperes
mA	milli Amperes
ms	milli seconds
MHz	Mega Hertz
ns	nano seconds
pF	pico Farad
ps	pico seconds
ppm	parts per million
W	Watts
Ω	ohms
V	Volts

Document History Page

Document Title: CY23FS08 Failsafe™ 2.5 V/3.3 V Zero Delay Buffer Document Number: 38-07518				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	123699	04/23/03	RGL	New Data Sheet
*A	224067	See ECN	RGL/ZJX	Changed the XTAL Specifications table.
*B	276749	See ECN	RGL	Removed (T_{LOCK}) Lock Time Specification.
*C	417645	See ECN	RGL	Added Lead-free devices Added typical nos. on jitters
*D	2865396	01/25/2010	KVM	Remove figures showing dynamic response to 180° phase change to REF Add waveforms for input slew rate and intrabank skew Change “Cl” to “C_{LOAD}” Absolute Maximum Conditions table: remove duplicate T_A parameter Replace crystal ECX–5806–18.432M with ECX–6362–18.432M Remove obsolete part numbers CY23FS08OI, CY23FS08OIT, CY23FS08OC and CY23FS08OCT Replace “Lead-free” with “Pb-free” Remove unreferenced footnote 9 Change package drawing title from “O28” to “SP28”, updated package diagram Added Table of Contents
*E	2925613	04/30/10	KVM	Posting to external web.
*F	3130032	01/06/2011	BASH	Changed $t_{D(\phi)}$ max value from 200 to 500 and removed $t_{D(\phi)}$ Typical value in Switching Characteristics on page 11. Added Ordering Code Definition. Added Acronyms and Units of Measure on page 13.

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