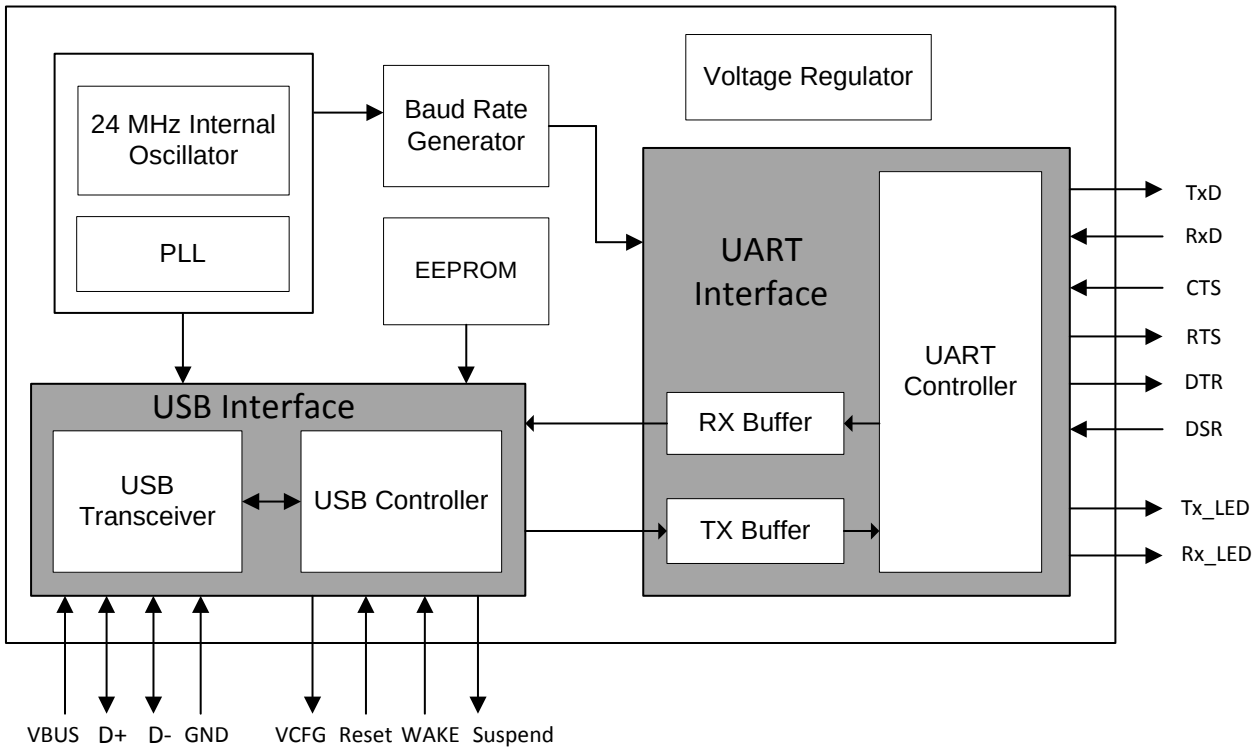
CY7C64225

USB to UART Bridge Controller

Features

- USB 2.0 Full-Speed (12 Mbps) USB to UART controller
- No programming required
- Supports Bus/Self powered configurations
- Software enabled configurations for
  - VID / PID
  - Product string descriptor
  - Manufacturer string descriptor
  - Bus / Self powered
  - Remote wakeup
  - Power consumption
- Integrated 64-byte transmit and 64-byte receive buffer
- Integrated EEPROM, oscillator, USB termination resistors and regulator for low-cost designs
- Integrated EEPROM for saving device description and configuration.
- LED drivers to indicate activity on Transmit and Receive lines
- Modulated LED output to save power
- Automatic suspend mode for low power consumption
- USB Endpoints
  - 1 interrupt endpoint
  - 1 Bulk-in and 1 Bulk-out endpoint
- No external crystal required
- Universal Asynchronous Receiver / Transceiver (UART)
  - Data transfer rates of 300 to 115200 baud
  - Data format: 8 data bits, 1 stop bit, no parity
  - Software selectable handshaking. CTS, RTS, DTR, DSR
- Device Drivers
  - Works with existing PC applications that support COM port communications
  - Royalty free Virtual COM Port (VCP) driver
  - Windows 7 / Vista / XP / 2000
- Single Supply Operation
  - 3.15 to 3.5 V
  - 4.35 to 5.25 V for bus-powered low cost designs
- Commercial operating temperature range: 0 ℃ to +70 ℃
- Available in 28-pin SSOP package

Block Diagram



Contents

Applications

- USB to UART cables
- Enable USB connectivity in legacy peripherals with UART
- Point of Service (POS) terminal printers
- Industrial and Metering devices

CY7C64225 Functional Overview

Introduction

The CY7C64225 is a fully integrated USB-to-UART Bridge that provides a simple way of updating RS-232 based devices to USB with a minimal number of components. The CY7C64225 includes a USB 2.0 Full-Speed controller, a UART transceiver, internal regulator, internal oscillator and internal EEPROM in a 28-pin SSOP package.

The internal EEPROM can be used to program customer specific information for OEM applications. This is done in-system via USB.

Royalty free Virtual COM Port (VCP) device drivers are provided by Cypress Semiconductor. This allows the device to appear as a COM port to PC applications. All UART signals including the handshaking and control signals are implemented.

Operational Details

Suspend and Resume

An active low on Suspend (pin 3) indicates that the USB Bus is suspended. This is used to put the CY7C64225 and other external devices in low power mode. The device can resume normal operations if,

- Activity is detected on the USB
- Or reset signal is detected

WAKE

When the device is in suspend. If Remote wakeup is enabled then asserting this signal generates remote wakeup signaling on the upstream. If acknowledged by the host the device will resume normal operation.

Reset and Activity Indicators

A high assertion on the Reset (pin 6) resets the device.

Tx_LED (pin 2) and Rx_LED (pin 27) are active low and sink a maximum current of 25 mA.

VCFG

An active low on the VCFG (pin 26) indicates that the VBUS is detected and the device is configured.

VBUS

A 1 kΩ resistor in series is required with VBUS (pin 7). This pin is used for VBUS monitoring in self-power applications.

Asynchronous Serial Data Bus (UART) Interface

The UART Bus consists of TxD (transmit) and RxD (receive) lines in addition to software selectable handshaking using DSR, DTR, RTS, CTS.

Baud rates supported are: 300, 600, 1200, 1800, 2400, 4800, 7200, 9600, 14400, 19200, 28800, 38400, 56000, 57600 and 115200.

The baud rate is configured through the USB interface by the driver.

Configurations

The internal EEPROM may be used to customize the values shown in the table below.

Name	Default Value
VID / PID	0x04B4 / 0x0008
Manufacturer string descriptor	2011 Cypress Semiconductor
Product string descriptor	Cypress-USB2UART-0123456
Bus/Self Powered	Self
Remote Wakeup	Yes
Power Consumption	100 mA

A free configuration utility is provided to configure parameters in above table to meet application specific requirements.

Driver

PC software can access a CY7C64225 based device as a Virtual COM Port. However the actual data is transferred over the USB interface. This allows existing COM Port based applications to communicate via USB to a CY7C64225 device without requiring any changes to the software.

This serves the following purpose

- Add an extra UART port to the PC
- Add UART port to PCs without UART port
- Facilitate easy migration for systems which have a free USB port and need an additional UART port

Pin Configuration

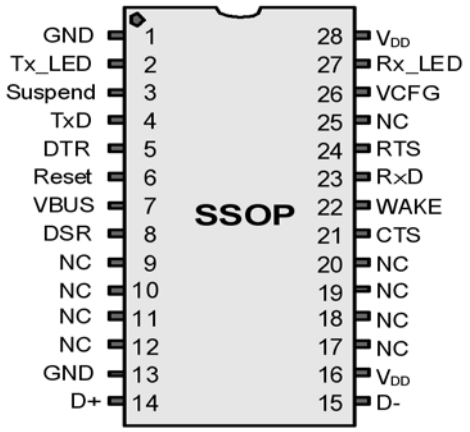
28-pin part pinout Description

The CY7C64225 USB-to-UART Bridge device is available in a 28-pin package that is listed and illustrated in the following table.

Table 1. 28-pin part pinout (SSOP)

Pin No.	Name	I/O	Description
1	GND	Power	Ground
2	Tx_LED	Output	Active low, UART Tx_LED, max current –20 mA
3	Suspend	Output	Active low indicates USB is suspended
4	TxD	Output	UART Data Transmit, Output
5	DTR	Output	Data Terminal Ready (DTR) Pin
6	Reset	Input	Active high on this pin resets the device
7	VBUS	Input	USB VBUS input.Used for VBUS monitoring. This pin requires a 1 kΩ resistor in series when connected to VBUS.
8	DSR	Input	Data Set Ready (DSR) pin
13	GND	Power	USB Ground
14	D+	USB	USB D+ Line
15	D–	USB	USB D– Line
16	V_{DD}	Power	Supply Voltage. 3.3 V or 5 V
21	CTS	Input	Clear to Send (CTS) input, handshake signal
22	WAKE	Input	Active high on this pin, generates remote wakeup on the Bus
23	RxD	Input	UART Data Receive, Input
24	RTS	Output	Request to Sent (RTS) output, handshake signal
26	VCFG	Output	Active low indicates VBUS is detected and device is configured
27	Rx_LED	Output	Active low, UART Rx_LED, max current –20 mA
28	V_{DD}	Power	Supply Voltage. 3.3 V or 5 V
9	NC	NC	No Connect
10	NC	NC	No Connect
11	NC	NC	No Connect
12	NC	NC	No Connect
17	NC	NC	No Connect
18	NC	NC	No Connect
19	NC	NC	No Connect
20	NC	NC	No Connect
25	NC	NC	No Connect

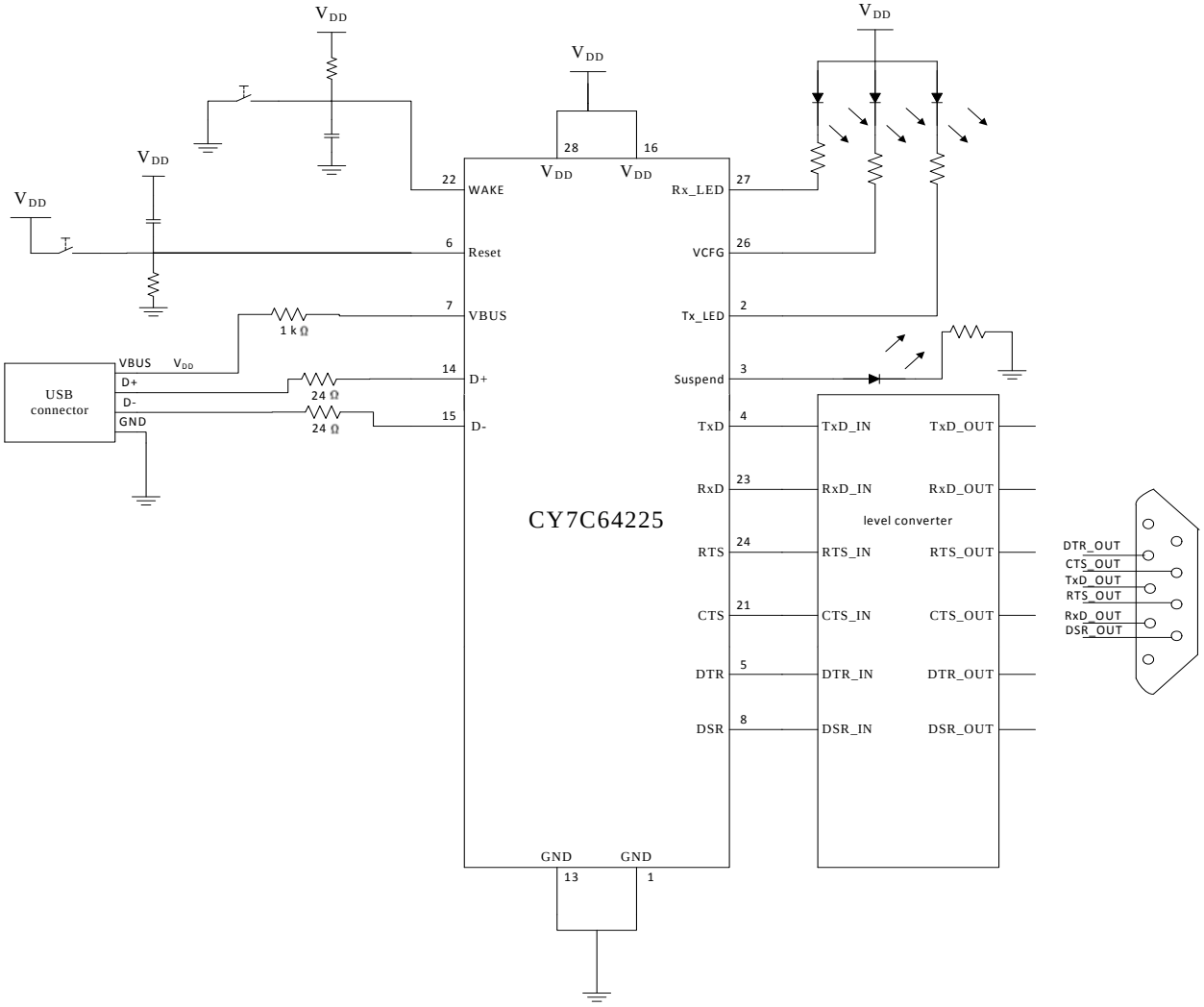
Figure 1. 28-pin SSOP USB-UART Bridge Device



Application Diagram

The USB-to-UART bridge sits between an embedded system and a host PC/embedded host. The embedded system connects to the bridge through a standard UART. The PC connects to the bridge through the USB. From the perspective of the embedded system, the bridge presents a PC UART port. From the perspective of the application software on the host PC, the bridge enumerates as a UART.

The following diagram provides systems connection diagram for CY7C64225.

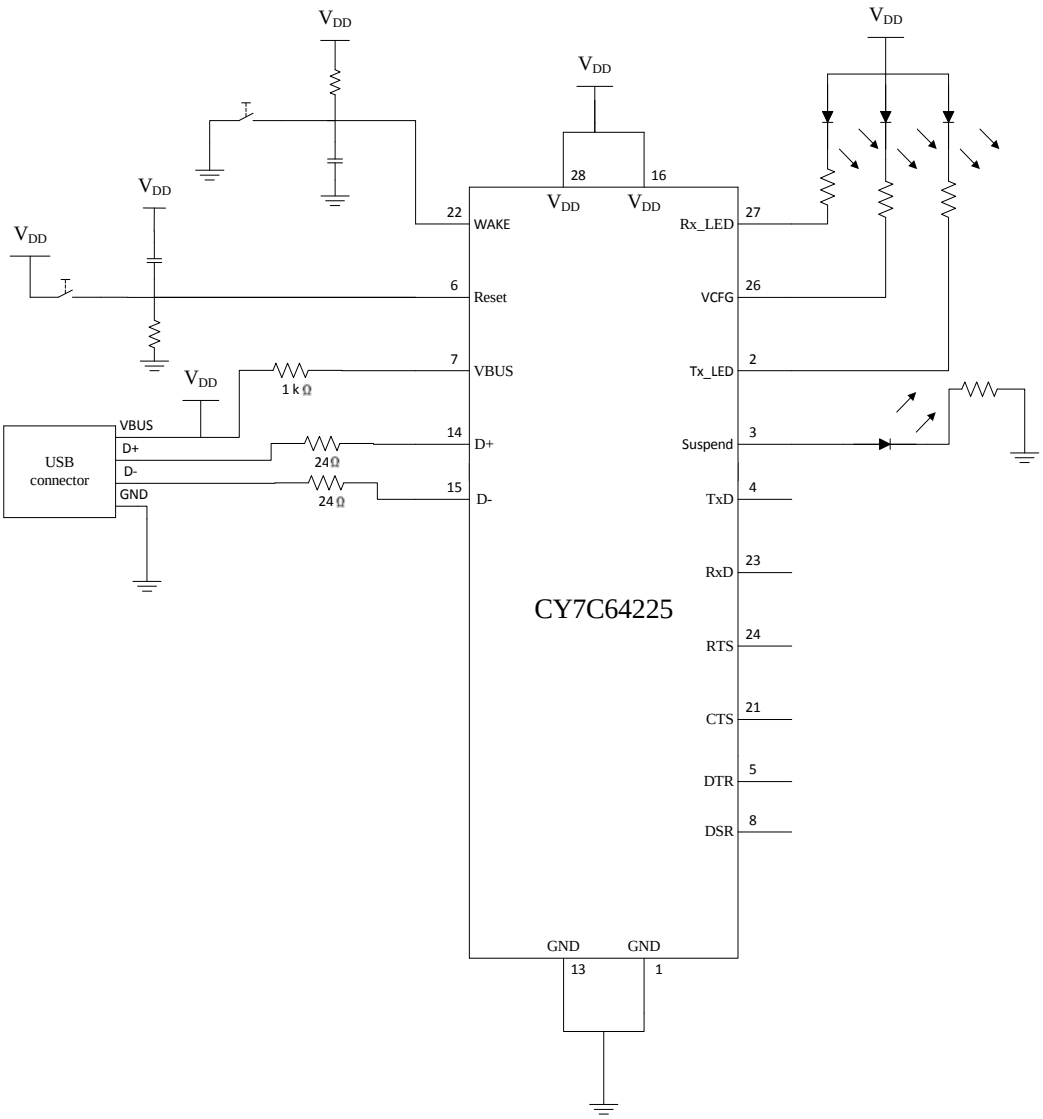


Application Circuits

The following diagrams illustrates typical application schematics circuits.

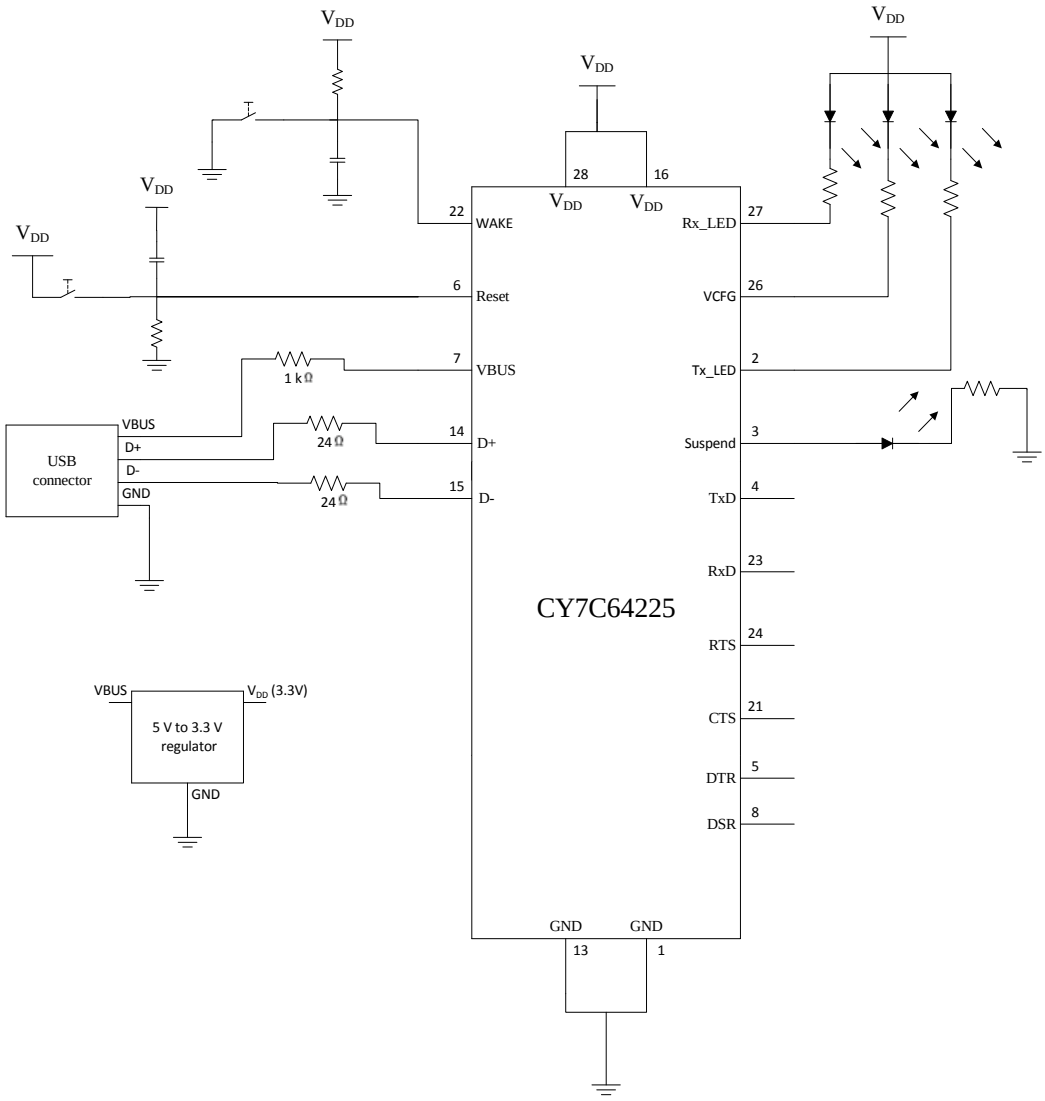
Bus Powered Design

Diagram below provides example schematics to use CY7C64225 in bus powereddesign.The design uses the internal regulator hence it operates with VBUS as the single power supply.



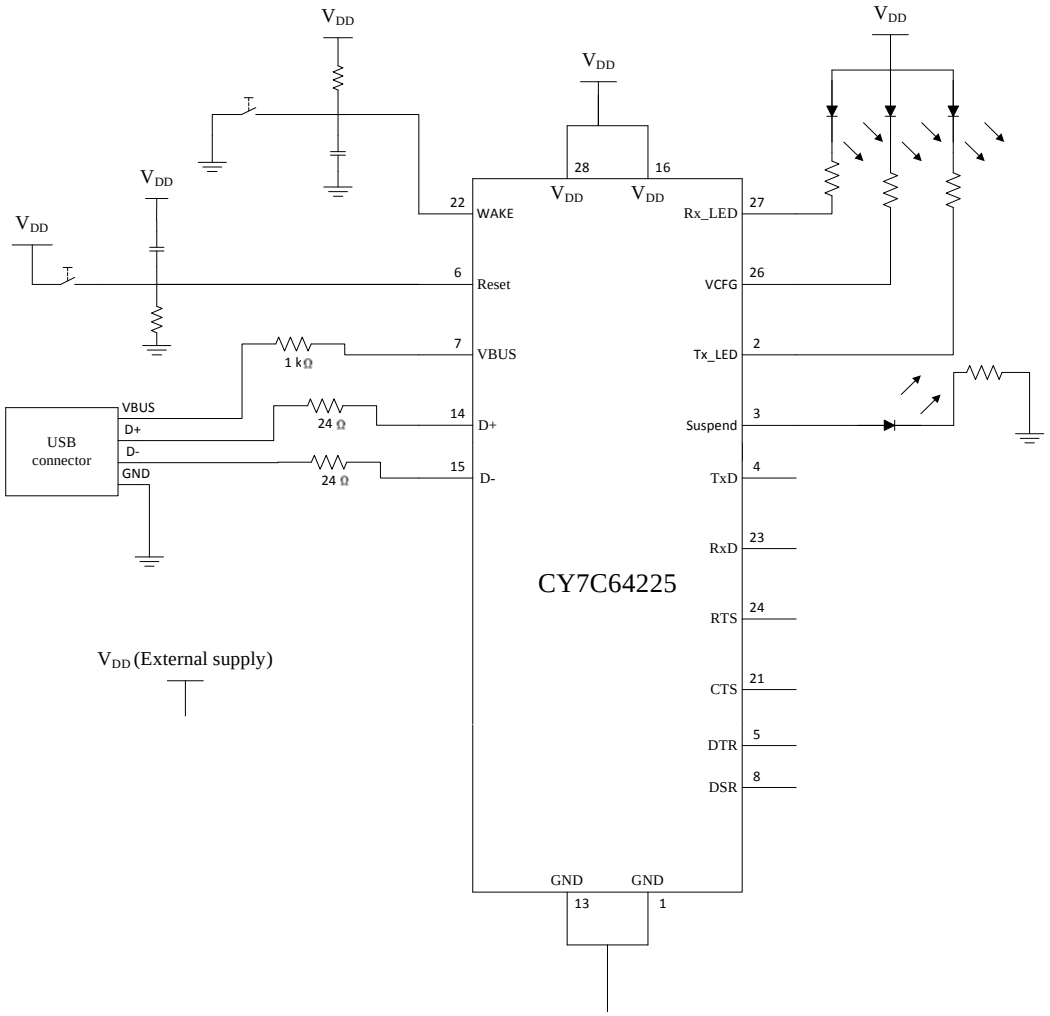
Bus Powered Design using External Regulator

The following diagram provides example schematics to use CY7C64225 in bus powered design using a external regulator. The design has a 5 V (VBUS has range of 4.75 to 5.25) to 3.3 V regulator hence CY7C64225 uses the 3.3 V regulator output as the single power supply. This is used in designs that already have a 3.3 V supply for other components on the board.



Self Powered Design

The following diagram provides example schematics to use CY7C64225 in self-powered design.Here the V_{DD} (5 V or 3.3 V) is obtained from an external power supply. This is used in designs that already have a 5 V or 3.3 V onboard supply. In self-powered designs VBUS pin is used for VBUS monitoring.



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Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{STG}	Storage temperature	–55	–	+100	℃	Higher storage temperatures reduces data retention time.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	℃	–
$T_{BAKETIME}$	Bake time	See package label	–	72	Hours	–
T_A	Ambient temperature with power applied	0	–	+70	°C	–
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	–
V_{IO}	DC input voltage	V_{SS} – 0.5	–	V_{DD} + 0.5	V	–
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	–
ESD	Electrostatic discharge voltage	–	–	2000	V	Human body model ESD.
$EEPROM_{ENPB}$	EEPROM endurance (per block)	50,000[1]	–	–	–	Erase/write cycles per block.
$EEPROM_{ENT}$	EEPROM endurance (total)[2]	1,800,000	–	–	–	Erase/write cycles.
$EEPROM_{DR}$	EEPROM data retention	10	–	–	Years	–

Operating Temperature

Table 3. Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{AC}	Commercial ambient temperature	0	–	+70	°C	–
T_J	Junction temperature	–40	–	+100	℃	The temperature rise from ambient to junction is package specific. See Thermal Impedance on page 12. The user must limit the power consumption to comply with this requirement.

Notes

1. The 50,000 cycle EEPROM endurance per block will only be guaranteed if the EEPROM is operating within one voltage range. Voltage ranges are 3.0 V to 3.6 V and 4.75 V to 5.25 V.
2. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).

DC Electrical Characteristics

DC GPIO Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and 0 °C ≤ T_A ≤ 70 °C, or 3.15 V to 3.5 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 4. DC GPIO Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{OH}	High output level	V_{DD} – 1.0	–	–	V	I_{OH} = 10 mA, V_{DD} = 4.75 to 5.25 V
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 25 mA, V_{DD} = 4.75 to 5.25 V
I_{OH}	High-level source current	10	–	–	mA	–
I_{OL}	Low-level sink current	25	–	–	mA	–
V_{IL}	Input low level	–	–	0.8	V	V_{DD} = 3.15 to 5.25 V
V_{IH}	Input high level	2.1	–		V	V_{DD} = 3.15 to 5.25 V

DC Full-Speed USB Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and 0 °C ≤ T_A ≤ 70 °C, or 3.15 V to 3.5 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

Table 5. DC Full Speed (12 Mbps) USB Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
USB Interface						
V_{DI}	Differential input sensitivity	0.2	–	–	V	| (D+) – (D–) |
V_{CM}	Differential input common mode range	0.8	–	2.5	V	–
V_{SE}	Single-ended receiver threshold	0.8	–	2.0	V	–
C_{IN}	Transceiver capacitance	–	–	20	pF	–
I_{IO}	High Z state data line leakage	–10	–	10	µA	0 V < V_{IN} < 3.3 V.
R_{EXT}	External USB series resistor	23	–	25	Ω	In series with each USB pin.
V_{UOH}	Static output high, driven	2.8	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOHI}	Static output high, idle	2.7	–	3.6	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
V_{UOL}	Static output low	–	–	0.3	V	15 kΩ ± 5% to ground. Internal pull-up enabled.
Z_O	USB driver output impedance	28	–	44	Ω	Including R_{EXT} resistor.
V_{CRS}	D+/D– crossover voltage	1.3	–	2.0	V	–

DC Chip Level Specifications

The following table lists guaranteed maximum and minimum specifications for the voltage and temperature ranges when the IMO is selected as system clock: 4.75 V to 5.25 V and 0 °C ≤ T_A ≤ 70 °C, or 3.15 V to 3.5 V and 0 °C ≤ T_A ≤ 70 °C, respectively. Typical parameters apply to 5 V and 3.3 V at 25 °C and are for design guidance only.

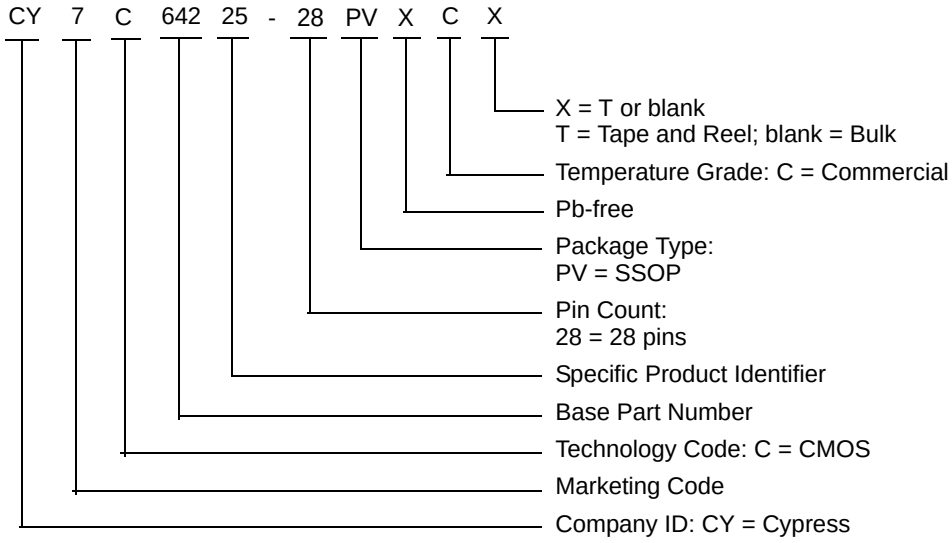
Table 6: DC Chip-Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
V_{DD}	Supply voltage	3.0	–	5.25	V	USB hardware is not functional when V_{DD} is between 3.5 V to 4.35 V
I_{DD5}	Supply current	–	14	27	mA	Conditions are V_{DD} = 5.0 V, T_A = 25 ℃
I_{DD3}	Supply current	–	8	14	mA	Conditions are V_{DD} = 3.3 V, T_A = 25 ℃
I_{SB}	Sleep (mode) current	–	3	6.5	µA	V_{DD} = 3.3 V, 0 ℃ ≤ T_A ≤ 55 ℃
I_{SBH}	Sleep (mode) current at high temperature.	–	4	25	µA	V_{DD} = 3.3 V, 55 ℃ < T_A ≤ 70 ℃
I_{susp1}	USB suspend current	–	232	345	µA	For 5 V operating voltage range
I_{susp2}	USB suspend current	–	207	258	µA	For 3.3 V operating voltage range

Ordering Information

Package	Ordering Code	Temperature Range
28-pin SSOP	CY7C64225-28PVXC	0 ℃ to 70 ℃
28-pin SSOP (Tape and Reel)	CY7C64225-28PVXCT	0 ℃ to 70 ℃

Ordering Code Definitions

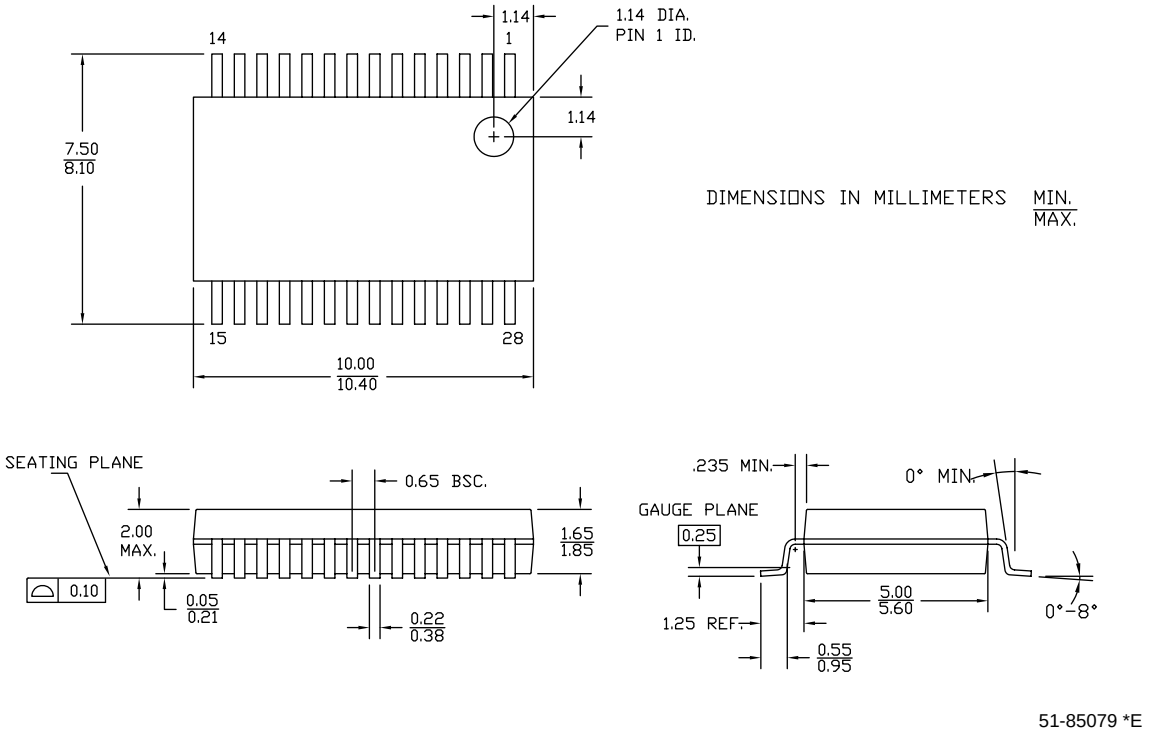


Packaging Information

This section illustrates the package specification for the CY7C64225, along with the thermal impedance for the package.

Package Diagrams

Figure 2. 28-pin SSOP (210 Mils) O28.21 Package Outline, 51-85079



51-85079 *E

Thermal Impedance

Table 7. Thermal Impedance for the Package

Package	Typical θ_{JA}
28-pin SSOP	96 °C/W

Note Assumes 2-layer PCB

Solder Reflow Peak Temperature

Following is the minimum solder reflow peak temperature to achieve good solderability.

Table 8. Solder Reflow Peak Temperature

Package	Maximum Peak Temperature	Time at Maximum Peak Temperature
28-pin SSOP	260 °C	20 s

Acronyms

The following table lists the acronyms used in this document.

Acronym	Description
DC	direct current
EEPROM	electrically erasable programmable read-only memory
GPIO	general purpose input/output
I/O	input/output
LED	light emitting diode
PC	personal computer
SSOP	shrink small outline package
UART	universal asynchronous receiver / transmitter
USB	universal serial bus

Reference Documents

USB 2.0 Specification

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kΩ	kilohm
µA	microampere
mA	milliampere
Ω	ohm
%	percent
s	second
V	volt
W	watt

Glossary

Asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
Buffer	1. A storage area for data that is used to compensate for a speed difference, when transferring data from one device to another. Usually refers to an area reserved for I/O operations, into which data is read, or from which data is written. 2. A portion of memory set aside to store data, often before it is sent to an external device or as it is received from an external device. 3. An amplifier used to lower the output impedance of a system.
EEPROM	Electrically Erasable Programmable Read-Only Memory and is a type of non-volatile memory used to store small amounts of data that must be saved when power is removed.
Reset	An active high signal that is driven into the device. It causes all operations of the CPU to stop and return to a pre-defined state.
V_{DD}	A name for a power net meaning “voltage drain” The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning “voltage source” The most negative power supply signal.
Virtual COM Port	A USB virtual COM port is a software interface that enables applications to access a USB device as if it were a built-in serial port. Many USB virtual COM-port devices function as bridges that convert between USB and RS-232 or other asynchronous serial interfaces.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.

Document History Page

Document Title: CY7C64225, USB to UART Bridge Controller Document Number: 001-76294				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	3533464	02/23/2012	HBM	New datasheet.
*A	3571321	05/15/2012	AASI	Added Application Circuit Diagrams. Minor content edits to add clarity. Updated DC Chip Level Specifications and Table 6.

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