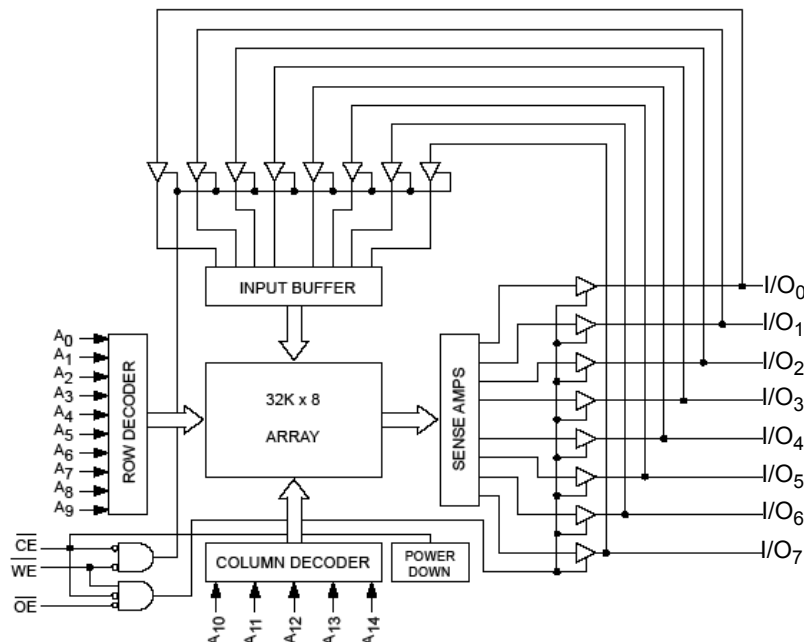


## Features

- Temperature ranges
  - $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Pin and function compatible with CY7C199C
- High speed
  - $t_{AA} = 10\text{ ns}$
- Low active power
  - $I_{CC} = 80\text{ mA}$  at  $10\text{ ns}$
- Low CMOS standby power
  - $I_{SB2} = 3\text{ mA}$
- 2.0 V data retention
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed/power
- Transistor-transistor logic (TTL) compatible inputs and outputs
- Easy memory expansion with  $\overline{\text{CE}}$  and  $\overline{\text{OE}}$  features
- Available in Pb-free 28-pin 300-Mil-wide molded small outline J-lead package (SOJ) and 28-pin thin small outline package (TSOP) I packages

## Logic Block Diagram



## Functional Description

The CY7C199D is a high performance CMOS static RAM organized as 32,768 words by 8-bits. Easy memory expansion is provided by an active LOW chip enable ( $\overline{\text{CE}}$ ), an active LOW output enable ( $\overline{\text{OE}}$ ) and tri-state drivers. This device has an automatic power-down feature, reducing the power consumption when deselected. The input and output pins ( $I/O_0$  through  $I/O_7$ ) are placed in a high impedance state when the device is deselected ( $\overline{\text{CE}}$  HIGH), the outputs are disabled ( $\overline{\text{OE}}$  HIGH), or during a write operation ( $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW).

Write to the device by taking chip enable ( $\overline{\text{CE}}$ ) and write enable ( $\overline{\text{WE}}$ ) inputs LOW. Data on the eight I/O pins ( $I/O_0$  through  $I/O_7$ ) is then written into the location specified on the address pins ( $A_0$  through  $A_{14}$ ).

Read from the device by taking chip enable ( $\overline{\text{CE}}$ ) and output enable ( $\overline{\text{OE}}$ ) LOW while forcing write enable ( $\overline{\text{WE}}$ ) HIGH. Under these conditions, the contents of the memory location specified by the address pins appears on the I/O pins.

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### Pin Configuration

Figure 1. 28-pin SOJ (Top View)

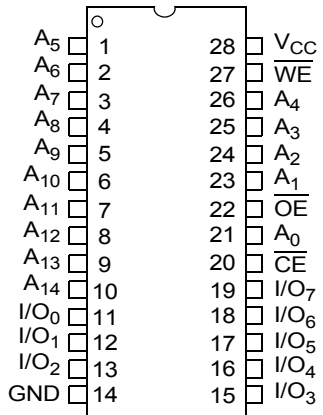
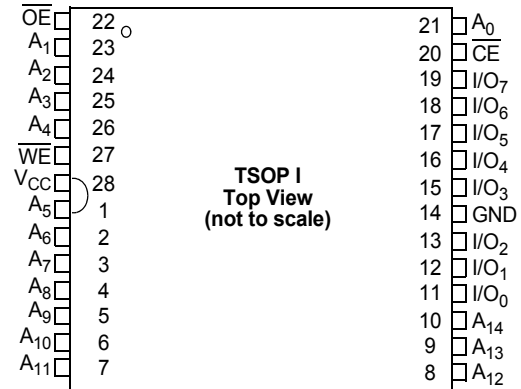


Figure 2. 28-pin TSOP I (Top View)



### Selection Guide

Description	-10 (Industrial)	Unit
Maximum access time	10	ns
Maximum operating current	80	mA
Maximum CMOS standby current	3	mA

## Maximum Ratings

Exceeding the maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage temperature .....	-65 °C to +150 °C
Ambient temperature with power applied .....	-55 °C to +125 °C
Supply voltage on $V_{CC}$ to relative GND <sup>[1]</sup> .....	-0.5 V to +6.0 V
DC voltage applied to outputs in high Z State <sup>[1]</sup> .....	-0.5 V to $V_{CC} + 0.5$ V

DC input voltage <sup>[1]</sup> .....	-0.5 V to $V_{CC} + 0.5$ V
Output current into outputs (LOW) .....	20 mA
Static discharge voltage .....	> 2,001 V (per MIL-STD-883, method 3015)
Latch-up current .....	> 140 mA

## Operating Range

Range	Ambient Temperature	$V_{CC}$	Speed
Industrial	-40 °C to +85 °C	5 V ± 0.5 V	10 ns

## Electrical Characteristics

Over the operating range

Parameter	Description	Test Conditions	CY7C199D-10		Unit	
			Min	Max		
$V_{OH}$	Output HIGH voltage	$I_{OH} = -4.0$ mA	2.4	-	V	
$V_{OL}$	Output LOW voltage	$I_{OL} = 8.0$ mA	-	0.4	V	
$V_{IH}$	Input HIGH voltage <sup>[1]</sup>		2.2	$V_{CC} + 0.5$	V	
$V_{IL}$	Input LOW voltage <sup>[1]</sup>		-0.5	0.8	V	
$I_{IX}$	Input leakage current	$GND \leq V_I \leq V_{CC}$	-1	+1	µA	
$I_{OZ}$	Output leakage current	$GND \leq V_O \leq V_{CC}$ , output disabled	-1	+1	µA	
$I_{CC}$	$V_{CC}$ operating supply current	$V_{CC} = V_{CC(max)}$ , $I_{OUT} = 0$ mA, $f = f_{max} = 1/t_{RC}$	100 MHz	-	80	mA
			83 MHz	-	72	mA
			66 MHz	-	58	mA
			40 MHz	-	37	mA
$I_{SB1}$	Automatic CE power-down current— TTL Inputs	$V_{CC} = V_{CC(max)}$ , $\overline{CE} \geq V_{IH}$ , $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$ , $f = f_{max}$	-	10	mA	
$I_{SB2}$	Automatic CE power-down current— CMOS Inputs	$V_{CC} = V_{CC(max)}$ , $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V or $V_{IN} \leq 0.3$ V, $f = 0$	-	3	mA	

### Note

- $V_{IL(min)} = -2.0$  V and  $V_{IH(max)} = V_{CC} + 1$  V for pulse durations of less than 5 ns.

### Capacitance

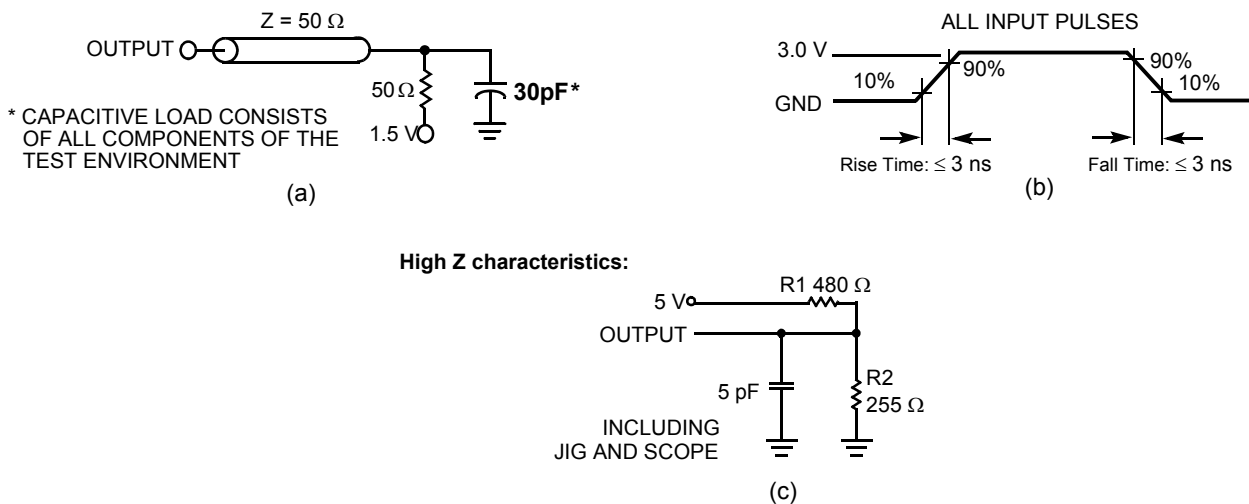
Parameter [2]	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input capacitance	T <sub>A</sub> = 25 °C, f = 1 MHz, V <sub>CC</sub> = 5.0 V	8	pF
C <sub>OUT</sub>	Output capacitance		8	pF

### Thermal Resistance

Parameter [2]	Description	Test Conditions	28-pin SOJ	28-pin TSOP I	Unit
Θ <sub>JA</sub>	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, four-layer printed circuit board	59.16	54.65	°C/W
Θ <sub>JC</sub>	Thermal resistance (junction to case)		40.84	21.49	°C/W

### AC Test Loads and Waveforms

Figure 3. AC Test Loads and Waveforms [3]



**Notes**

2. Tested initially and after any design or process changes that may affect these parameters.
3. AC characteristics (except high Z) are tested using the load conditions shown in Figure 3 (a). High Z characteristics are tested for all speeds using the test load shown in Figure 3 (c).

## Switching Characteristics

Over the operating range

Parameter <sup>[4]</sup>	Description	CY7C199D-10		Unit
		Min	Max	
<b>Read Cycle</b>				
$t_{power}^{[5]}$	$V_{CC(ypical)}$ to the first access	100	–	$\mu s$
$t_{RC}$	Read cycle time	10	–	ns
$t_{AA}$	Address to data valid	–	10	ns
$t_{OHA}$	Data hold from address change	3	–	ns
$t_{ACE}$	$\overline{CE}$ LOW to data valid	–	10	ns
$t_{DOE}$	$\overline{OE}$ LOW to data valid	–	5	ns
$t_{LZOE}^{[6]}$	$\overline{OE}$ LOW to low Z	0	–	ns
$t_{HZOE}^{[6, 7]}$	$\overline{OE}$ HIGH to high Z	–	5	ns
$t_{LZCE}^{[6]}$	$\overline{CE}$ LOW to low Z	3	–	ns
$t_{HZCE}^{[6, 7]}$	$\overline{CE}$ HIGH to high Z	–	5	ns
$t_{PU}^{[8]}$	$\overline{CE}$ LOW to power-up	0	–	ns
$t_{PD}^{[8]}$	$\overline{CE}$ HIGH to power-down	–	10	ns
<b>Write Cycle <sup>[9, 10]</sup></b>				
$t_{WC}$	Write cycle time	10	–	ns
$t_{SCE}$	$\overline{CE}$ LOW to write end	7	–	ns
$t_{AW}$	Address setup to write end	7	–	ns
$t_{HA}$	Address hold from write end	0	–	ns
$t_{SA}$	Address setup to write start	0	–	ns
$t_{PWE}$	$\overline{WE}$ pulse width	7	–	ns
$t_{SD}$	Data setup to write end	6	–	ns
$t_{HD}$	Data hold from write end	0	–	ns
$t_{HZWE}^{[6]}$	$\overline{WE}$ LOW to high Z	–	5	ns
$t_{LZWE}^{[6, 7]}$	$\overline{WE}$ HIGH to low Z	3	–	ns

### Notes

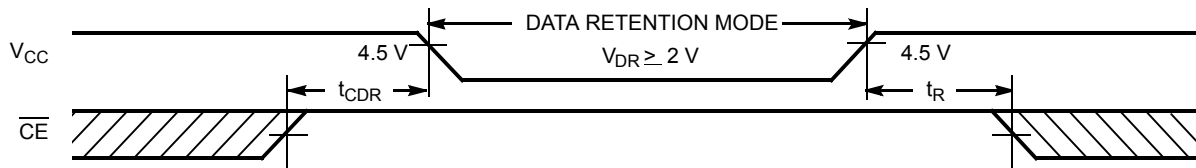
- Test conditions assume signal transition time of 3 ns or less for all speeds, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified  $I_{OL}/I_{OH}$  and 30-pF load capacitance.
- $t_{POWER}$  gives the minimum amount of time that the power supply should be at typical  $V_{CC}$  values until the first memory access can be performed.
- At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
- $t_{HZOE}$ ,  $t_{HZCE}$ , and  $t_{HZWE}$  are specified with  $C_L = 5$  pF as in part (b) of [Figure 3 on page 5](#). Transition is measured  $\pm 200$  mV from steady-state voltage.
- This parameter is guaranteed by design and is not tested.
- The internal write time of the memory is defined by the overlap of  $\overline{CE}$  LOW and  $\overline{WE}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- The minimum write cycle time for Write Cycle No. 3 ( $\overline{WE}$  controlled,  $\overline{OE}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .

### Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Max	Unit
$V_{DR}$	$V_{CC}$ for data retention		2.0	–	V
$I_{CCDR}$	Data retention current	$V_{CC} = V_{DR} = 2.0\text{ V}$ , $\overline{CE} \geq V_{CC} - 0.3\text{ V}$ , $V_{IN} \geq V_{CC} - 0.3\text{ V}$ or $V_{IN} \leq 0.3\text{ V}$	–	3	mA
$t_{CDR}^{[11]}$	Chip deselect to data retention time		0	–	ns
$t_R^{[12]}$	Operation recovery time		15	–	ns

### Data Retention Waveform



### Switching Waveforms

Figure 4. Read Cycle No. 1: Address Transition Controlled [13, 14]

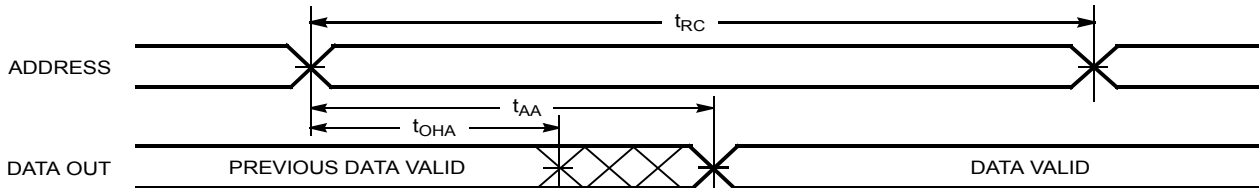
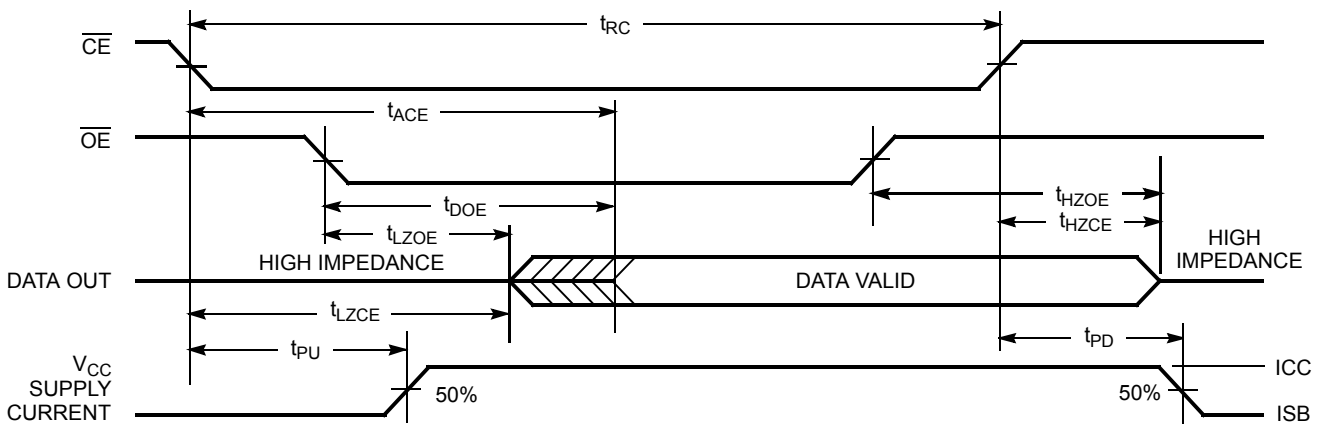


Figure 5. Read Cycle No. 2  $\overline{OE}$  Controlled [14, 15]



**Notes**

- 11. Tested initially and after any design or process changes that may affect these parameters.
- 12. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 50\ \mu\text{s}$  or stable at  $V_{CC(min)} \geq 50\ \mu\text{s}$ .
- 13. Device is continuously selected.  $OE, CE = V_{IL}$ .
- 14.  $WE$  is HIGH for read cycle.
- 15. Address valid prior to or coincident with  $\overline{CE}$  transition LOW.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 1:  $\overline{\text{CE}}$  Controlled [16, 17, 18]

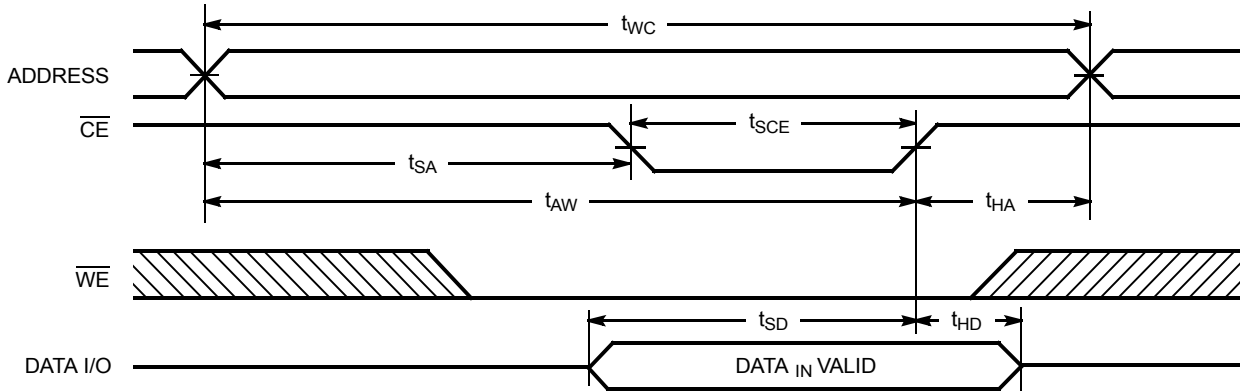
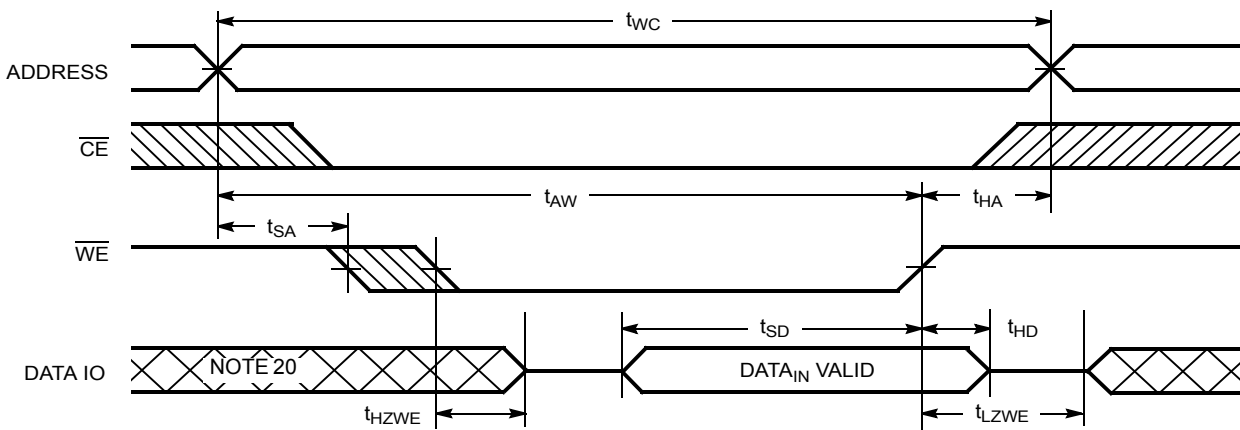


Figure 7. Write Cycle No. 3  $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW [18, 19]



Notes

- 16. The internal write time of the memory is defined by the overlap of  $\overline{\text{CE}}$  LOW and  $\overline{\text{WE}}$  LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 17. Data I/O is high impedance if  $\overline{\text{OE}} = V_{IH}$ .
- 18. If  $\overline{\text{CE}}$  goes HIGH simultaneously with  $\overline{\text{WE}}$  HIGH, the output remains in a high-impedance state.
- 19. The minimum write cycle time for Write Cycle No. 3 ( $\overline{\text{WE}}$  controlled,  $\overline{\text{OE}}$  LOW) is the sum of  $t_{HZWE}$  and  $t_{SD}$ .
- 20. During this period the I/Os are in the output state and input signals should not be applied.



**Truth Table**

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby ( $I_{SB}$ )
L	H	L	Data out	Read	Active ( $I_{CC}$ )
L	L	X	Data in	Write	Active ( $I_{CC}$ )
L	H	H	High Z	Deselect, output disabled	Active ( $I_{CC}$ )

**Ordering Information**

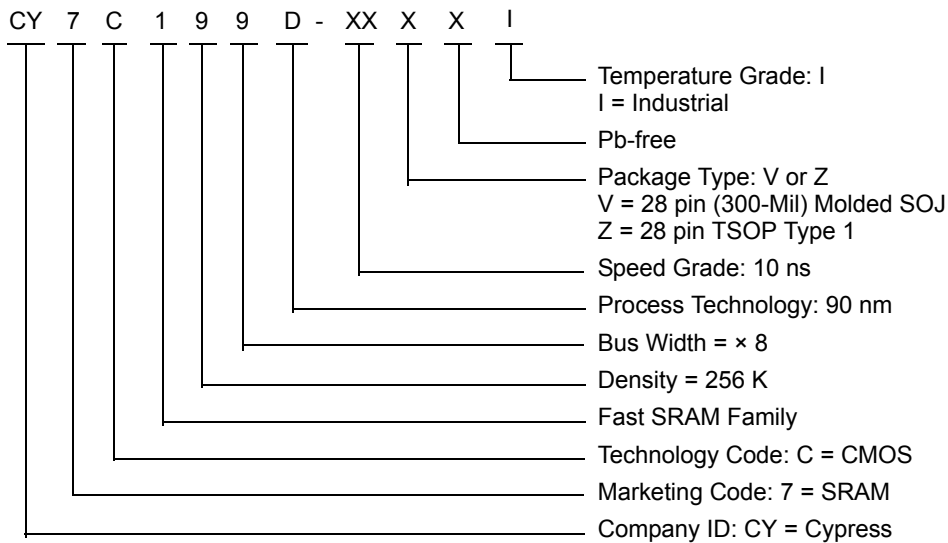
Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative.

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Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C199D-10VXI	51-85031	28-pin (300-Mil) Molded SOJ (Pb-free)	Industrial
	CY7C199D-10ZXI	51-85071	28-pin TSOP Type I (Pb-free)	

Please contact your local Cypress sales representative for availability of these parts.

**Ordering Code Definitions**

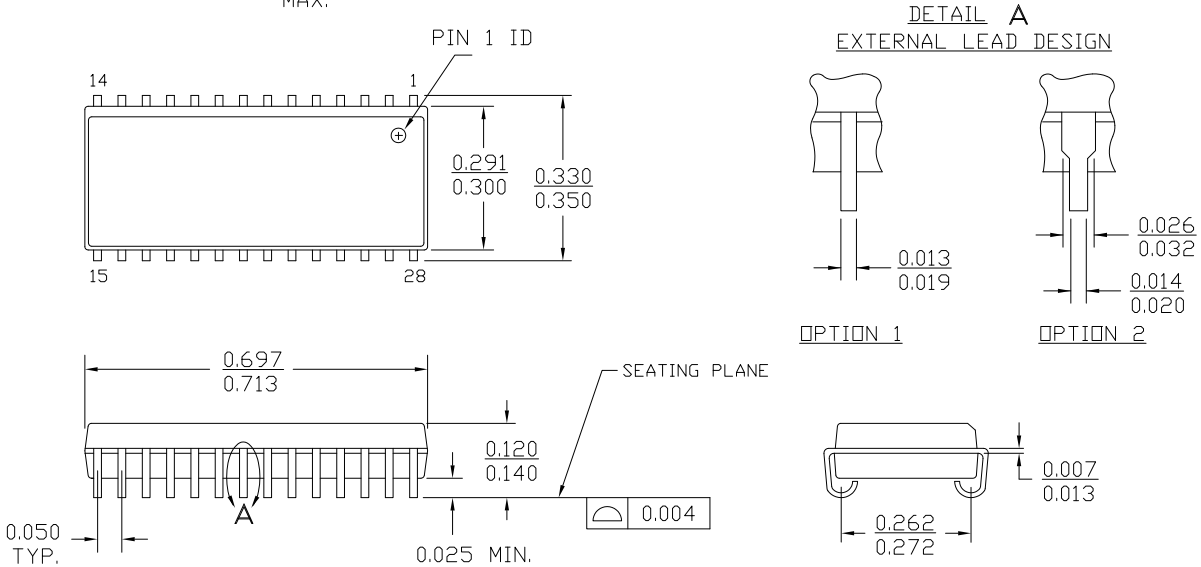


Package Diagrams

Figure 8. 28-pin SOJ 300-Mils V28.3 (Molded SOJ V21)

NOTE :

1. JEDEC STD REF M0088
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH  
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.006 in (0.152 mm) PER SIDE
3. DIMENSIONS IN INCHES MIN.  
MAX.

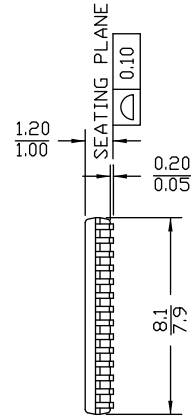
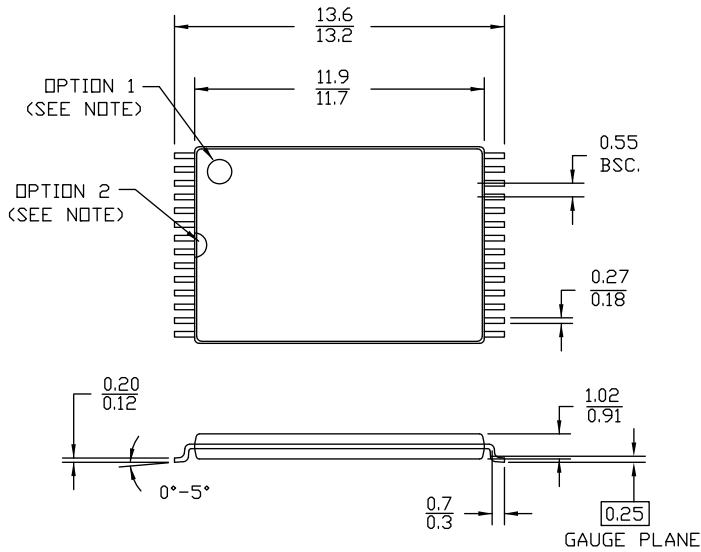


51-85031 \*D

Package Diagrams (continued)

Figure 9. 28-pin TSOP Type 1 (8 × 13.4 × 1.2 mm) Z28 (Standard)

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



DIMENSION IN MM  
MAX.  
MIN.

51-85071 \*1

## Acronyms

Acronym	Description
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SOJ	small outline J-lead
SRAM	static random access memory
TSOP	thin small outline package
TTL	transistor-transistor logic
$\overline{WE}$	write enable

## Document Conventions

### Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
μA	micro Amperes
μs	micro seconds
mA	milli Amperes
mm	milli meter
ns	nano seconds
pF	pico Farad
V	Volts
W	Watts

**Document History Page**

Document Title: CY7C199D, 256 K (32 K × 8) Static RAM Document Number: 38-05471				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	201560	SWI	See ECN	Advance Information datasheet for C9 IPP
*A	233728	RKF	See ECN	DC parameters modified as per EROS (Spec # 01-02165) Pb-free Offering in Ordering Information
*B	262950	RKF	See ECN	Removed 28-LCC Pinout and Package Diagrams Added Data Retention Characteristics table Added T <sub>power</sub> Spec in Switching Characteristics table Shaded Ordering Information
*C	307594	RKF	See ECN	Reduced Speed bins to -10, -12 and -15 ns
*D	820660	VKN	See ECN	Converted from Preliminary to Final Removed 12 ns and 15 ns speed bin Removed Commercial Operating range Removed "L" part Removed 28-pin PDIP and 28-pin SOIC package Changed Overshoot spec from V <sub>CC</sub> +2V to V <sub>CC</sub> +1V in footnote #2 Changed I <sub>CC</sub> spec from 60 mA to 80 mA for 100 MHz speed bin Added I <sub>CC</sub> specs for 83 MHz, 66 MHz and 40 MHz speed bins Updated Thermal Resistance table Updated Ordering Information Table
*E	2745093	VKN	See ECN	Included 28-Pin SOIC package Changed V <sub>IH</sub> level from 2.0V to 2.2V For Industrial grade, changed t <sub>SD</sub> from 5 ns to 6 ns, and t <sub>HZWE</sub> from 6 ns to 5 ns Included Automotive-E information
*F	2897087	AJU	03/22/10	Removed obsolete parts from ordering information table Updated package diagrams
*G	3023234	RAME	09/06/2010	Added Auto-E SOIC package related info Changed TDOE spec from 10 ns to 11 ns in CY7C199D-25. Added <a href="#">Ordering Code Definitions</a> . Added <a href="#">Acronyms</a> and <a href="#">Document Conventions</a> .
*H	3130763	PRAS	01/07/11	Dislodged Automotive information to a new datasheet (001-65530)
*I	3271782	PRAS	06/02/2011	Updated <a href="#">Functional Description</a> (Removed "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines."). Updated <a href="#">Package Diagrams</a> . Updated in new template.

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<a href="#">Lighting &amp; Power Control</a>	<a href="http://cypress.com/go/powerpsoc">cypress.com/go/powerpsoc</a> <a href="http://cypress.com/go/plc">cypress.com/go/plc</a>
<a href="#">Memory</a>	<a href="http://cypress.com/go/memory">cypress.com/go/memory</a>
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<a href="#">PSoC</a>	<a href="http://cypress.com/go/psoc">cypress.com/go/psoc</a>
<a href="#">Touch Sensing</a>	<a href="http://cypress.com/go/touch">cypress.com/go/touch</a>
<a href="#">USB Controllers</a>	<a href="http://cypress.com/go/USB">cypress.com/go/USB</a>
<a href="#">Wireless/RF</a>	<a href="http://cypress.com/go/wireless">cypress.com/go/wireless</a>

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