

# MediaClock™ Mini Disc Clock Generator

## Features

- Integrated phase-locked loop (PLL)
- Low jitter, high accuracy outputs
- 3.3V operation
- 8-pin SOIC package

## Benefits

- High performance PLL tailored for mini disc applications.
- Meets critical timing requirements in complex system designs.
- Enables application compatibility.
- Industry standard package saves on board space.

Part Number	Outputs	Input Frequency Range	Output Frequencies
CY24115-1	1	1 MHz–30 MHz	45.1584 MHz and 90.3168 MHz (selectable)
CY24115-2	1	1 MHz–30 MHz	90.3168 MHz and 180.6336 MHz (selectable)

## Logic Block Diagram

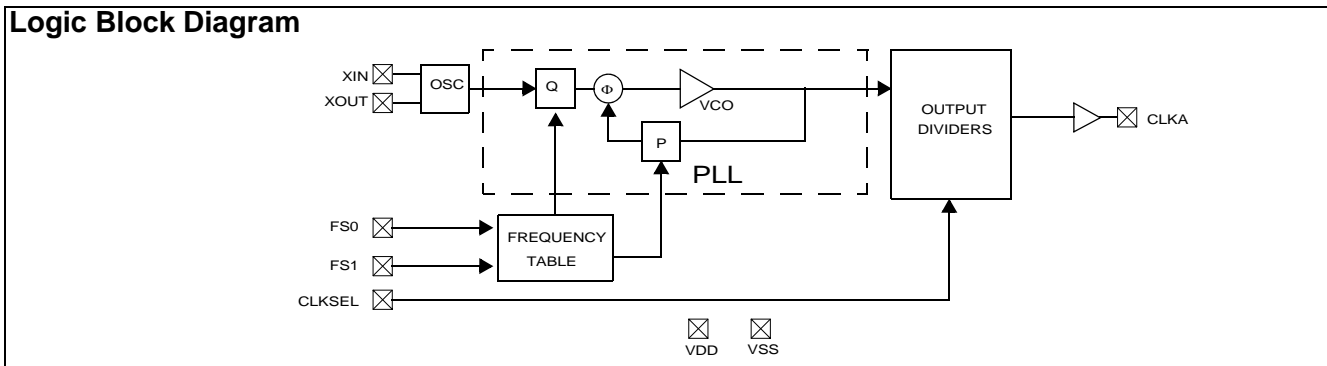


Table 1. CLKSEL Function CY24115-1

CLKSEL	CLKA	Unit	PPM Error
0	45.1584	MHz	0
1	90.3168	MHz	0

Table 2. CLKSEL Function, CY24115-2

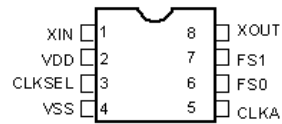
CLKSEL	CLKA	Unit	PPM Error
0	90.3168	MHz	0
1	180.6336	MHz	0

Table 3. Input Frequency Function, CY24115-1 and CY24115-2

FS1	FS0	Xtal Input	Unit
0	0	2.8224	MHz
0	1	5.6448	MHz
1	0	11.2896	MHz
1	1	22.5792	MHz

## Pin Configurations

**Figure 1. CY24115 8-Pin SOIC**



**Table 4. Pin Summary**

Pin Name	Pin Number	Pin Description
X <sub>IN</sub>	1	Reference input (crystal or external input)
V <sub>DD</sub>	2	3.3V voltage supply
CLKSEL	3	CLKA select line For 24115-1, see <a href="#">Table 1</a> on page 1 for output values For 24115-2, see <a href="#">Table 2</a> on page 1 for output values
V <sub>SS</sub>	4	Ground
CLKA	5	24115-1: 45.1584 MHz and 90.3168 MHz (frequency selectable). See <a href="#">Table 1</a> on page 1. 24115-2: 90.3168 MHz and 180.6336 MHz (frequency selectable). See <a href="#">Table 2</a> on page 1.
FS0	6	Input frequency FS0. See <a href="#">Table 3</a> on page 1.
FS1	7	Input frequency FS1. See <a href="#">Table 3</a> on page 1.
X <sub>OUT</sub> <sup>[1]</sup>	8	Reference output

**Note**

1. Float X<sub>OUT</sub> if X<sub>IN</sub> is externally driven.

**Absolute Maximum Conditions**

Parameter	Description	Min	Max	Unit
V <sub>DD</sub>	Supply Voltage	-0.5	7.0	V
T <sub>S</sub>	Storage Temperature <sup>[2]</sup>	-65	125	°C
T <sub>J</sub>	Junction Temperature		125	°C
	Digital Inputs	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Digital Outputs Referred to V <sub>DD</sub>	V <sub>SS</sub> - 0.3	V <sub>DD</sub> + 0.3	V
	Electrostatic Discharge	2		kV

**Recommended Operating Conditions**

Parameter	Description	Min	Typ	Max	Unit
V <sub>DD</sub>	Operating Voltage	3.14	3.3	3.47	V
T <sub>A</sub>	Ambient Temperature	0		70	°C
C <sub>LOAD</sub>	Max. Load Capacitance			15	pF
f <sub>REF</sub>	Reference Frequency	2.8224		22.5792	MHz
t <sub>1</sub>	Driven Reference Edge Rate	0.8			V/ns
DC <sub>IN</sub>	Driven Reference Duty Cycle	40		60	%
C <sub>IN</sub>	X <sub>IN</sub> , X <sub>OUT</sub> capacitance		12		pF
t <sub>PU</sub>	Power up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.05		500	ms

**DC Electrical Characteristics**

Parameter	Name	Description	Min	Typ	Max	Unit
I <sub>OH</sub>	Output High Current	V <sub>OH</sub> = V <sub>DD</sub> - 0.5, V <sub>DD</sub> = 3.3V (source)	12	24		mA
I <sub>OL</sub>	Output Low Current	V <sub>OL</sub> = 0.5, V <sub>DD</sub> = 3.3V (sink)	12	24		mA
C <sub>IN</sub>	Input Capacitance	CLKSEL, FS0, FS1, excludes XIN, XOUT			7	pF
V <sub>IL</sub>	Input Low Voltage				30	% of V <sub>DD</sub>
V <sub>IH</sub>	Input High Voltage		70			% of V <sub>DD</sub>
I <sub>Iz</sub>	Input Leakage Current			5		μA
I <sub>DD</sub>	Supply Current	Sum of core and output current			35	mA

**AC Electrical Characteristics (V<sub>DD</sub> = 3.3V)**

Parameter <sup>[3]</sup>	Name	Description	Min	Typ	Max	Unit
DC	Output Duty Cycle	Duty cycle is defined in <a href="#">Figure 3</a> , 50% of V <sub>DD</sub>	45	50	55	%
t <sub>3</sub>	Rising Edge Slew Rate	Output clock rise time, 20%–80% of V <sub>DD</sub>	0.8	1.4		V/ns
t <sub>4</sub>	Falling Edge Slew Rate	Output clock fall time, 80%–20% of V <sub>DD</sub>	0.8	1.4		V/ns
t <sub>9</sub>	Clock Jitter	Peak to peak period jitter			350	ps
t <sub>10</sub>	PLL Lock Time				3	ms

**Notes**

2. Rated for 10 years.
3. Not 100% tested.

Figure 2. Test Circuit

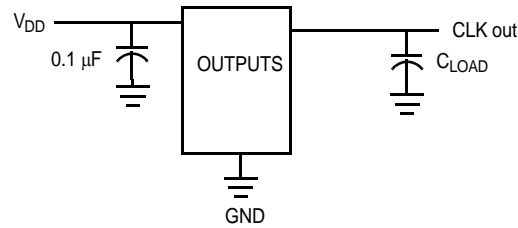


Figure 3. Duty Cycle Definition;  $DC = t2/t1$

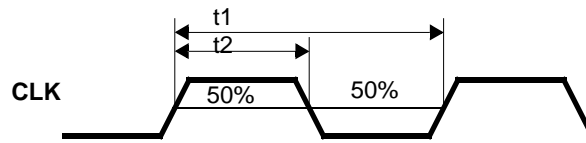
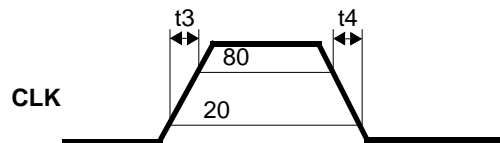


Figure 4. Rise and Fall Time Definitions



### Ordering Information

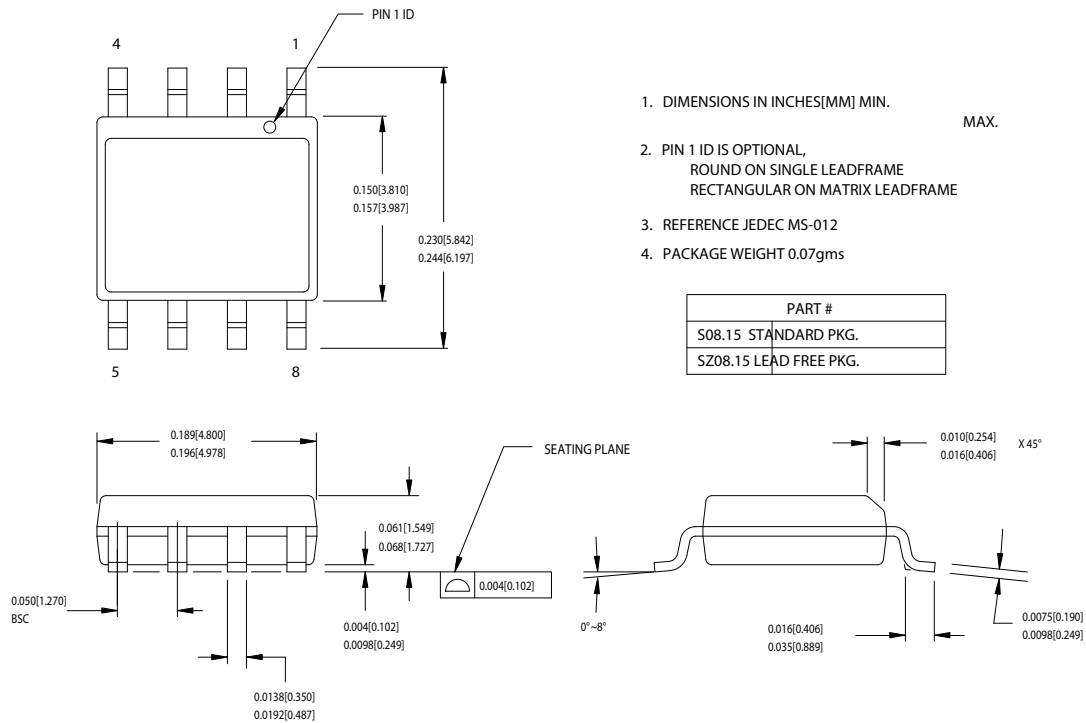
Ordering Code	Package Type	Operating Range	Operating Voltage
CY24115SC-1 <sup>[4]</sup>	8-pin SOIC	Commercial	3.3V
CY24115SC-1T <sup>[4]</sup>	8-pin SOIC - Tape and Reel	Commercial	3.3V
CY24115SC-2 <sup>[4]</sup>	8-pin SOIC	Commercial	3.3V
CY24115SC-2T <sup>[4]</sup>	8-pin SOIC - Tape and Reel	Commercial	3.3V
<b>Pb-Free</b>			
CY24115SXC-1 <sup>[4]</sup>	8-pin SOIC	Commercial	3.3V
CY24115SXC-1T <sup>[4]</sup>	8-pin SOIC - Tape and Reel	Commercial	3.3V
CY24115SXC-2 <sup>[4]</sup>	8-pin SOIC	Commercial	3.3V
CY24115SXC-2T <sup>[4]</sup>	8-pin SOIC - Tape and Reel	Commercial	3.3V
CY24115KSXC-2	8-pin SOIC	Commercial	3.3V
CY24115KSXC-2T	8-pin SOIC - Tape and Reel	Commercial	3.3V

**Note**

4. Not recommended for new designs.

Package Drawing and Dimensions

Figure 5. 8-Lead (150-Mil) SOIC S8



51-85066-°C

## Document History Page

Document Title: CY24115 MediaClock™ Mini Disc Clock Generator Document Number: 38-07275				
Revision	ECN No.	Orig. of Change	Submission Date	Description of Change
**	110767	CKN	02/06/02	New Data Sheet
*A	113515	CKN	04/30/02	Changed from Preliminary to Final P. 2 in Electrical Characteristics table added (source) to row 1 and (sink) to row 2
*B	121884	RBI	12/14/02	Power up requirements added to Operating Conditions Information
*C	252154	RGL	08/26/04	Added Lead Devices
*D	2441946	AESA	05/15/08	Updated template. Added Note "Not recommended for new designs." Added part number CY24115KSXC-2, and CY24115KSXC-2T in ordering information table.

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USB	<a href="http://psoc.cypress.com/usb">psoc.cypress.com/usb</a>

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