

Features

- Very high speed: 45 ns
 - Industrial: -40 °C to +85 °C
 - Automotive-E: -40 °C to +125 °C
- Wide voltage range: 4.5 V–5.5 V
- Ultra low standby power
 - Typical standby current: 2 μA
 - Maximum standby current: 8 μA (Industrial)
- Ultra low active power
 - Typical active current: 1.8 mA at f = 1 MHz
- Ultra low standby power
- Easy memory expansion with \overline{CE}_1 , CE_2 and \overline{OE} features
- Automatic power down when deselected
- CMOS for optimum speed and power
- Available in Pb-free 44-pin TSOP II and 48-ball VFBGA package

Functional Description

The CY62157E is a high performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable

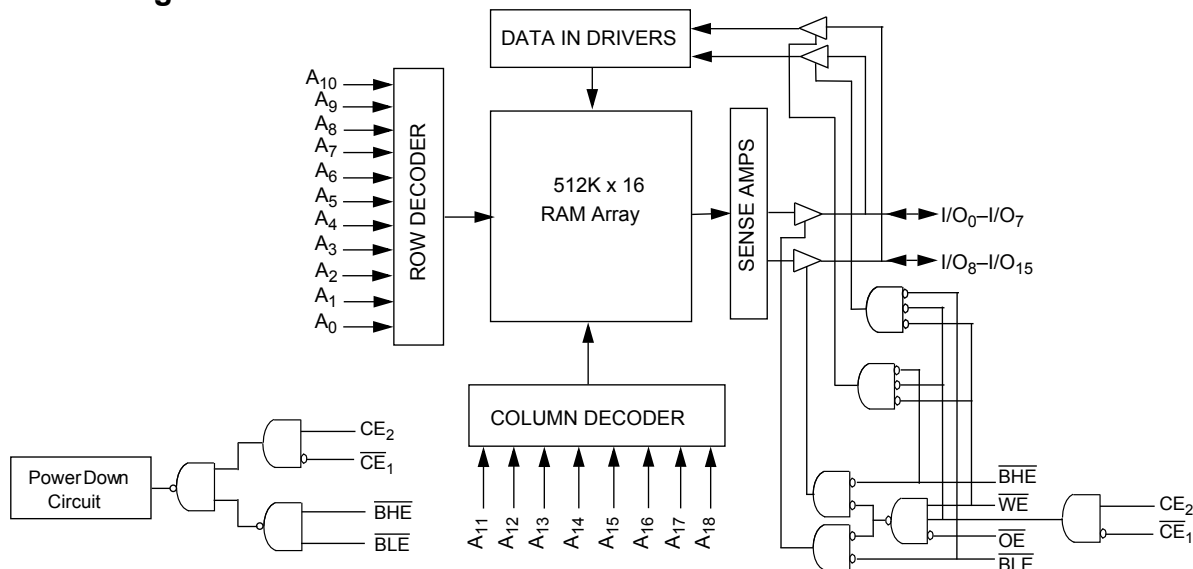
applications such as cellular telephones. The device also has an automatic power down feature that significantly reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected (\overline{CE}_1 HIGH or CE_2 LOW or both \overline{BHE} and \overline{BLE} are HIGH). The input or output pins (I/O_0 through I/O_{15}) are placed in a high impedance state when:

- Deselected (\overline{CE}_1 HIGH or CE_2 LOW)
- Outputs are disabled (\overline{OE} HIGH)
- Both Byte High Enable and Byte Low Enable are disabled (\overline{BHE} , \overline{BLE} HIGH)
- Write operation is active (\overline{CE}_1 LOW, CE_2 HIGH and \overline{WE} LOW)

To write to the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{18}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{18}).

To read from the device, take Chip Enable (\overline{CE}_1 LOW and CE_2 HIGH) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins appear on I/O_0 to I/O_7 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory appears on I/O_8 to I/O_{15} . See Truth Table on page 12 for a complete description of read and write modes.

Logic Block Diagram

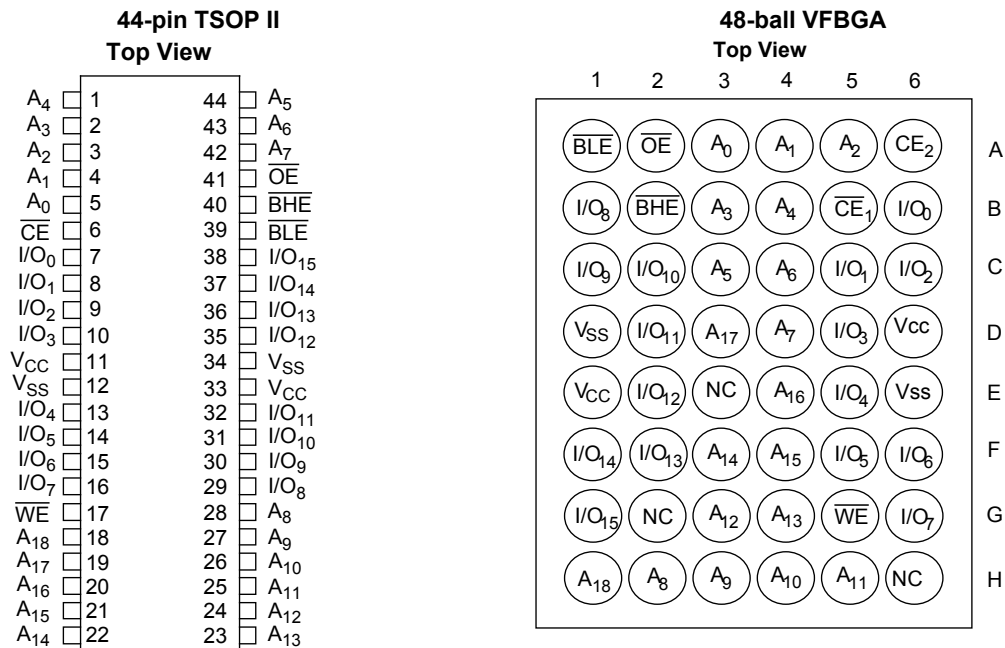


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Product Portfolio

| Product | Range | V _{CC} Range (V) | | | Speed (ns) | Power Dissipation | | | | | |
|------------|------------|---------------------------|--------------------|----------------------|------------|--------------------------------|-----|--------------------|-----|--------------------------------|-----|
| | | | | | | Operating I _{CC} (mA) | | | | Standby, I _{SB2} (μA) | |
| | | f = 1 MHz | | f = f _{max} | | | | | | | |
| | | Min | Typ ^[1] | Max | | Typ ^[1] | Max | Typ ^[1] | Max | Typ ^[1] | Max |
| CY62157ELL | Industrial | 4.5 | 5.0 | 5.5 | 45 | 1.8 | 3 | 18 | 25 | 2 | 8 |
| CY62157ELL | Automotive | 4.5 | 5.0 | 5.5 | 55 | 1.8 | 4 | 18 | 35 | 2 | 30 |

Pin Configuration ^[2, 3]

Notes

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
2. NC pins are not connected on the die.
3. The 44-pin TSOP II package has only one chip enable (\overline{CE}) pin.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage Temperature -65 °C to + 150 °C

Ambient Temperature with Power Applied -55 °C to + 125 °C

Supply Voltage to Ground Potential -0.5 V to 6.0 V

DC Voltage Applied to Outputs in High Z State^[4, 5] -0.5 V to 6.0 V

DC Input Voltage^[4, 5] -0.5 V to 6.0 V

Output Current into Outputs (LOW) 20 mA

Static Discharge Voltage (MIL-STD-883, Method 3015) > 2001 V

Latch up Current > 200 mA

Operating Range

| Device | Range | Ambient Temperature | V _{CC} ^[6] |
|------------|------------|---------------------|--------------------------------|
| CY62157ELL | Industrial | -40 °C to +85 °C | 4.5 V to 5.5 V |
| | Automotive | -40 °C to +125 °C | |

Electrical Characteristics

Over the Operating Range

| Parameter | Description | Test Conditions | 45 ns (Industrial) | | | 55 ns (Automotive) | | | Unit |
|---------------------------------|---|--|--------------------|--------------------|-----------------------|--------------------|--------------------|-----------------------|------|
| | | | Min | Typ ^[7] | Max | Min | Typ ^[7] | Max | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -1 mA | 2.4 | - | - | 2.4 | - | - | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 2.1 mA | - | - | 0.4 | - | - | 0.4 | V |
| V _{IH} | Input HIGH Voltage | V _{CC} = 4.5 V to 5.5 V | 2.2 | - | V _{CC} + 0.5 | 2.2 | - | V _{CC} + 0.5 | V |
| V _{IL} | Input LOW Voltage | V _{CC} = 4.5 V to 5.5 V | -0.5 | - | 0.8 | -0.5 | - | 0.8 | V |
| I _{IX} | Input Leakage Current | GND ≤ V _I ≤ V _{CC} | -1 | - | +1 | -4 | - | +4 | μA |
| I _{OZ} | Output Leakage Current | GND ≤ V _O ≤ V _{CC} , Output Disabled | -1 | - | +1 | -4 | - | +4 | μA |
| I _{CC} | V _{CC} Operating Supply Current | f = f _{max} = 1/t _{RC} | - | 18 | 25 | - | 18 | 35 | mA |
| | | f = 1 MHz | - | 1.8 | 3 | - | 1.8 | 4 | |
| I _{SB1} ^[8] | Automatic CE Power Down Current — CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2 V$ or $CE_2 \leq 0.2 V$ or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V, V _{IN} ≤ 0.2 V, f = f _{max} (Address and Data Only), f = 0 (OE and WE), V _{CC} = V _{CC(max)} | - | 2 | 8 | - | 2 | 30 | μA |
| I _{SB2} ^[8] | Automatic CE Power Down Current — CMOS Inputs | $\overline{CE}_1 \geq V_{CC} - 0.2 V$ or $CE_2 \leq 0.2 V$ or (BHE and BLE) ≥ V _{CC} - 0.2 V, V _{IN} ≥ V _{CC} - 0.2 V or V _{IN} ≤ 0.2 V, f = 0, V _{CC} = V _{CC(max)} | - | 2 | 8 | - | 2 | 30 | μA |

Notes

- V_{IL(min)} = -2.0 V for pulse durations less than 20 ns for I < 30 mA.
- V_{IH(max)} = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full device AC operation assumes a 100 μs ramp time from 0 to V_{CC(min)} and 200 μs wait time after V_{CC} stabilization.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.
- Chip enables (CE₁ and CE₂) and byte enables (BHE and BLE) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

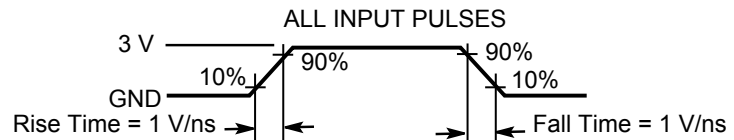
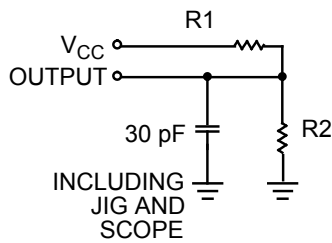
| Parameter ^[9] | Description | Test Conditions | Max | Unit |
|--------------------------|--------------------|---|-----|------|
| C _{IN} | Input Capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)} | 10 | pF |
| C _{OUT} | Output Capacitance | | 10 | pF |

Thermal Resistance

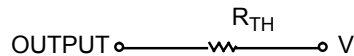
| Parameter ^[9] | Description | Test Conditions | 44-pin TSOP II | 48-ball VFBGA | Unit |
|--------------------------|--|--|----------------|---------------|------|
| Θ _{JA} | Thermal Resistance (Junction to Ambient) | Still Air, soldered on a 3 × 4.5 inch, two-layer printed circuit board | 77 | 72 | °C/W |
| Θ _{JC} | Thermal Resistance (Junction to Case) | | 13 | 8.86 | °C/W |

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



Equivalent to: THEVENIN EQUIVALENT



| Parameters | Values | Unit |
|-----------------|--------|------|
| R1 | 1800 | Ω |
| R2 | 990 | Ω |
| R _{TH} | 639 | Ω |
| V _{TH} | 1.77 | V |

Note

9. Tested initially and after any design or process changes that may affect these parameters.

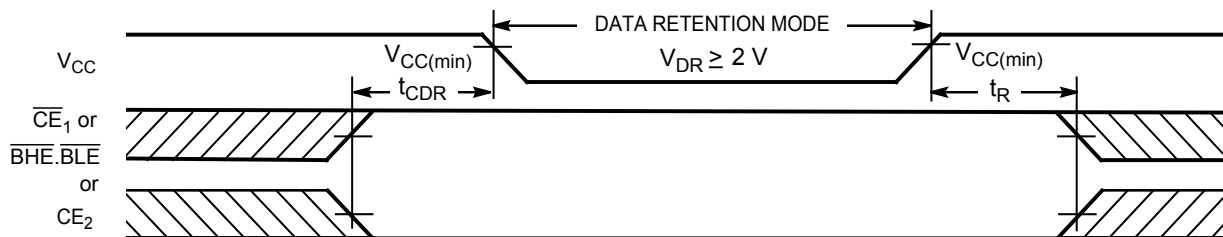
Data Retention Characteristics

Over the Operating Range

| Parameter | Description | Conditions | Min | Typ ^[10] | Max | Unit |
|----------------------------|--------------------------------------|--|------------|---------------------|-----|---------------|
| V_{DR} | V_{CC} for Data Retention | | 2 | – | – | V |
| I_{CCDR} ^[11] | Data Retention Current | $V_{CC} = 2\text{ V}$, $\overline{CE}_1 \geq V_{CC} - 0.2\text{ V}$ or $CE_2 \leq 0.2\text{ V}$ or $(\overline{BHE}$ and $\overline{BLE}) \geq V_{CC} - 0.2\text{ V}$, $V_{IN} \geq V_{CC} - 0.2\text{ V}$ or $V_{IN} \leq 0.2\text{ V}$ | Industrial | – | 8 | μA |
| | | | Automotive | – | – | 30 |
| t_{CDR} ^[12] | Chip Deselect to Data Retention Time | | 0 | – | – | ns |
| t_R ^[13] | Operation Recovery Time | | | | | |
| | | CY62157ELL-45 | 45 | – | – | ns |
| | | CY62157ELL-55 | 55 | – | – | |

Data Retention Waveform

Figure 2. Data Retention Waveform^[14]



Notes

- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, $T_A = 25\text{ }^\circ\text{C}$.
- Chip enables (\overline{CE}_1 and CE_2) and byte enables (\overline{BHE} and \overline{BLE}) need to be tied to CMOS levels to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
- Tested initially and after any design or process changes that may affect these parameters.
- Full device operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)}$ $\geq 100\text{ }\mu\text{s}$ or stable at $V_{CC(min)}$ $\geq 100\text{ }\mu\text{s}$.
- \overline{BHE} . \overline{BLE} is the AND of both \overline{BHE} and \overline{BLE} . Deselect the chip by either disabling chip enable signals or by disabling both \overline{BHE} and \overline{BLE} .

Switching Characteristics

Over the Operating Range

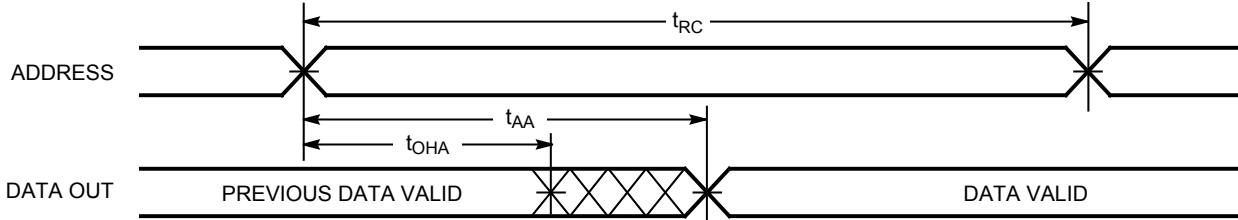
| Parameter ^[15, 16] | Description | 45 ns (Industrial) | | 55 ns (Automotive) | | Unit |
|-----------------------------------|---|--------------------|-----|--------------------|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t_{RC} | Read Cycle Time | 45 | – | 55 | – | ns |
| t_{AA} | Address to Data Valid | – | 45 | – | 55 | ns |
| t_{OHA} | Data Hold from Address Change | 10 | – | 10 | – | ns |
| t_{ACE} | \overline{CE}_1 LOW and CE_2 HIGH to Data Valid | – | 45 | – | 55 | ns |
| t_{DOE} | \overline{OE} LOW to Data Valid | – | 22 | – | 25 | ns |
| t_{LZOE} | \overline{OE} LOW to Low Z ^[17] | 5 | – | 5 | – | ns |
| t_{HZOE} | \overline{OE} HIGH to High Z ^[17, 18] | – | 18 | – | 20 | ns |
| t_{LZCE} | \overline{CE}_1 LOW and CE_2 HIGH to Low Z ^[17] | 10 | – | 10 | – | ns |
| t_{HZCE} | \overline{CE}_1 HIGH and CE_2 LOW to High Z ^[17, 18] | – | 18 | – | 20 | ns |
| t_{PU} | \overline{CE}_1 LOW and CE_2 HIGH to Power Up | 0 | – | 0 | – | ns |
| t_{PD} | \overline{CE}_1 HIGH and CE_2 LOW to Power Down | – | 45 | – | 55 | ns |
| t_{DBE} | $\overline{BLE}/\overline{BHE}$ LOW to Data Valid | – | 45 | – | 55 | ns |
| t_{LZBE} | $\overline{BLE}/\overline{BHE}$ LOW to Low Z ^[17] | 10 | – | 10 | – | ns |
| t_{HZBE} | $\overline{BLE}/\overline{BHE}$ HIGH to High Z ^[17, 18] | – | 18 | – | 20 | ns |
| Write Cycle^[19] | | | | | | |
| t_{WC} | Write Cycle Time | 45 | – | 55 | – | ns |
| t_{SCE} | \overline{CE}_1 LOW and CE_2 HIGH to Write End | 35 | – | 40 | – | ns |
| t_{AW} | Address Setup to Write End | 35 | – | 40 | – | ns |
| t_{HA} | Address Hold from Write End | 0 | – | 0 | – | ns |
| t_{SA} | Address Setup to Write Start | 0 | – | 0 | – | ns |
| t_{PWE} | \overline{WE} Pulse Width | 35 | – | 40 | – | ns |
| t_{BW} | $\overline{BLE}/\overline{BHE}$ LOW to Write End | 35 | – | 40 | – | ns |
| t_{SD} | Data Setup to Write End | 25 | – | 25 | – | ns |
| t_{HD} | Data Hold from Write End | 0 | – | 0 | – | ns |
| t_{HZWE} | \overline{WE} LOW to High Z ^[17, 18] | – | 18 | – | 20 | ns |
| t_{LZWE} | \overline{WE} HIGH to Low Z ^[17] | 10 | – | 10 | – | ns |

Notes

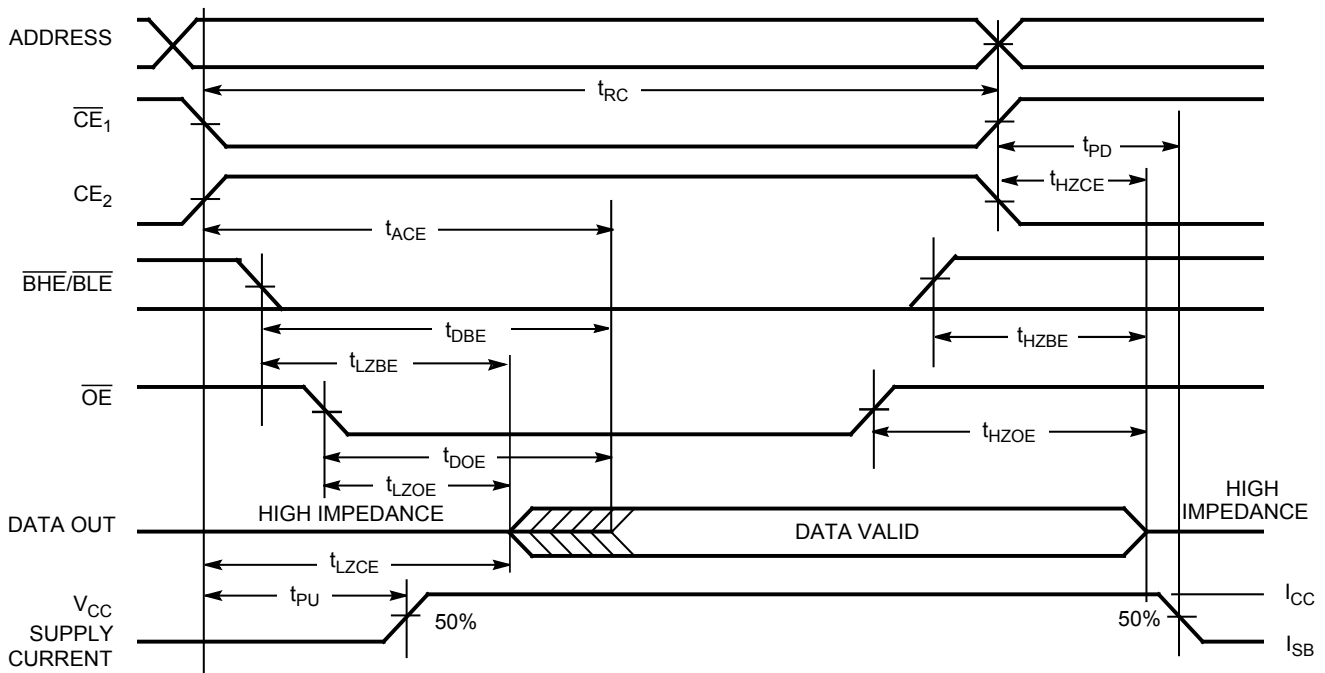
15. Test conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the *AC Test Loads and Waveforms* on page 5.
16. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See *application note AN13842* for further clarification.
17. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.
18. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.
19. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, BHE, BLE, or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Read Cycle No. 1 (Address Transition Controlled) [20, 21]



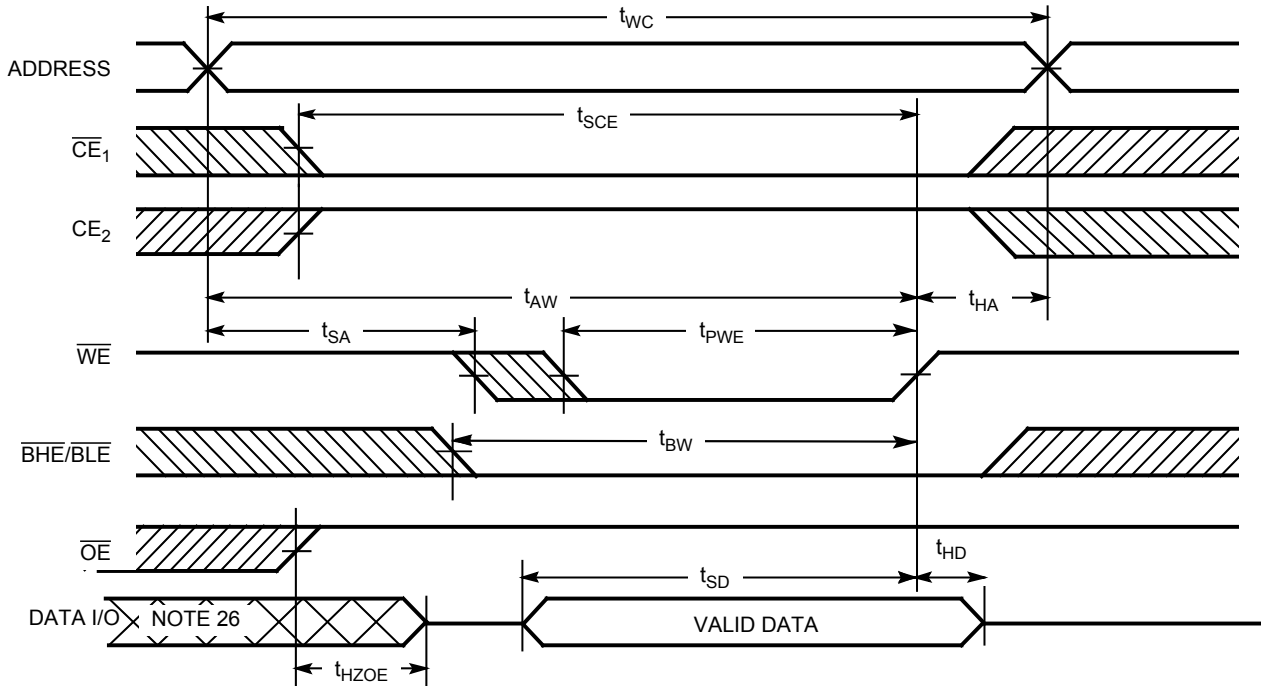
Read Cycle No. 2 (\overline{OE} Controlled) [21, 22]



Notes

- 20. The device is continuously selected. \overline{OE} , \overline{CE}_1 = V_{IL} , \overline{BHE} , \overline{BLE} or both = V_{IL} , and CE_2 = V_{IH} .
- 21. \overline{WE} is HIGH for read cycle.
- 22. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

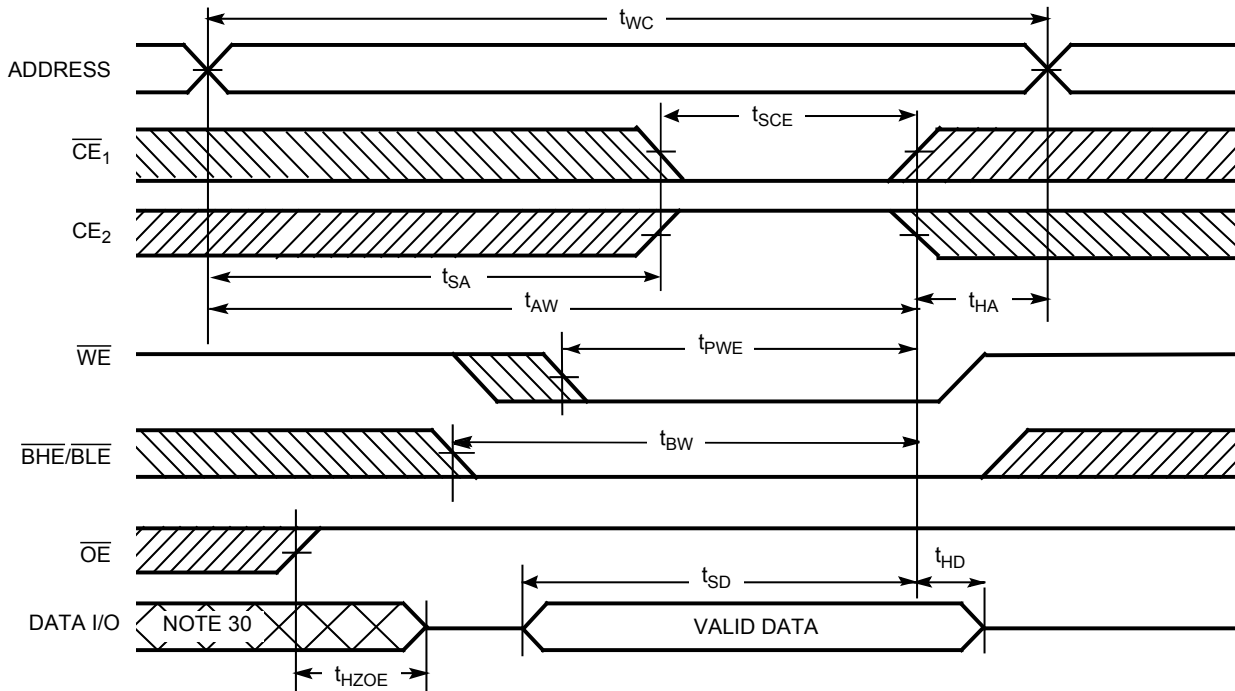
Switching Waveforms (continued)
Write Cycle No. 1 (\overline{WE} Controlled) [23, 24, 25]



Notes

- 23. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 24. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 25. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 26. During this period, the I/Os are in output state. Do not apply input signals.

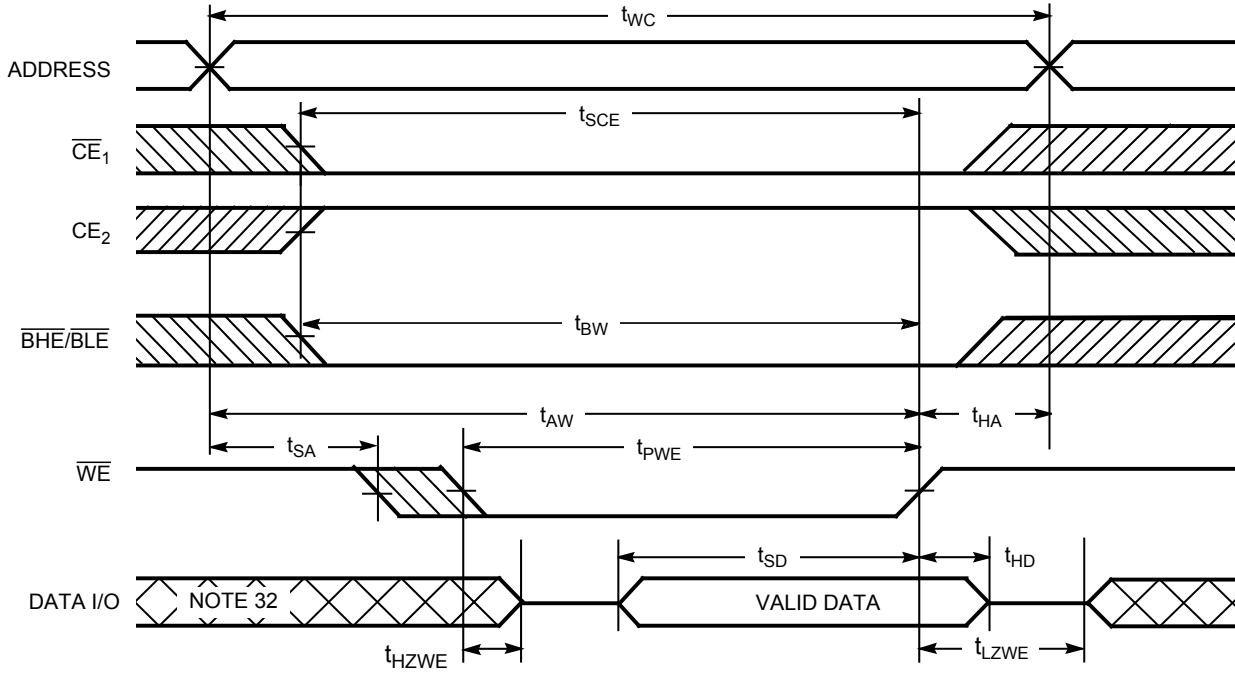
Switching Waveforms (continued)
Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled) [27, 28, 29]



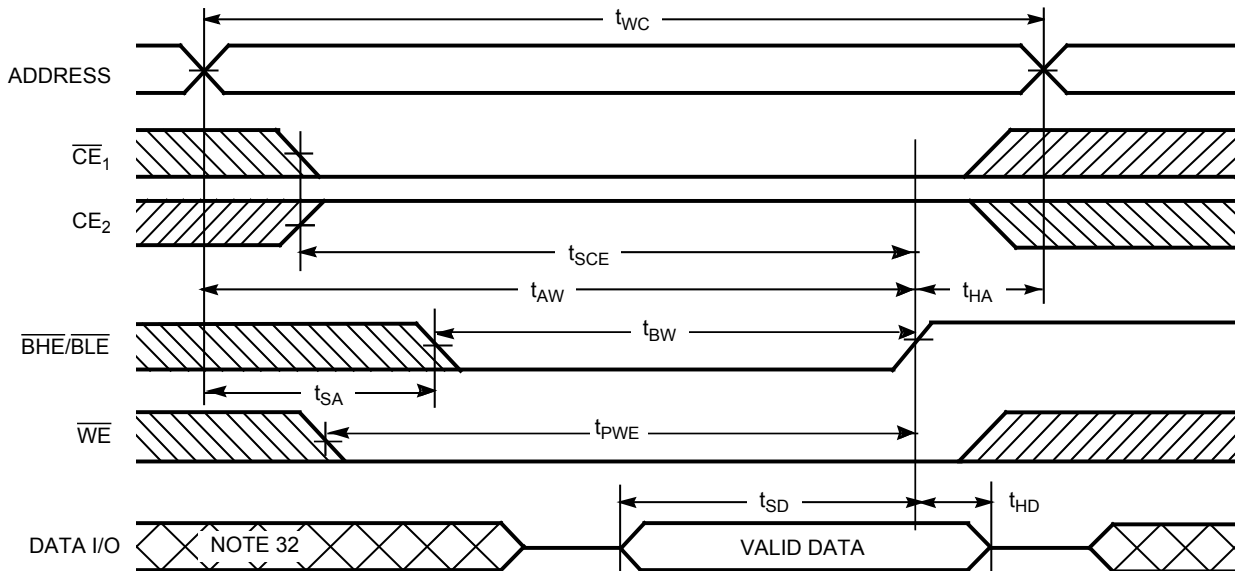
Notes

- 27. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} , or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing must be referenced to the edge of the signal that terminates the write.
- 28. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 29. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 30. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)
Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) [31]



Write Cycle No. 4 ($\overline{BHE}/\overline{BLE}$ Controlled, \overline{OE} LOW) [31]



Notes

- 31. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 32. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

| \overline{CE}_1 | CE_2 | \overline{WE} | \overline{OE} | \overline{BHE} | \overline{BLE} | Inputs/Outputs | Mode | Power |
|-------------------|-------------------|-----------------|-----------------|------------------|------------------|--|---------------------|----------------------|
| H | X ^[33] | X | X | X | X | High Z | Deselect/Power Down | Standby (I_{SB}) |
| X ^[33] | L | X | X | X | X | High Z | Deselect/Power Down | Standby (I_{SB}) |
| X ^[33] | X ^[33] | X | X | H | H | High Z | Deselect/Power Down | Standby (I_{SB}) |
| L | H | H | L | L | L | Data Out (I/O_0 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | H | L | Data Out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | L | L | H | High Z (I/O_0 – I/O_7); Data Out (I/O_8 – I/O_{15}) | Read | Active (I_{CC}) |
| L | H | H | H | L | H | High Z | Output Disabled | Active (I_{CC}) |
| L | H | H | H | H | L | High Z | Output Disabled | Active (I_{CC}) |
| L | H | H | H | L | L | High Z | Output Disabled | Active (I_{CC}) |
| L | H | L | X | L | L | Data In (I/O_0 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | H | L | Data In (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |
| L | H | L | X | L | H | High Z (I/O_0 – I/O_7); Data In (I/O_8 – I/O_{15}) | Write | Active (I_{CC}) |

Note

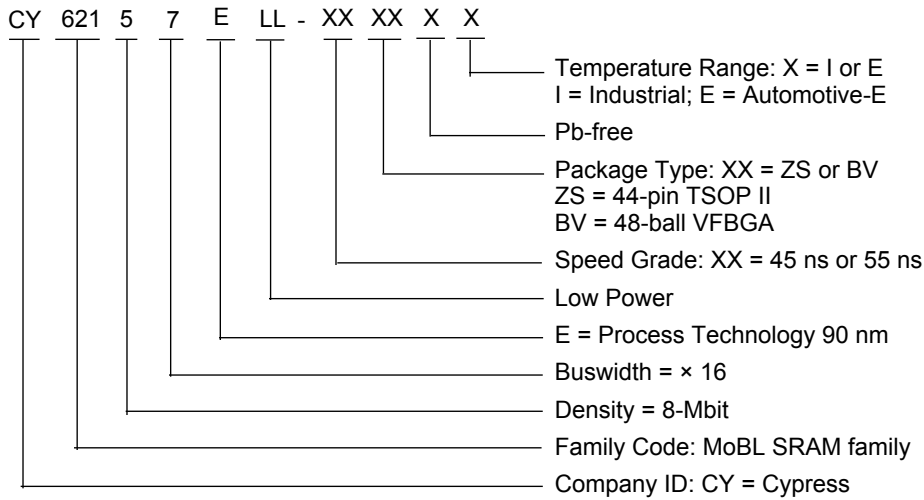
33. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

| Speed (ns) | Ordering Code | Package Diagram | Package Type | Operating Range |
|------------|-------------------|-----------------|---|-----------------|
| 45 | CY62157ELL-45ZSXI | 51-85087 | 44-pin Thin Small Outline Package Type II (Pb-free) | Industrial |
| 55 | CY62157ELL-55ZSXE | 51-85087 | 44-pin Thin Small Outline Package Type II (Pb-free) | Automotive |
| | CY62157ELL-55BVXE | 51-85150 | 48-ball Very Fine-Pitch Ball Grid Array (Pb-free) | |

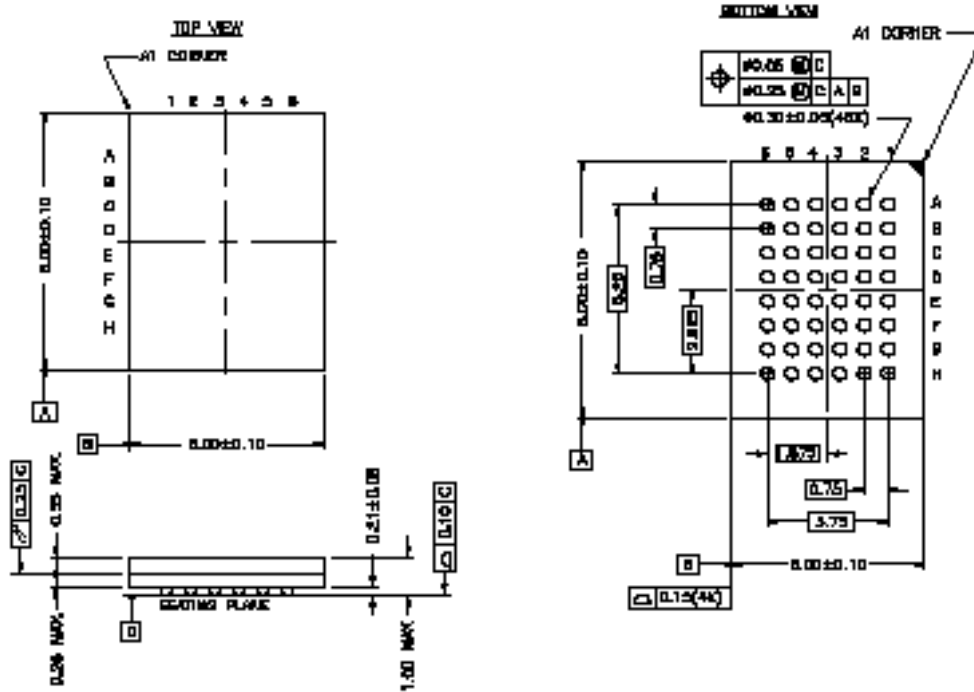
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

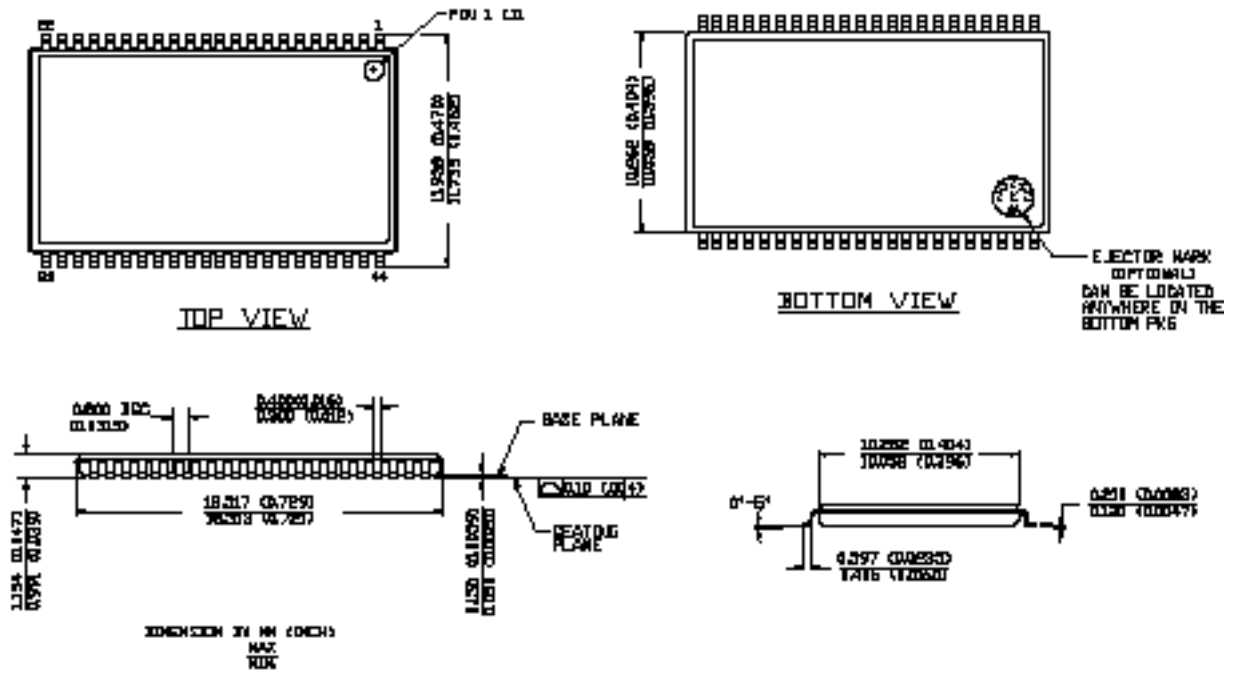
Figure 3. 48-ball VFBGA (6 × 8 × 1 mm) BV48/BZ48, 51-85150



51-85150 *F

Package Diagrams (continued)

Figure 4. 44-pin TSOP Z44-II, 51-85087



51-85087 *C

Acronyms

| Acronym | Description |
|-----------------|---|
| \overline{CE} | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| \overline{OE} | output enable |
| RAM | random access memory |
| SRAM | static random access memory |
| TTL | transistor-transistor logic |
| TSOP | thin small outline package |
| VFBGA | very fine-pitch ball grid array |
| \overline{WE} | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| °C | degree Celcius |
| MHz | Mega Hertz |
| μA | micro Amperes |
| μs | micro seconds |
| mA | milli Amperes |
| mm | milli meter |
| ns | nano seconds |
| Ω | ohms |
| % | percent |
| pF | pico Farad |
| V | Volts |
| W | Watts |

Document History Page

| Document Title: CY62157E MoBL [®] , 8-Mbit (512 K × 16) Static RAM Document Number: 38-05695 | | | | |
|--|---------|------------|-----------------|---|
| Rev. | ECN No. | Issue Date | Orig. of Change | Description of Change |
| ** | 291273 | See ECN | PCI | New data sheet |
| *A | 457689 | See ECN | NXR | Added Automotive Product Removed Industrial Product Removed 35 ns and 45 ns speed bins Removed "L" bin Updated AC Test Loads table Corrected t_R in Data Retention Characteristics from 100 μ s to t_{RC} ns Updated the Ordering Information and replaced the Package Name column with Package Diagram |
| *B | 467033 | See ECN | NXR | Added Industrial Product (Final Information) Removed 48 ball VFBGA package and its relevant information Changed the $I_{CC(typ)}$ value of Automotive from 2 mA to 1.8 mA for $f = 1$ MHz Changed the $I_{SB2(typ)}$ value of Automotive from 5 μ A to 1.8 μ A Modified footnote #4 to include current limit Updated the Ordering Information table |
| *C | 569114 | See ECN | VKN | Added 48 ball VFBGA package Updated Logic Block Diagram Added footnote #3 Updated the Ordering Information table |
| *D | 925501 | See ECN | VKN | Added footnote #9 related to I_{SB2} and I_{CCDR} Added footnote #14 related AC timing parameters |
| *E | 1045801 | See ECN | VKN | Converted Automotive specs from preliminary to final |
| *F | 2934396 | 06/03/10 | VKN | Added footnote #23 related to chip enable Updated package diagrams Updated template. |
| *G | 3110053 | 12/14/2010 | PRAS | Changed Table Footnotes to Footnotes. Added Ordering Code Definitions. |
| *H | 3269641 | 05/30/2011 | RAME | Removed the note "For best practice recommendations, please refer to the Cypress application note AN1064, SRAM System Guidelines." and its reference in Functional Description . Updated Electrical Characteristics . Updated Data Retention Characteristics . Added Acronyms and Units of Measure . Updated in new template. |

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