

16-Mbit (1 M × 16 / 2 M × 8) Static RAM

Features

- Configurable as 1 M × 16 or as 2 M × 8 SRAM
- Very high speed: 45 ns
- Wide voltage range: 4.5 V to 5.5 V
- Ultra low standby power
 - Typical standby current: 1.5 μA
 - Maximum standby current: 12 μA
- Ultra low active power
 - Typical active current: 2.2 mA at f = 1 MHz
- Easy memory expansion with \overline{CE}_1 , CE_2 , and \overline{OE} features
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Offered in 48-pin TSOP I package

Functional Description

The CY62167E is a high performance CMOS static RAM organized as 1 M words by 16-bits/2 M words by 8-bits. This device features advanced circuit design to provide an ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power down feature that

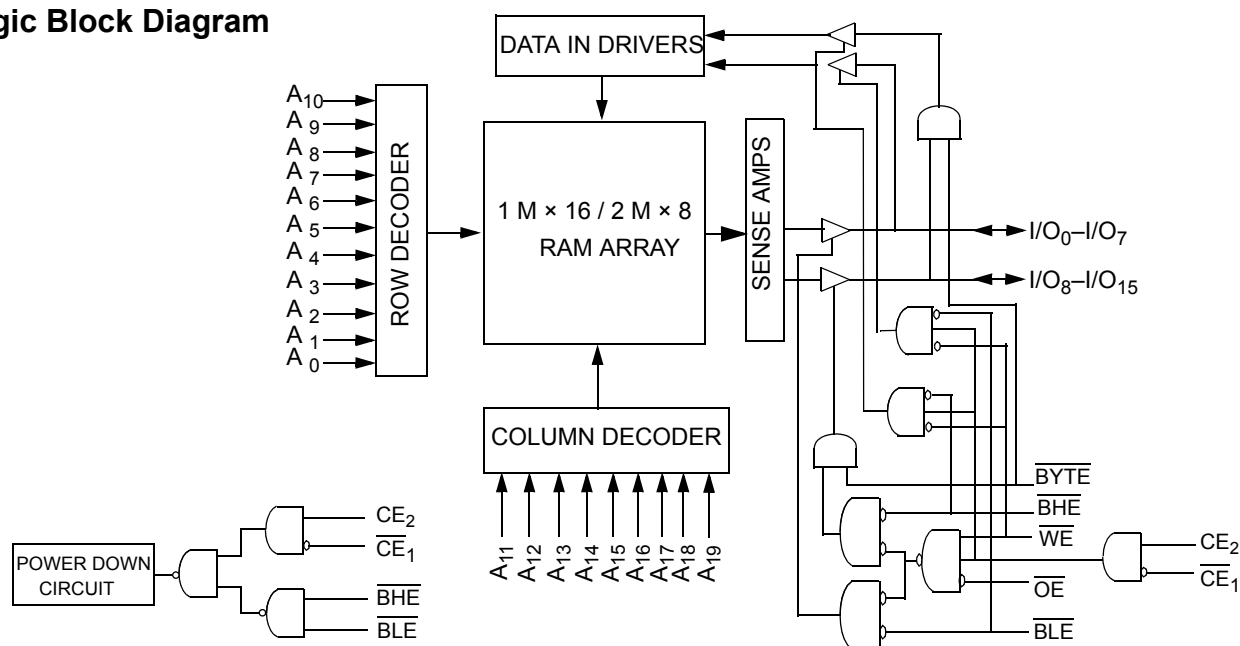
reduces power consumption when addresses are not toggling. Place the device into standby mode when deselected (CE_1 HIGH, or CE_2 LOW, or both BHE and BLE are HIGH). The input and output pins (I/O₀ through I/O₁₅) are placed in a high impedance state when:

- The device is deselected (\overline{CE}_1 HIGH or CE_2 LOW)
- Outputs are disabled (\overline{OE} HIGH)
- Both byte high enable and byte low enable are disabled (\overline{BHE} , BLE HIGH) or
- A write operation is in progress (\overline{CE}_1 LOW, CE_2 HIGH, and \overline{WE} LOW)

To write to the device, take chip enables (\overline{CE}_1 LOW and CE_2 HIGH) and write enable (\overline{WE}) input LOW. If byte low enable (BLE) is LOW, then data from I/O pins (I/O₀ through I/O₇), is written into the location specified on the address pins (A₀ through A₁₉). If byte high enable (BHE) is LOW, then data from the I/O pins (I/O₈ through I/O₁₅) is written into the location specified on the address pins (A₀ through A₁₉).

To read from the device, take chip enables (\overline{CE}_1 LOW and CE_2 HIGH) and output enable (\overline{OE}) LOW while forcing the write enable (\overline{WE}) HIGH. If byte low enable (BLE) is LOW, then data from the memory location specified by the address pins appears on I/O₀ to I/O₇. If byte high enable (\overline{BHE}) is LOW, then data from memory appears on I/O₈ to I/O₁₅. See Truth Table on page 12 for a complete description of read and write modes.

Logic Block Diagram

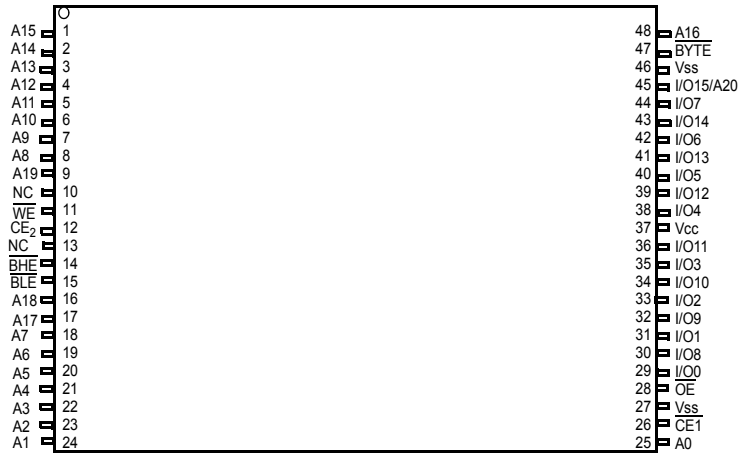


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Pin Configuration

48-pin TSOP I Top View [1, 2]



Product Portfolio

Product	V _{CC} Range (V)			Speed (ns)	Power Dissipation					
					Operating I _{CC} (mA)				Standby I _{SB2} (μA)	
	f = 1 MHz		f = f _{max}							
	Min	Typ ^[3]	Max		Typ ^[3]	Max	Typ ^[3]	Max	Typ ^[3]	Max
CY62167ELL	4.5	5.0	5.5	45	2.2	4.0	25	30	1.5	12

Notes

- NC pins are not connected on the die.
- The BYTE pin in the 48-pin TSOP I package must be tied to V_{CC} to use the device as a 1 M × 16 SRAM. The 48-TSOP I package can also be used as a 2 M × 8 SRAM by tying the BYTE signal to V_{SS}. In the 2 M × 8 configuration, pin 45 is A20, while BHE, BLE and I/O₈ to I/O₁₄ pins are not used.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC(typ)}, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential	-0.5 V to 6.0 V
DC voltage applied to outputs in high Z state ^[4, 5]	-0.5 V to 6.0 V

DC input voltage ^[4, 5]	-0.5 V to 6.0 V
Output current into outputs (LOW)	20 mA
Static discharge voltage	>2001 V (MIL-STD-883, method 3015)
Latch-up current	>200 mA

Operating Range

Device	Range	Ambient Temperature	V _{CC} ^[6]
CY62167ELL	Industrial	-40 °C to +85 °C	4.5 V to 5.5 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	45 ns			Unit
			Min	Typ ^[8]	Max	
V _{OH}	Output HIGH voltage	I _{OH} = -1.0 mA	2.4	-	-	V
V _{OL}	Output LOW voltage	I _{OL} = 2.1 mA	-	-	0.4	V
V _{IH}	Input HIGH voltage	V _{CC} = 4.5 V to 5.5 V	2.2	-	V _{CC} + 0.5 V	V
V _{IL}	Input LOW voltage	V _{CC} = 4.5 V to 5.5 V	-0.5	-	0.7 ^[7]	V
I _{IX}	Input leakage current	GND ≤ V _I ≤ V _{CC}	-1	-	+1	μA
I _{OZ}	Output leakage current	GND ≤ V _O ≤ V _{CC} , output disabled	-1	-	+1	μA
I _{CC}	V _{CC} operating supply current	f = f _{MAX} = 1/t _{RC}	-	25	30	mA
		f = 1 MHz	-	2.2	4.0	
I _{SB2} ^[9]	Automatic power down current—CMOS inputs	$\overline{CE}_1 \geq V_{CC} - 0.2 \text{ V}$ or $CE_2 \leq 0.2 \text{ V}$, or BHE and $BLE \geq V_{CC} - 0.2 \text{ V}$, $V_{IN} \geq V_{CC} - 0.2 \text{ V}$ or $V_{IN} \leq 0.2 \text{ V}$, $f = 0$, V _{CC} = V _{CC} (max)	-	1.5	12	μA

Notes

- V_{IL}(min) = -2.0 V for pulse durations less than 20 ns.
- V_{IH}(max) = V_{CC} + 0.75 V for pulse durations less than 20 ns.
- Full Device AC operation is based on a 100 μs ramp time from 0 to V_{CC}(min) and 200 μs wait time after V_{CC} stabilization.
- Under DC conditions the device meets a V_{IL} of 0.8 V. However, in dynamic conditions input LOW voltage applied to the device must not be higher than 0.7 V.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25 °C
- Chip enables (\overline{CE}_1 and CE₂), byte enables (BHE and BLE) and BYTE need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

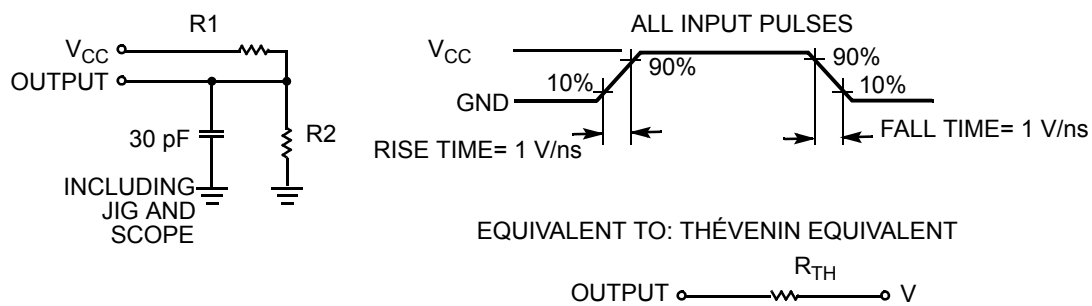
Parameter ^[10]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = V _{CC(typ)}	10	pF
C _{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter ^[10]	Description	Test Conditions	48-pin TSOP I	Unit
Θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	60	°C/W
Θ _{JC}	Thermal resistance (junction to case)		4.3	°C/W

AC Test Loads and Waveforms

Figure 1. AC Test Loads and Waveforms



Parameters	Values	Unit
R1	1800	Ω
R2	990	Ω
R _{TH}	639	Ω
V _{TH}	1.77	V

Note

¹⁰. Tested initially and after any design or process changes that may affect these parameters.

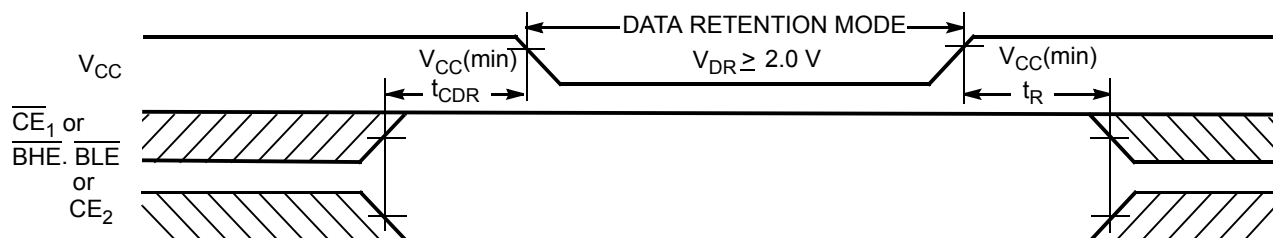
Data Retention Characteristics

Over the operating range

Parameter	Description	Conditions	Min	Typ ^[11]	Max	Unit
V _{DR}	V _{CC} for data retention	–	2.0	–	–	V
I _{CCDR} ^[12]	Data retention current	V _{CC} = V _{DR} , CE ₁ ≥ V _{CC} – 0.2 V or CE ₂ ≤ 0.2 V, or BHE and BLE ≥ V _{CC} – 0.2 V, V _{IN} ≥ V _{CC} – 0.2 V or V _{IN} ≤ 0.2 V	–	–	12	μA
t _{CDR} ^[13]	Chip deselect to data retention time	–	0	–	–	ns
t _R ^[14]	Operation recovery time	–	45	–	–	ns

Data Retention Waveform

Figure 2. Data Retention Waveform^[15]



Notes

11. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC}(typ), T_A = 25 °C.
12. Chip enables (CE₁ and CE₂), byte enables (BHE and BLE) and BYTE need to be tied to CMOS levels to meet the I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
13. Tested initially and after any design or process changes that may affect these parameters.
14. Full device operation requires linear V_{CC} ramp from V_{DR} to V_{CC}(min) ≥ 100 μs or stable at V_{CC}(min) ≥ 100 μs.
15. BHE, BLE is the AND of BHE and BLE. Deselect the chip by either disabling the chip enable signals or by disabling BHE and BLE.

Switching Characteristics

Over the Operating Range

Parameter ^[16, 17]	Description	45 ns		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	\overline{CE}_1 LOW and CE_2 HIGH to data valid	–	45	ns
t_{DOE}	\overline{OE} LOW to data valid	–	22	ns
t_{LZOE}	\overline{OE} LOW to low Z ^[18]	5	–	ns
t_{HZOE}	\overline{OE} HIGH to high Z ^[18, 19]	–	18	ns
t_{LZCE}	\overline{CE}_1 LOW and CE_2 HIGH to low Z ^[18]	10	–	ns
t_{HZCE}	\overline{CE}_1 HIGH and CE_2 LOW to high Z ^[18, 19]	–	18	ns
t_{PU}	\overline{CE}_1 LOW and CE_2 HIGH to power-up	0	–	ns
t_{PD}	\overline{CE}_1 HIGH and CE_2 LOW to power-down	–	45	ns
t_{DBE}	BLE/BHE LOW to data valid	–	45	ns
t_{LZBE}	$\overline{BLE}/\overline{BHE}$ LOW to low Z ^[18, 20]	5	–	ns
t_{HZBE}	$\overline{BLE}/\overline{BHE}$ HIGH to high Z ^[18, 19]	–	18	ns
Write Cycle^[21]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	\overline{CE}_1 LOW and CE_2 HIGH to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	\overline{WE} pulse width	35	–	ns
t_{BW}	$\overline{BLE}/\overline{BHE}$ LOW to write end	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	\overline{WE} LOW to high Z ^[18, 19]	–	18	ns
t_{LZWE}	\overline{WE} HIGH to low Z ^[18]	10	–	ns

Notes

16. Test conditions for all parameters other than tristate parameters assume signal transition time of 1 V/ns, timing reference levels of $V_{CC}(typ)/2$, input pulse levels of 0 to $V_{CC}(typ)$, and output loading of the specified I_{OL}/I_{OH} as shown in [Figure 1 on page 5](#).

17. AC timing parameters are subject to byte enable signals (BHE or BLE) not switching when chip is disabled. See [application note AN13842](#) for further clarification.

18. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZBE} is less than t_{LZBE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any device.

19. t_{HZOE} , t_{HZCE} , t_{HZBE} , and t_{HZWE} transitions are measured when the outputs enter a high impedance state.

20. If both byte enables are toggled together, this value is 10 ns.

21. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 3. Read Cycle No. 1 (Address Transition Controlled) [22, 23]

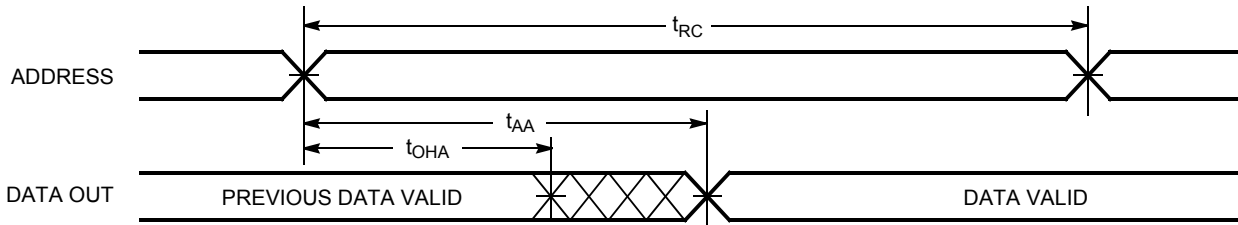
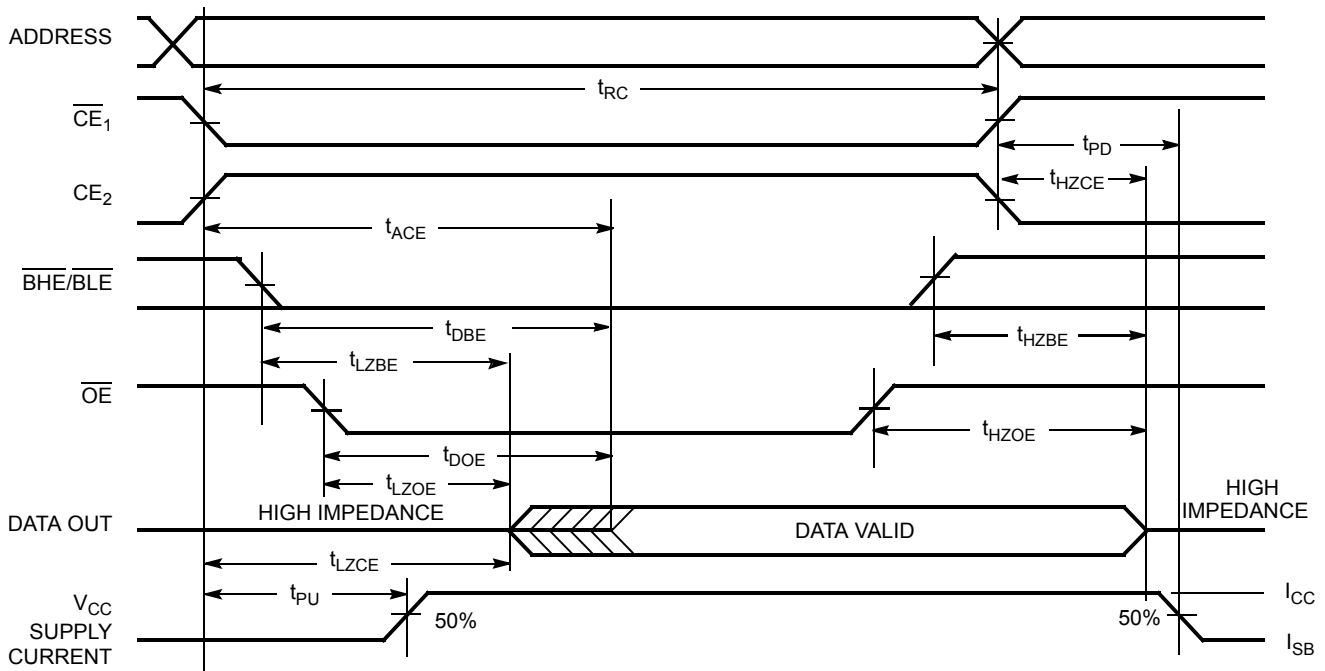


Figure 4. Read Cycle No. 2 (\overline{OE} Controlled) [23, 24]

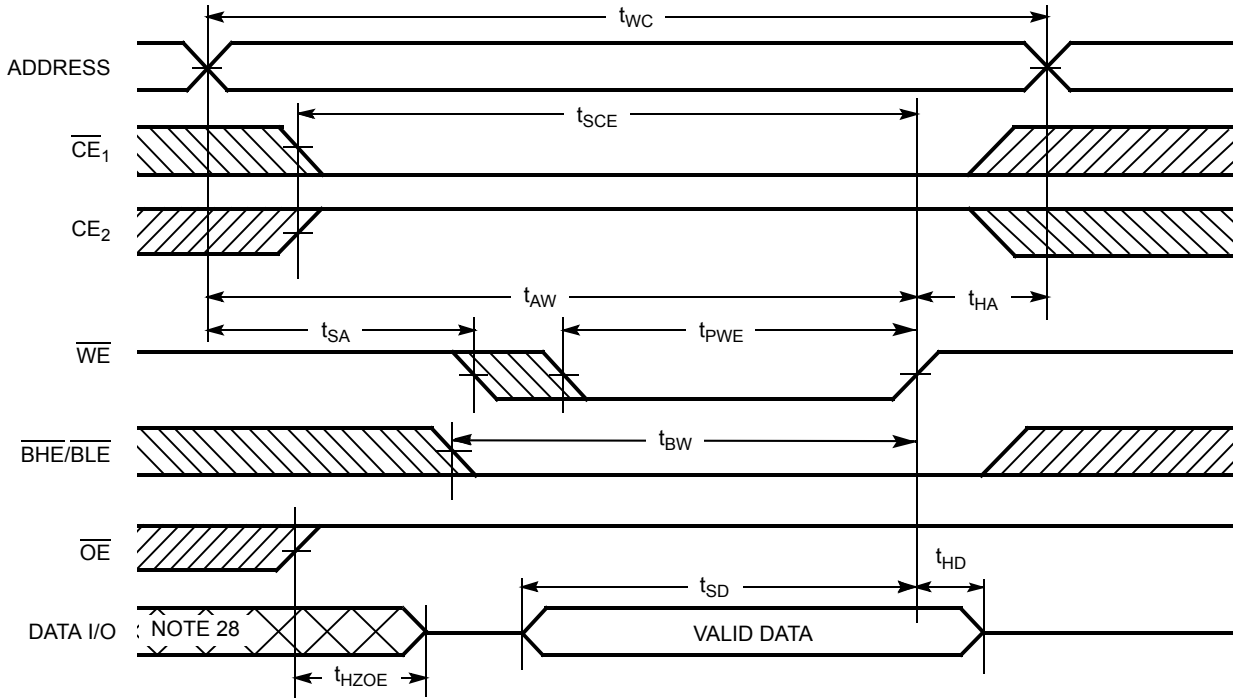


Notes

- 22. The device is continuously selected. \overline{OE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} , \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$.
- 23. \overline{WE} is HIGH for read cycle.
- 24. Address valid before or similar to \overline{CE}_1 , \overline{BHE} , \overline{BLE} transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 1 (\overline{WE} Controlled) [25, 26, 27]



Notes

- 25. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 26. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 27. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 28. During this period the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 (\overline{CE}_1 or CE_2 Controlled).^[29, 30, 31]

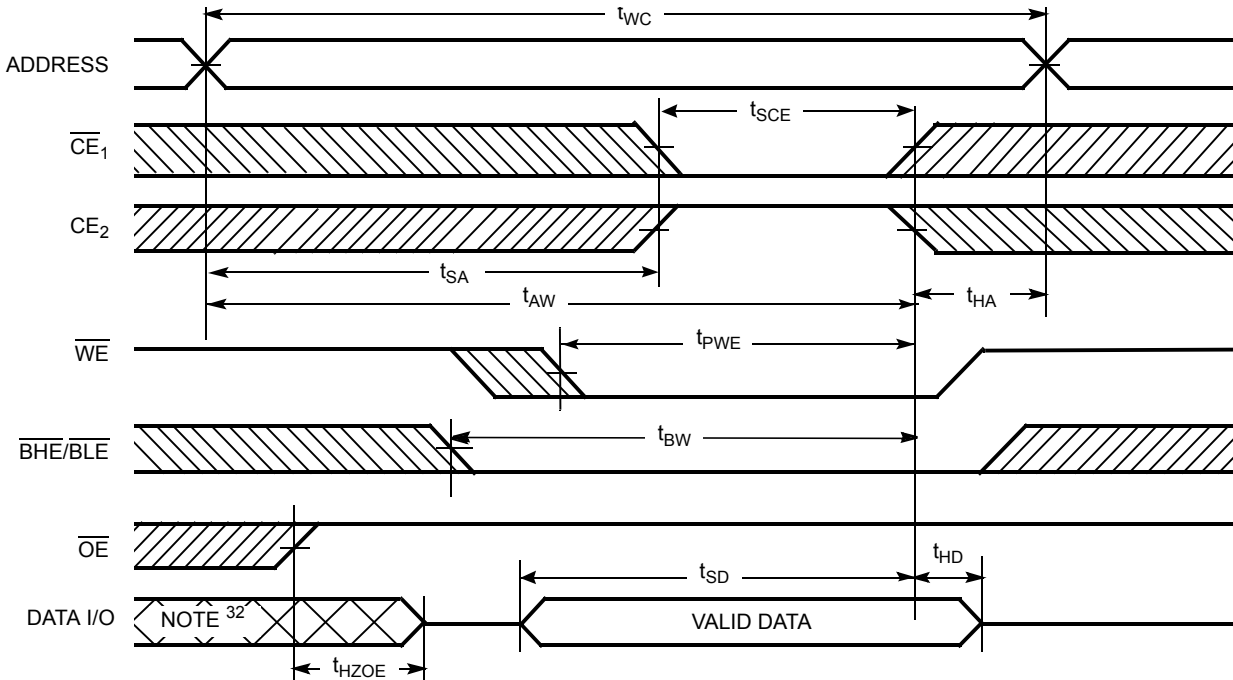
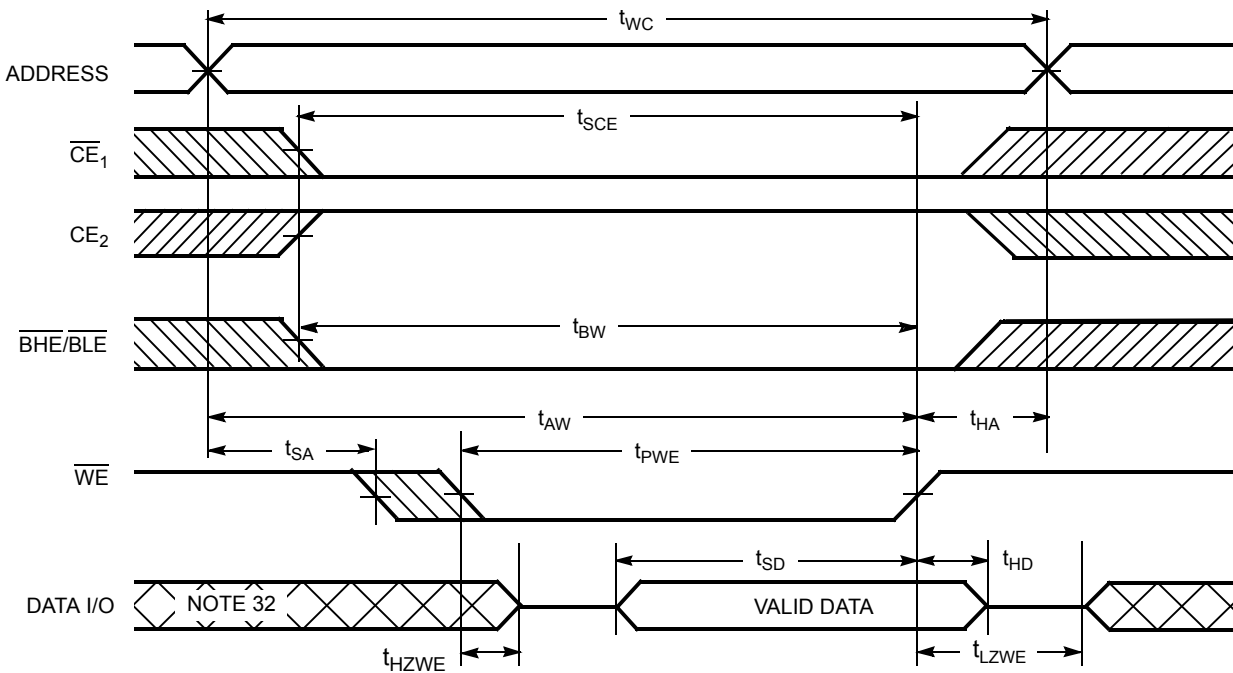


Figure 7. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)^[31]

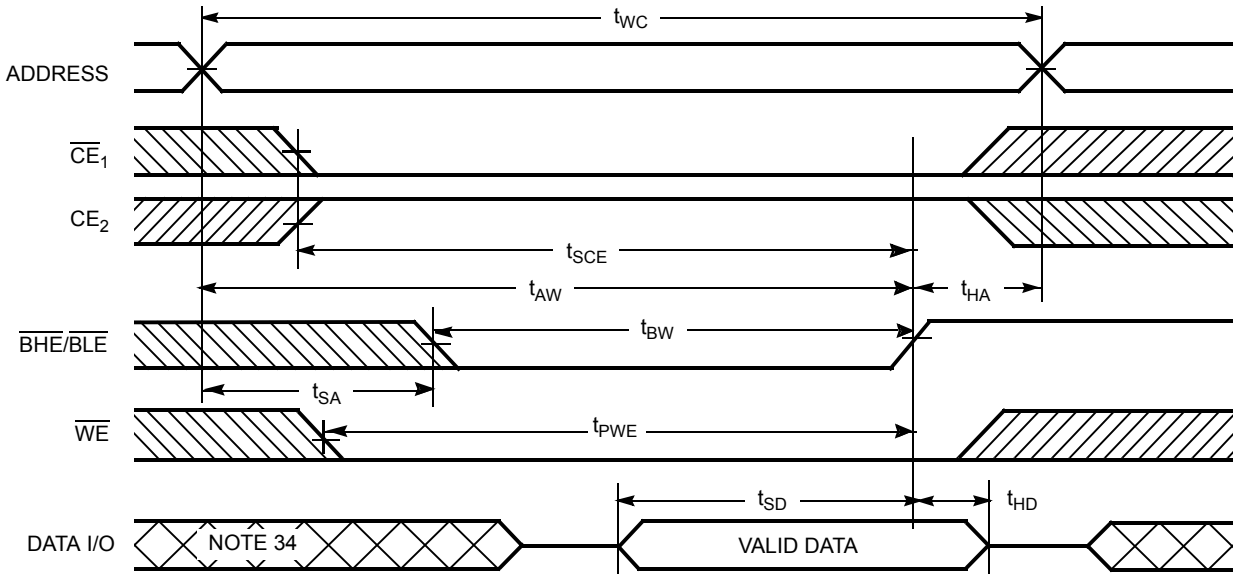


Notes

- 29. The internal write time of the memory is defined by the overlap of \overline{WE} , $\overline{CE}_1 = V_{IL}$, \overline{BHE} or \overline{BLE} or both = V_{IL} , and $CE_2 = V_{IH}$. All signals must be active to initiate a write and any of these signals can terminate a write by going inactive. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
- 30. Data I/O is high impedance if $\overline{OE} = V_{IH}$.
- 31. If \overline{CE}_1 goes HIGH and CE_2 goes LOW simultaneously with $\overline{WE} = V_{IH}$, the output remains in a high impedance state.
- 32. During this period the I/Os are in output state and input signals must not be applied.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 4 ($\overline{\text{BHE}}/\overline{\text{BLE}}$ controlled, $\overline{\text{OE}}$ LOW) [33]



Notes

- 33. If $\overline{\text{CE}}_1$ goes HIGH and CE_2 goes LOW simultaneously with $\overline{\text{WE}} = V_{IH}$, the output remains in a high impedance state.
- 34. During this period the I/Os are in output state and input signals must not be applied.

Truth Table

\overline{CE}_1	\overline{CE}_2	\overline{WE}	\overline{OE}	\overline{BHE}	\overline{BLE}	Inputs Outputs	Mode	Power
H	X ^[35]	X	X	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X ^[35]	L	X	X	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X ^[35]	X ^[35]	X	X	H	H	High Z	Deselect/power-down	Standby (I_{SB})
L	H	H	L	L	L	Data out (I/O_0 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	H	L	Data out (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	L	L	H	High Z (I/O_0 – I/O_7); Data out (I/O_8 – I/O_{15})	Read	Active (I_{CC})
L	H	H	H	L	H	High Z	Output disabled	Active (I_{CC})
L	H	H	H	H	L	High Z	Output disabled	Active (I_{CC})
L	H	H	H	L	L	High Z	Output disabled	Active (I_{CC})
L	H	L	X	L	L	Data in (I/O_0 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	H	L	Data in (I/O_0 – I/O_7); High Z (I/O_8 – I/O_{15})	Write	Active (I_{CC})
L	H	L	X	L	H	High Z (I/O_0 – I/O_7); Data in (I/O_8 – I/O_{15})	Write	Active (I_{CC})

Note

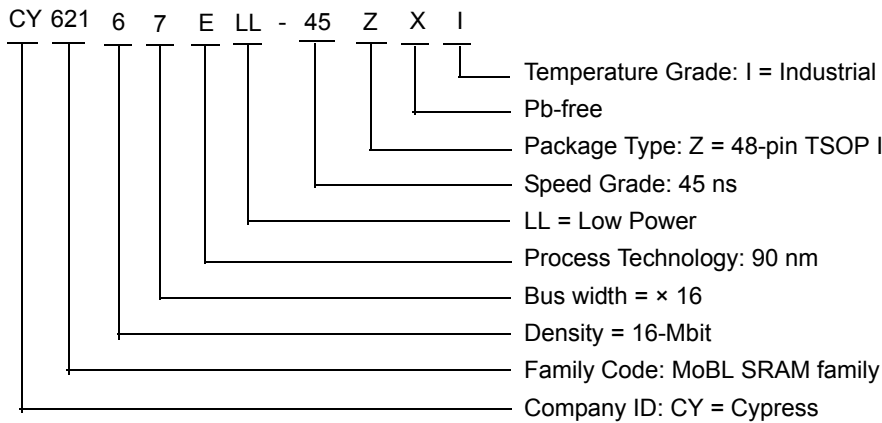
35. The 'X' (Do not care) state for the chip enables in the truth table refers to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

The below table lists the CY62167ELL key package features and ordering codes. The table contains only the parts that are currently available. If you do not see what you are looking for, contact your local sales representative. For more information, visit the Cypress website at www.cypress.com and refer to the product summary page at <http://www.cypress.com/products>.

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62167ELL-45ZXI	51-85183	48-pin TSOP I (Pb-free)	Industrial

Ordering Code Definitions

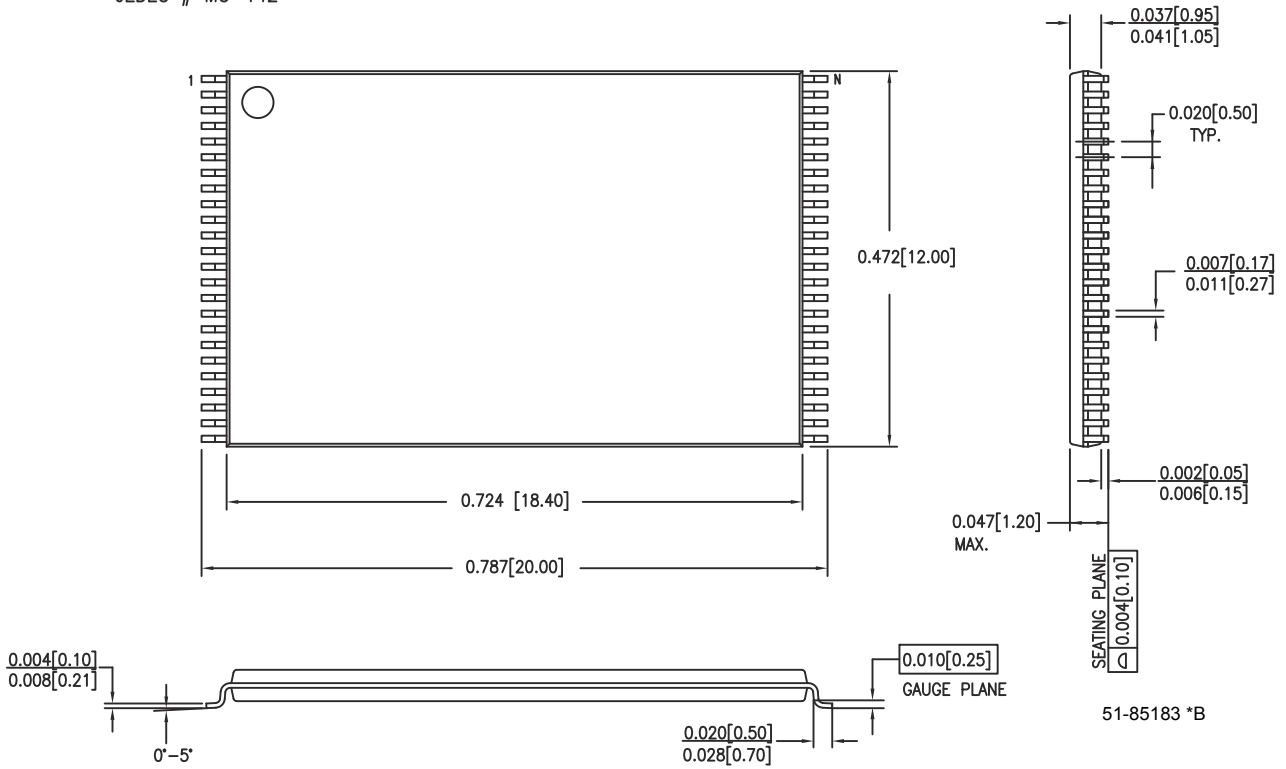


Package Diagram

Figure 9. 48-pin TSOP I (12 × 18.4 × 1.0 mm) Z48A, 51-85183

DIMENSIONS IN INCHES[MM] MIN.
MAX.

JEDEC # MO-142



Acronyms

Acronym	Description
BHE	byte high enable
BLE	byte low enable
CMOS	complementary metal oxide semiconductor
CE	chip enable
I/O	input/output
OE	output enable
SRAM	static random access memory
TSOP	thin small outline package
WE	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
μA	micro Amperes
mA	milli Amperes
mm	milli meter
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY62167E MoBL®, 16-Mbit (1 M × 16 / 2 M × 8) Static RAM Document Number: 001-15607				
Rev.	ECN No.	Issue Date	Orig. of Change	Description of Change
**	1103145	See ECN	VKN	New Data Sheet
*A	1138903	See ECN	VKN	Converted from preliminary to final Changed $I_{CC(max)}$ spec from 2.8 mA to 4.0 mA for $f=1$ MHz Changed $I_{CC(typ)}$ spec from 22 mA to 25 mA for $f=f_{max}$ Changed $I_{CC(max)}$ spec from 25 mA to 30 mA for $f=f_{max}$ Added footnote# 8 related to V_{IL} Changed I_{CCDR} spec from 10 μ A to 12 μ A Added footnote# 14 related to AC timing parameters
*B	2934385	06/03/10	VKN	Included \overline{BHE} , \overline{BLE} in I_{SB2} , I_{CCDR} test conditions to reflect byte power down feature Added footnote #35 related to chip enable Updated package diagram Updated template
*C	3279426	06/10/2011	RAME	Removed the Note "For best practice recommendations, refer to the Cypress application note AN1064, SRAM System Guidelines." in page 1 and its reference in Functional Description . Updated Switching Characteristics (changed the Min value of t_{LZBE} parameter). Updated in new template.

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