

Features

- Temperature range:
 - Commercial: 0 °C to 70 °C
 - Automotive-A: -40 °C to 85 °C
- High speed
 - $t_{AA} = 15 \text{ ns}$
- Low active power
 - 1540 mW (max.)
- Low CMOS standby power
 - 2.75 mW (max.)
- 2.0 V data retention (400 μW at 2.0 V retention)
- Automatic power-down when deselected
- TTL-compatible inputs and outputs
- Easy memory expansion with $\overline{\text{CE}}$ and $\overline{\text{OE}}$ features
- Available in Pb-free and non Pb-free 44-pin TSOP II and molded 44-pin (400-Mil) SOJ packages

Functional Description

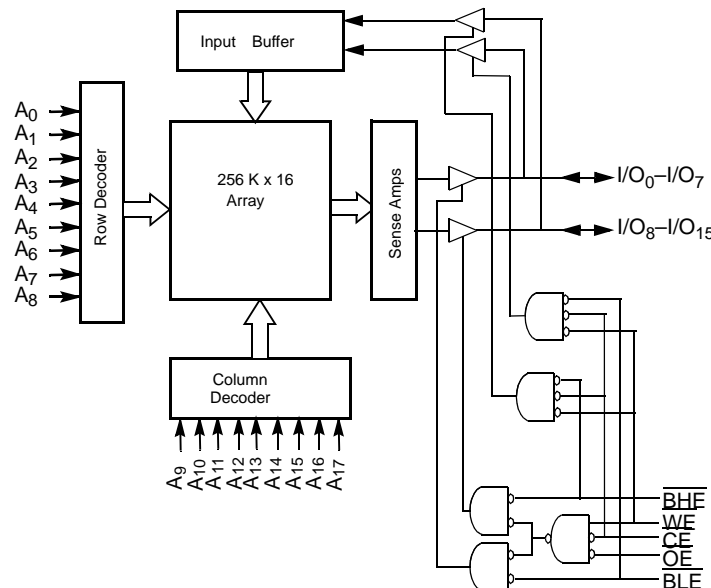
The CY7C1041BN is a high-performance CMOS static RAM organized as 262,144 words by 16 bits. Writing to the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Write Enable ($\overline{\text{WE}}$) inputs LOW. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from I/O pins (I/O_0 through I/O_7), is written into the location specified on the address pins (A_0 through A_{17}). If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from I/O pins (I/O_8 through I/O_{15}) is written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable ($\overline{\text{CE}}$) and Output Enable ($\overline{\text{OE}}$) LOW while forcing the Write Enable ($\overline{\text{WE}}$) HIGH. If Byte Low Enable ($\overline{\text{BLE}}$) is LOW, then data from the memory location specified by the address pins will appear on I/O_0 to I/O_7 . If Byte High Enable ($\overline{\text{BHE}}$) is LOW, then data from memory will appear on I/O_8 to I/O_{15} . See the truth table at the back of this data sheet for a complete description of read and write modes.

The input/output pins (I/O_0 through I/O_{15}) are placed in a high-impedance state when the device is deselected ($\overline{\text{CE}}$ HIGH), the outputs are disabled ($\overline{\text{OE}}$ HIGH), the $\overline{\text{BHE}}$ and $\overline{\text{BLE}}$ are disabled ($\overline{\text{BHE}}$, $\overline{\text{BLE}}$ HIGH), or during a write operation ($\overline{\text{CE}}$ LOW, and $\overline{\text{WE}}$ LOW).

The CY7C1041BN is available in a standard 44-pin 400-mil-wide body width SOJ and 44-pin TSOP II package with center power and ground (revolutionary) pinout.

Logic Block Diagram



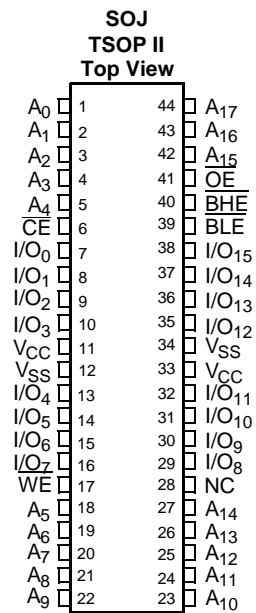
Contents

| | | | |
|--|----------|--|-----------|
| Selection Guide | 3 | Truth Table | 9 |
| Pin Configuration | 3 | Ordering Information | 10 |
| Maximum Ratings | 4 | Ordering Code Definitions | 10 |
| Operating Range | 4 | Package Diagrams | 11 |
| Electrical Characteristics | | Acronyms | 11 |
| Over the Operating Range | 4 | Document Conventions | 11 |
| Capacitance | 5 | Units of Measure | 11 |
| AC Test Loads and Waveforms | 5 | Sales, Solutions, and Legal Information | 13 |
| Switching Characteristics | | Worldwide Sales and Design Support | 13 |
| Over the Operating Range | 5 | Products | 13 |
| Data Retention Characteristics | | PSoC Solutions | 13 |
| Over the Operating Range (Commercial only) | 6 | | |
| Data Retention Waveform | 6 | | |
| Switching Waveforms | 7 | | |
| Read Cycle No. 1 | 7 | | |
| Read Cycle No. 2 (\overline{OE} Controlled) | 7 | | |
| Write Cycle No. 1 (\overline{CE} Controlled) | 8 | | |
| Write Cycle No. 2 (\overline{BLE} or \overline{BHE} Controlled) | 8 | | |
| Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW) | 9 | | |

Selection Guide

| Description | | -15 | -20 | Unit |
|------------------------------|--------------|-----|-----|------|
| Maximum access time | | 15 | 20 | ns |
| Maximum operating current | Commercial | 190 | 170 | mA |
| | Automotive-A | – | 190 | – |
| Maximum CMOS standby current | Commercial | 0.5 | 0.5 | mA |
| | Automotive-A | – | 6 | |

Pin Configuration



Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature -65 °C to +150 °C
 Ambient temperature with power applied -55 °C to +125 °C
 Supply voltage on V_{CC} to relative GND^[1].....-0.5 V to +7.0 V
 DC voltage applied to outputs in High Z State^[1].....-0.5 V to $V_{CC} + 0.5$ V
 DC input voltage^[1].....-0.5 V to $V_{CC} + 0.5$ V
 Current into outputs (LOW) 20 mA

Operating Range

| Range | Ambient Temperature ^[2] | V_{CC} |
|--------------|------------------------------------|-----------|
| Commercial | 0 °C to +70 °C | 5 V ± 0.5 |
| Automotive-A | -40 °C to +85 °C | |

Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | -15 | | -20 | | Unit | |
|-------------------------|---|---|--------|----------------|------|----------------|------|----|
| | | | Min | Max | Min | Max | | |
| V_{OH} | Output HIGH voltage | Min V_{CC} , $I_{OH} = -4.0$ mA | 2.4 | - | 2.4 | - | V | |
| V_{OL} | Output LOW voltage | Min V_{CC} , $I_{OL} = 8.0$ mA | - | 0.4 | - | 0.4 | V | |
| V_{IH} ^[1] | Input HIGH voltage | - | 2.2 | $V_{CC} + 0.5$ | 2.2 | $V_{CC} + 0.5$ | V | |
| V_{IL} ^[1] | Input LOW voltage | - | -0.5 | 0.8 | -0.5 | 0.8 | V | |
| I_{IX} | Input load current | $GND \leq V_{IN} \leq V_{CC}$ | -1 | +1 | -1 | +1 | μA | |
| I_{OZ} | Output leakage current | $GND \leq V_{OUT} \leq V_{CC}$, Output Disabled | -1 | +1 | -1 | +1 | μA | |
| I_{CC} | V_{CC} operating supply current | Max V_{CC} , $f = f_{MAX} = 1/t_{RC}$ | Comm'l | - | 190 | - | 170 | mA |
| | | | Auto-A | - | - | - | 190 | mA |
| I_{SB1} | Automatic CE Power-down current—TTL inputs | Max V_{CC} , $\overline{CE} \geq V_{IH}$, $V_{IN} \geq V_{IH}$ or $V_{IN} \leq V_{IL}$, $f = f_{MAX}$ | - | 40 | - | 40 | mA | |
| I_{SB2} | Automatic CE power-down current—CMOS inputs | Max V_{CC} , $\overline{CE} \geq V_{CC} - 0.3$ V, $V_{IN} \geq V_{CC} - 0.3$ V, or $V_{IN} \leq 0.3$ V, $f = 0$ | Comm'l | - | 0.5 | - | 0.5 | mA |
| | | | Auto-A | - | - | - | 6 | mA |

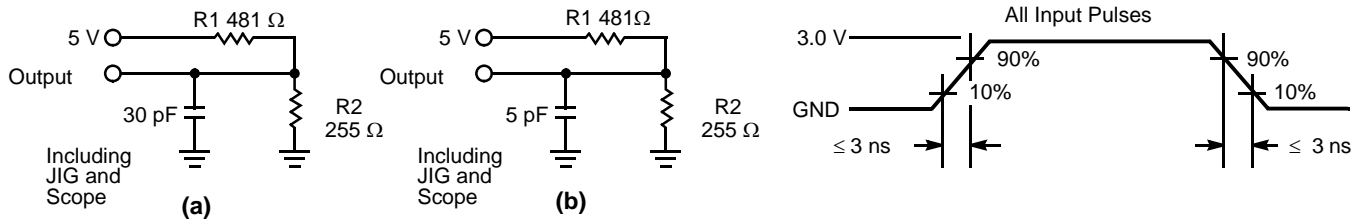
Notes

- V_{IL} (min.) = -2.0 V for pulse durations of less than 20 ns.
- T_A is the case temperature.

Capacitance

| Parameter ^[3] | Description | Test Conditions | Max | Unit |
|--------------------------|-------------------|---|-----|------|
| C _{IN} | Input capacitance | T _A = 25 °C, f = 1 MHz, V _{CC} = 5.0 V | 8 | pF |
| C _{OUT} | I/O capacitance | | 8 | pF |

AC Test Loads and Waveforms



Equivalent to: Thévenin Equivalent
 Output $\text{---} \frac{167\ \Omega}{\text{---}} \text{---} 1.73\ \text{V}$

Switching Characteristics^[4] Over the Operating Range

| Parameter | Description | -15 | | -20 | | Unit |
|--------------------|--|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | |
| Read Cycle | | | | | | |
| t _{power} | V _{CC} (typical) to the first access ^[5] | 1 | – | 1 | – | μs |
| t _{RC} | Read cycle time | 15 | – | 20 | – | ns |
| t _{AA} | Address to data valid | – | 15 | – | 20 | ns |
| t _{OHA} | Data hold from address change | 3 | – | 3 | – | ns |
| t _{ACE} | $\overline{\text{CE}}$ LOW to data valid | – | 15 | – | 20 | ns |
| t _{DOE} | $\overline{\text{OE}}$ LOW to data valid | – | 7 | – | 8 | ns |
| t _{LZOE} | $\overline{\text{OE}}$ LOW to low Z | 0 | – | 0 | – | ns |
| t _{HZOE} | $\overline{\text{OE}}$ HIGH to high Z ^[6, 7] | – | 7 | – | 8 | ns |
| t _{LZCE} | $\overline{\text{CE}}$ LOW to low Z ^[7] | 3 | – | 3 | – | ns |
| t _{HZCE} | $\overline{\text{CE}}$ HIGH to high Z ^[6, 7] | – | 7 | – | 8 | ns |
| t _{PU} | $\overline{\text{CE}}$ LOW to power-up | 0 | – | 0 | – | ns |
| t _{PD} | $\overline{\text{CE}}$ HIGH to power-down | – | 15 | – | 20 | ns |
| t _{DBE} | Byte enable to data valid | – | 7 | – | 8 | ns |
| t _{LZBE} | Byte enable to low Z | 0 | – | 0 | – | ns |
| t _{HZBE} | Byte disable to high Z | – | 7 | – | 8 | ns |

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5 V, input pulse levels of 0 to 3.0 V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
- This part has a voltage regulator which steps down the voltage from 5 V to 3.3 V internally. t_{power} time has to be provided initially before a read/write operation is started.
- t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
- At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.

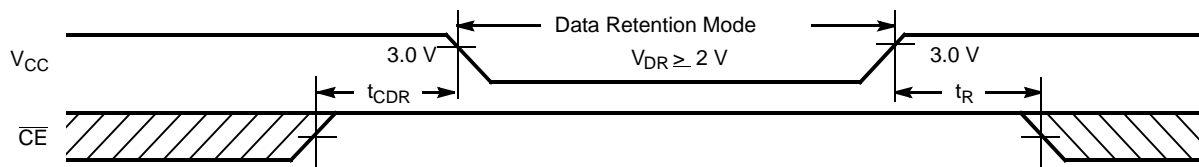
Switching Characteristics^[4] Over the Operating Range (continued)

| Parameter | Description | -15 | | -20 | | Unit |
|---------------------------------------|-------------------------------------|-----|-----|-----|-----|------|
| | | Min | Max | Min | Max | |
| Write Cycle^[11, 12] | | | | | | |
| t _{WC} | Write cycle time | 15 | – | 20 | – | ns |
| t _{SCE} | CE LOW to write end | 12 | – | 13 | – | ns |
| t _{AW} | Address setup to write end | 12 | – | 13 | – | ns |
| t _{HA} | Address hold from write end | 0 | – | 0 | – | ns |
| t _{SA} | Address setup to write start | 0 | – | 0 | – | ns |
| t _{PWE} | WE pulse width | 12 | – | 13 | – | ns |
| t _{SD} | Data setup to write end | 8 | – | 9 | – | ns |
| t _{HD} | Data hold from write end | 0 | – | 0 | – | ns |
| t _{LZWE} | WE HIGH to low Z ^[10] | 3 | – | 3 | – | ns |
| t _{HZWE} | WE LOW to high Z ^[9, 10] | – | 7 | – | 8 | ns |
| t _{BW} | Byte enable to end of write | 12 | – | 13 | – | ns |

Data Retention Characteristics Over the Operating Range (Commercial only)

| Parameter | Description | Conditions ^[14] | Min | Max | Unit |
|---------------------------------|--------------------------------------|---|-----------------|-----|------|
| V _{DR} | V _{CC} for data retention | – | 2.0 | – | V |
| I _{CCDR} | Data retention current | V _{CC} = V _{DR} = 2.0 V, CE ≥ V _{CC} – 0.3 V, | – | 200 | μA |
| t _{CDR} ^[8] | Chip deselect to data retention time | V _{IN} ≥ V _{CC} – 0.3 V or V _{IN} ≤ 0.3 V | 0 | – | ns |
| t _R ^[13] | Operation recovery time | | t _{RC} | – | ns |

Data Retention Waveform



Notes

8. Tested initially and after any design or process changes that may affect these parameters.
9. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
10. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}; t_{HZOE} is less than t_{LZOE}; and t_{HZWE} is less than t_{LZWE} for any given device.
11. The internal write time of the memory is defined by the overlap of CE LOW, and WE LOW. CE and WE must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
12. The minimum write cycle time for Write Cycle no. 3 (WE controlled, OE LOW) is the sum of t_{HZWE} and t_{SD}.
13. t_r ≤ 3 ns for the -15 speed. t_r ≤ 5 ns for the -20 and slower speeds.
14. No input may exceed V_{CC} + 0.5 V.

Switching Waveforms

Figure 1. Read Cycle No. 1^[15, 16]

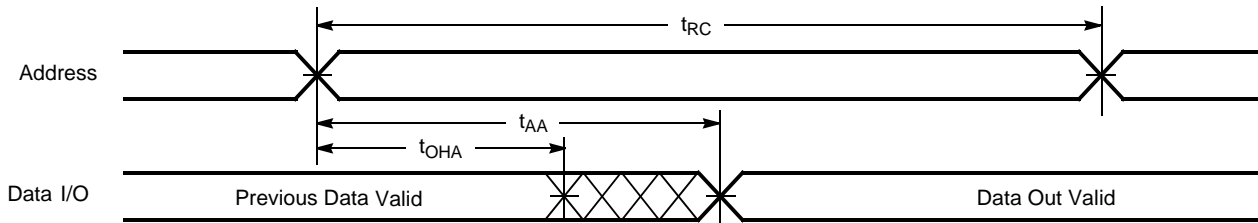
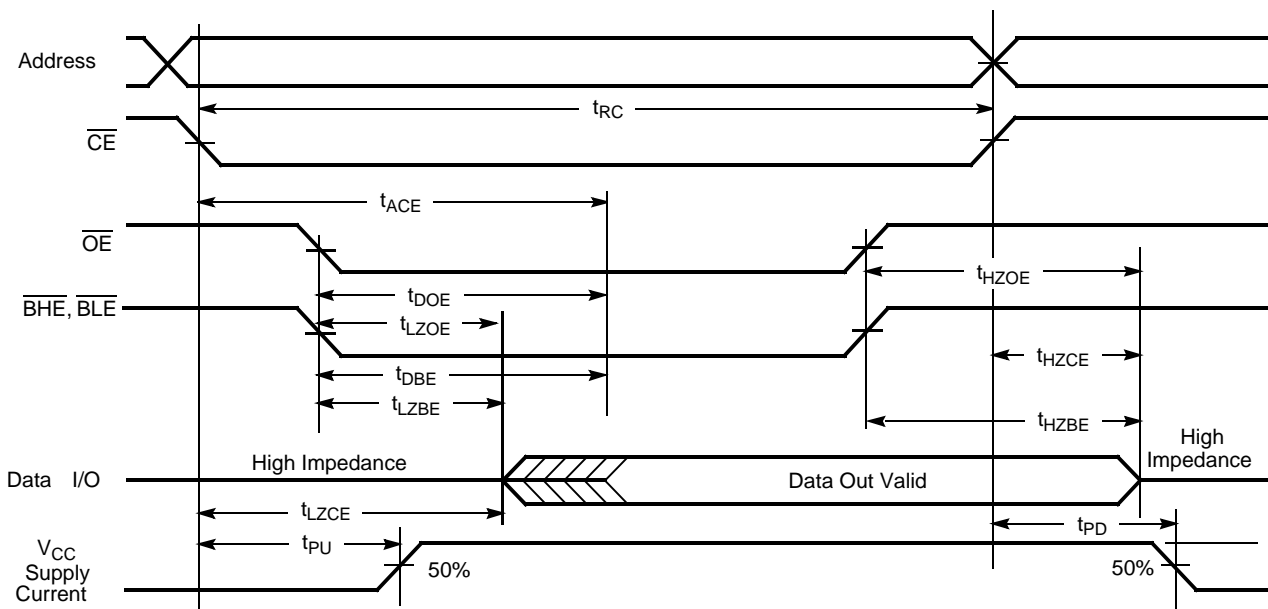


Figure 2. Read Cycle No. 2 (\overline{OE} Controlled)^[16, 17]



Notes

- 15. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} , and/or \overline{BLE} = V_{IL} .
- 16. \overline{WE} is HIGH for read cycle.
- 17. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Figure 3. Write Cycle No. 1 ($\overline{\text{CE}}$ Controlled)^[18, 19]

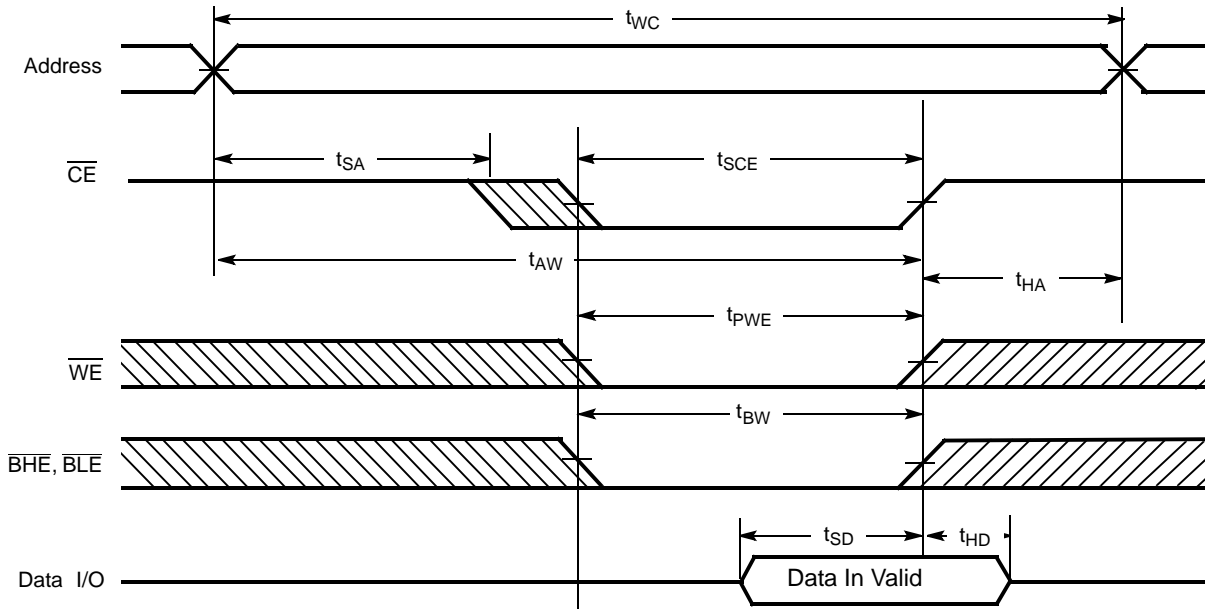
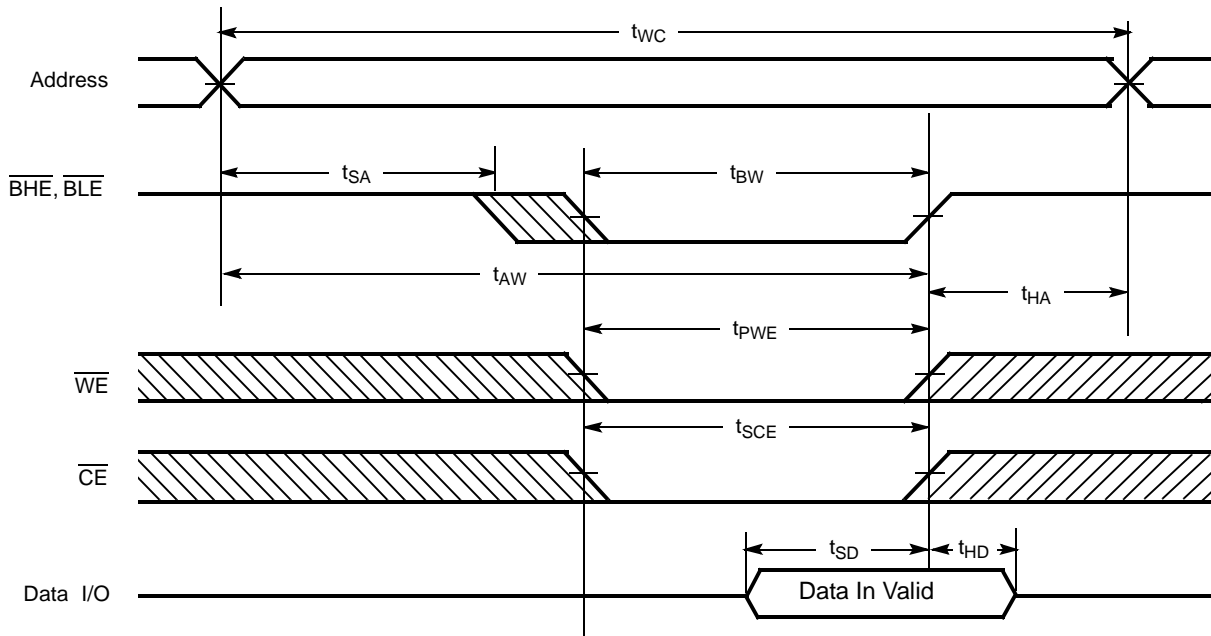


Figure 4. Write Cycle No. 2 ($\overline{\text{BLE}}$ or $\overline{\text{BHE}}$ Controlled)

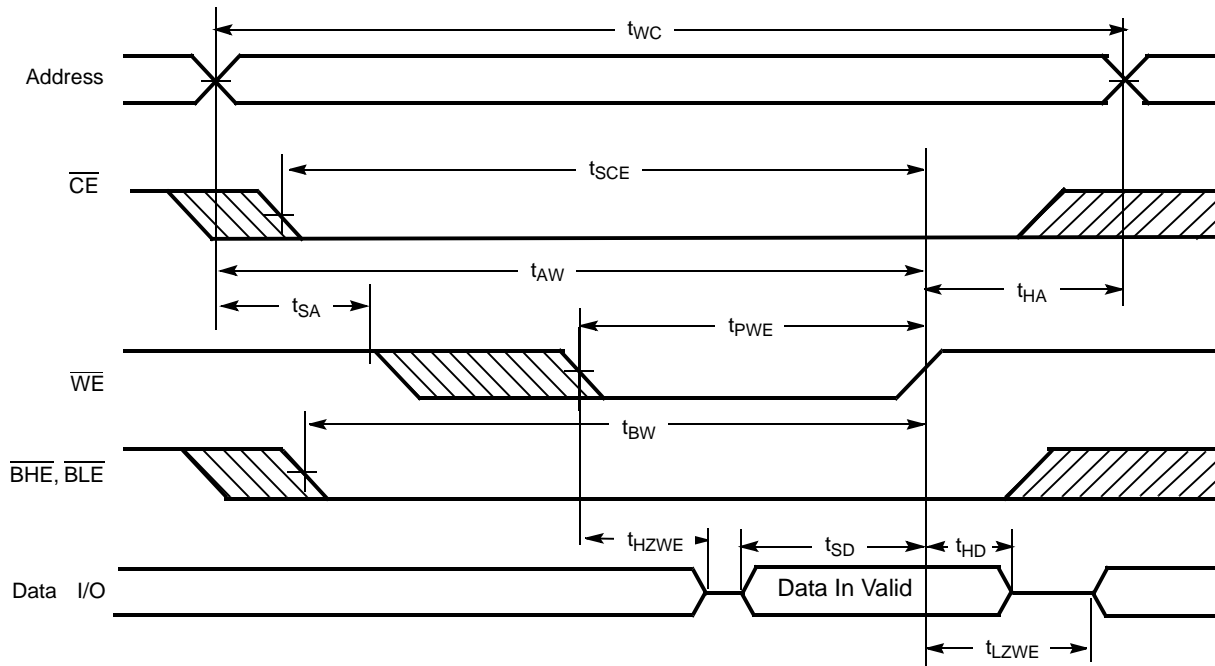


Notes

- 18. Data I/O is high impedance if $\overline{\text{OE}}$ or $\overline{\text{BHE}}$ and/or $\overline{\text{BLE}} = V_{IH}$.
- 19. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Figure 5. Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)



Truth Table

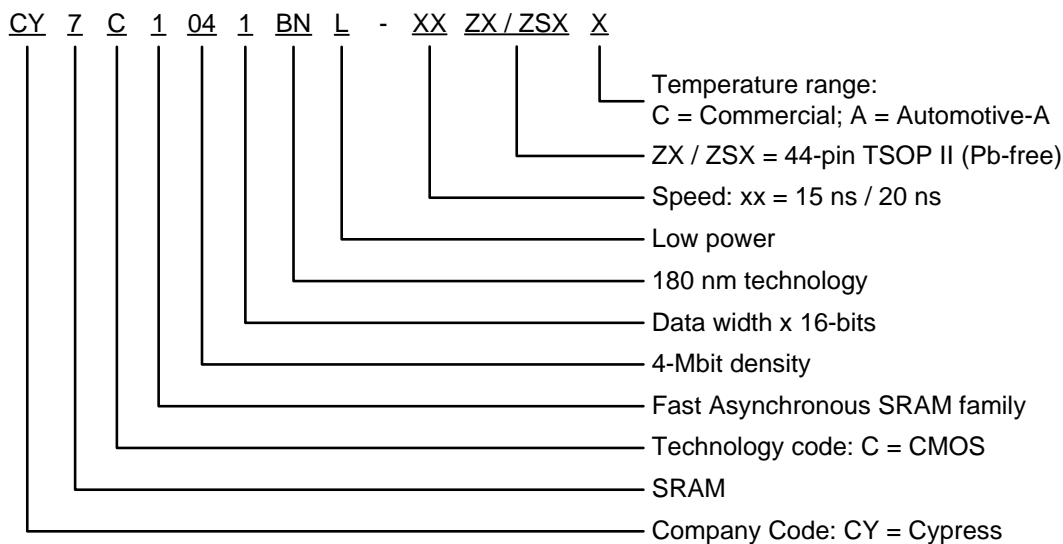
| \overline{CE} | \overline{OE} | \overline{WE} | \overline{BLE} | \overline{BHE} | I/O ₀ -I/O ₇ | I/O ₈ -I/O ₁₅ | Mode | Power |
|-----------------|-----------------|-----------------|------------------|------------------|------------------------------------|-------------------------------------|----------------------------|----------------------------|
| H | X | X | X | X | High Z | High Z | Power-down | Standby (I _{SB}) |
| L | L | H | L | L | Data out | Data out | Read all bits | Active (I _{CC}) |
| L | L | H | L | H | Data out | High Z | Read lower bits only | Active (I _{CC}) |
| L | L | H | H | L | High Z | Data out | Read upper bits only | Active (I _{CC}) |
| L | X | L | L | L | Data in | Data in | Write all bits | Active (I _{CC}) |
| L | X | L | L | H | Data in | High Z | Write lower bits only | Active (I _{CC}) |
| L | X | L | H | L | High Z | Data in | Write upper bits only | Active (I _{CC}) |
| L | H | H | X | X | High Z | High Z | Selected, Outputs disabled | Active (I _{CC}) |

Ordering Information

Cypress offers other versions of this type of product in many different configurations and features. The following table contains only the list of parts that are currently available. For a complete listing of all options, visit the Cypress website at <http://www.cypress.com> and refer to the product summary page at <http://www.cypress.com/products> or contact your local sales representative. Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives and distributors. To find the office closest to you, visit us at <http://www.cypress.com/go/datasheet/offices>.

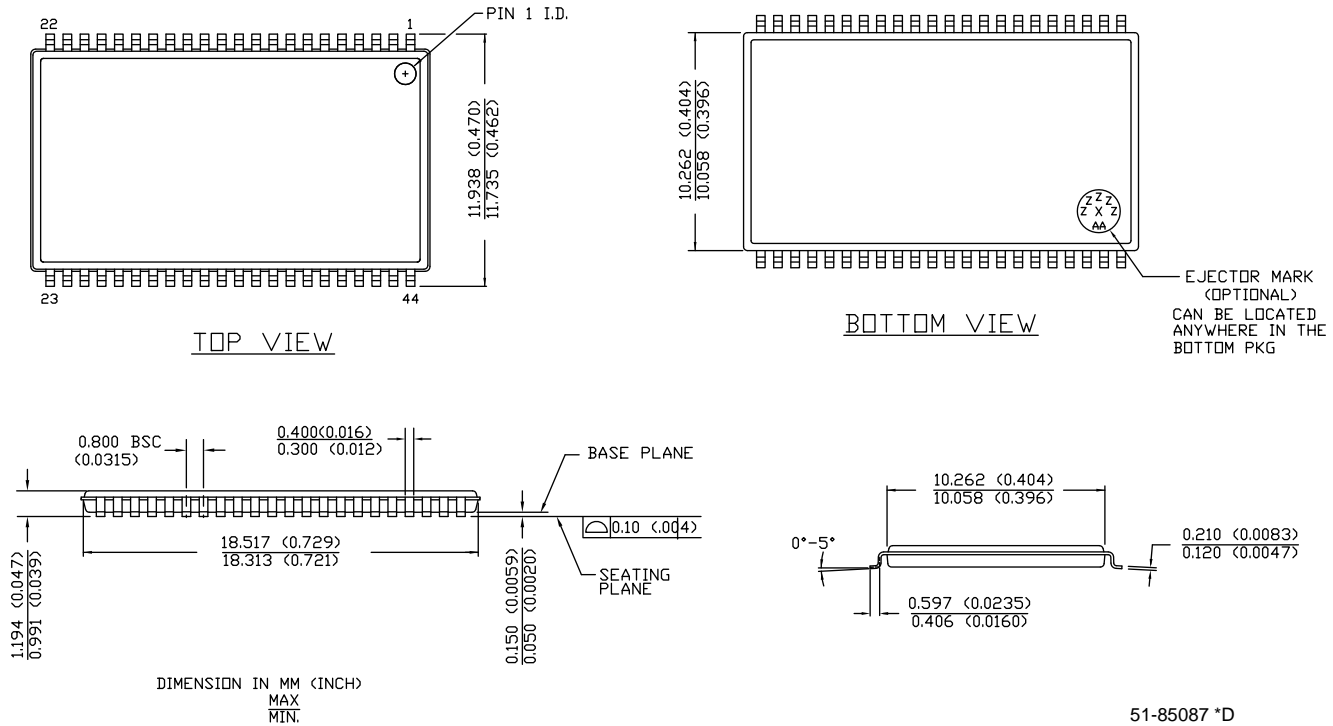
| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|------------|-------------------|--------------|-------------------------------|-----------------|
| 15 | CY7C1041BNL-15ZXC | 51-85087 | 44-pin TSOP Type II (Pb-free) | Commercial |
| 20 | CY7C1041BN-20ZSXA | | 44-pin TSOP Type II | Automotive-A |

Ordering Code Definitions



Package Diagrams

Figure 6. 44-Pin TSOP II (51-85087)



Acronyms

| Acronym | Description |
|---------|---|
| BHE | byte high enable |
| BLE | byte low enable |
| CE | chip enable |
| CMOS | complementary metal oxide semiconductor |
| I/O | input/output |
| OE | output enable |
| SRAM | static random access memory |
| TSOP | thin small outline package |
| WE | write enable |

Document Conventions

Units of Measure

| Symbol | Unit of Measure |
|--------|-----------------|
| ns | nanosecond |
| V | volt |
| μA | microampere |
| mA | milliampere |
| mV | millivolt |
| mW | milliwatt |
| MHz | megahertz |
| pF | picofarad |
| °C | degree Celsius |
| W | watt |

Document History Page

| Document Title: CY7C1041BN 256 K x 16 Static RAM Document Number: 001-06496 | | | | |
|--|---------|-----------------|-----------------|---|
| Revision | ECN | Orig. of Change | Submission Date | Description of Change |
| ** | 424111 | NXR | See ECN | New Data Sheets |
| *A | 498575 | NXR | See ECN | Added Automotive-A operating range updated Ordering Information Table |
| *B | 2897061 | AJU | 03/22/10 | Removed obsolete parts from ordering information table Updated package diagrams |
| *C | 2906679 | NXR | 04/07/10 | Removed inactive part CY7C1041BNL-20VXCT from the ordering information table. |
| *D | 3086674 | PRAS | 11/15/10 | Removed inactive parts (CY7C1041BN-15ZXI, CY7C1041BN-15VXI). Added Ordering Code Definition. |
| *E | 3232637 | PRAS | 04/20/2011 | Fixed unit for Input Load current and Output Leakage current under Electrical Characteristics table from mA to μ A. Updated template. Added Units table. |
| *F | 3383869 | TAVA | 09/26/2011 | Removed all references to Industrial information. All "Commercial-L" changed to "Commercial". Modified the notes in figures under Read cycle and Write cycle sections. Rearranged sections for better clarity. Revised package diagram. |

Sales, Solutions, and Legal Information

Worldwide Sales and Design Support

Cypress maintains a worldwide network of offices, solution centers, manufacturer's representatives, and distributors. To find the office closest to you, visit us at [Cypress Locations](#).

Products

| | |
|--|--|
| Automotive | cypress.com/go/automotive |
| Clocks & Buffers | cypress.com/go/clocks |
| Interface | cypress.com/go/interface |
| Lighting & Power Control | cypress.com/go/powerpsoc cypress.com/go/plc |
| Memory | cypress.com/go/memory |
| Optical & Image Sensing | cypress.com/go/image |
| PSoC | cypress.com/go/psoc |
| Touch Sensing | cypress.com/go/touch |
| USB Controllers | cypress.com/go/USB |
| Wireless/RF | cypress.com/go/wireless |

PSoC Solutions

[psoc.cypress.com/solutions](#)
PSoC 1 | PSoC 3 | PSoC 5

© Cypress Semiconductor Corporation, 2006-2011. The information contained herein is subject to change without notice. Cypress Semiconductor Corporation assumes no responsibility for the use of any circuitry other than circuitry embodied in a Cypress product. Nor does it convey or imply any license under patent or other rights. Cypress products are not warranted nor intended to be used for medical, life support, life saving, critical control or safety applications, unless pursuant to an express written agreement with Cypress. Furthermore, Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress products in life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Any Source Code (software and/or firmware) is owned by Cypress Semiconductor Corporation (Cypress) and is protected by and subject to worldwide patent protection (United States and foreign), United States copyright laws and international treaty provisions. Cypress hereby grants to licensee a personal, non-exclusive, non-transferable license to copy, use, modify, create derivative works of, and compile the Cypress Source Code and derivative works for the sole purpose of creating custom software and or firmware in support of licensee product to be used only in conjunction with a Cypress integrated circuit as specified in the applicable agreement. Any reproduction, modification, translation, compilation, or representation of this Source Code except as specified above is prohibited without the express written permission of Cypress.

Disclaimer: CYPRESS MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARD TO THIS MATERIAL, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE. Cypress reserves the right to make changes without further notice to the materials described herein. Cypress does not assume any liability arising out of the application or use of any product or circuit described herein. Cypress does not authorize its products for use as critical components in life-support systems where a malfunction or failure may reasonably be expected to result in significant injury to the user. The inclusion of Cypress' product in a life-support systems application implies that the manufacturer assumes all risk of such use and in doing so indemnifies Cypress against all charges.

Use may be limited by and subject to the applicable Cypress software license agreement.