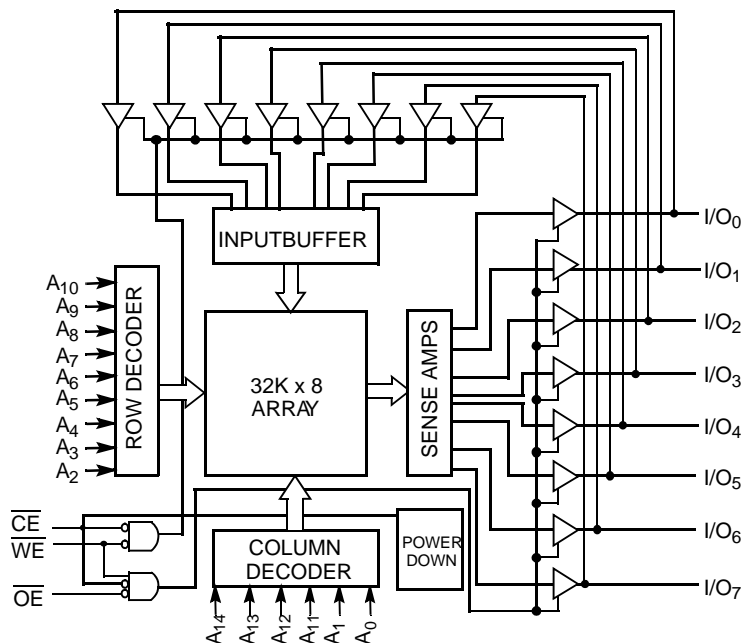


Features

- Temperature ranges
 - Commercial: 0 °C to +70 °C
 - Industrial: -40 °C to +85 °C
 - Automotive-A: -40 °C to +85 °C
 - Automotive-E: -40 °C to +125 °C
- Speed: 70 ns
- Low voltage range: 2.7 V to 3.6 V
- Low active power and standby power
- Easy memory expansion with \overline{CE} and \overline{OE} features
- TTL compatible inputs and outputs
- Automatic power-down when deselected
- CMOS for optimum speed and power
- Available in standard Pb-free and non Pb-free 28-pin (300-mil) narrow SOIC, 28-pin TSOP-I, and 28-pin reverse TSOP-I packages

Logic Block Diagram



Functional Description

The CY62256VN family is composed of two high performance CMOS static RAM's organized as 32K words by 8 bits. Easy memory expansion is provided by an active LOW chip enable (\overline{CE}) and active LOW output enable (\overline{OE}) and tristate drivers. These devices have an automatic power-down feature, reducing the power consumption by over 99% when deselected.

An active LOW write enable signal (\overline{WE}) controls the writing/reading operation of the memory. When \overline{CE} and \overline{WE} inputs are both LOW, data on the eight data input/output pins (I/O_0 through I/O_7) is written into the memory location addressed by the address present on the address pins (A_0 through A_{14}). Reading the device is accomplished by selecting the device and enabling the outputs, \overline{CE} and \overline{OE} active LOW, while \overline{WE} remains inactive or HIGH. Under these conditions, the contents of the location addressed by the information on address pins are present on the eight data input/output pins.

The input/output pins remain in a high impedance state unless the chip is selected, outputs are enabled, and write enable (\overline{WE}) is HIGH.

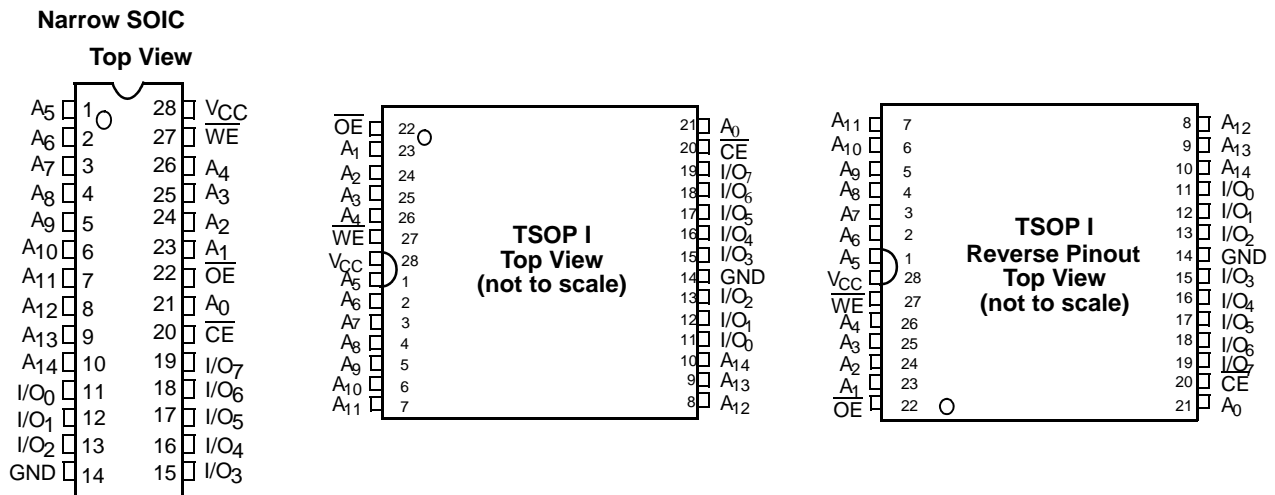
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Product Portfolio

Product	Range	V _{CC} Range (V)			Power Dissipation			
		Min	Typ ^[1]	Max	Operating, I _{CC} (mA)		Standby, I _{SB2} (μA)	
					Typ ^[1]	Max	Typ ^[1]	Max
CY62256VNLL	Commercial	2.7	3.0	3.6	11	30	0.1	5
CY62256VNLL	Industrial	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-A	2.7	3.0	3.6	11	30	0.1	10
CY62256VNLL	Automotive-E	2.7	3.0	3.6	11	30	0.1	130

Pin Configurations



Pin Definitions

Pin Number	Type	Description
1–10, 21, 23–26	Input	A ₀ –A ₁₄ . Address inputs
11–13, 15–19	Input/Output	I/O ₀ –I/O ₇ . Data lines. Used as input or output lines depending on operation.
27	Input/Control	WE. When selected LOW, a WRITE is conducted. When selected HIGH, a READ is conducted.
20	Input/Control	CE. When LOW, selects the chip. When HIGH, deselects the chip
22	Input/Control	OE. Output Enable. Controls the direction of the I/O pins. When LOW, the I/O pins behave as outputs. When deasserted HIGH, I/O pins are tristated, and act as input data pins
14	Ground	GND. Ground for the device
28	Power Supply	V _{CC} . Power supply for the device

Note

1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25 °C, and t_{AA} = 70 ns.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature	-65 °C to +150 °C
Ambient temperature with power applied	-55 °C to +125 °C
Supply voltage to ground potential (pin 28 to pin 14).....	-0.5 V to +4.6 V
DC voltage applied to outputs in high Z State ^[2]	-0.5 V to V _{CC} + 0.5 V
DC input voltage ^[2]	-0.5 V to V _{CC} + 0.5 V
Output current into outputs (LOW)	20 mA

Static discharge voltage..... > 2001 V
(per MIL-STD-883, method 3015)

Latch-up current

Operating Range

Device	Range	Ambient Temperature (T _A) ^[3]	V _{CC}
CY62256VN	Commercial	0 °C to +70 °C	2.7 V to 3.6 V
	Industrial	-40 °C to +85 °C	
	Automotive-A	-40 °C to +85 °C	
	Automotive-E	-40 °C to +125 °C	

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions	-70			Unit		
			Min	Typ ^[4]	Max			
V _{OH}	Output HIGH voltage	I _{OH} = -1.0 mA	V _{CC} = 2.7 V		2.4	-	-	V
V _{OL}	Output LOW voltage	I _{OL} = 2.1 mA	V _{CC} = 2.7 V		-	-	0.4	V
V _{IH}	Input HIGH voltage				2.2	-	V _{CC} + 0.3V	V
V _{IL}	Input LOW voltage				-0.5	-	0.8	V
I _{IX}	Input leakage current	GND ≤ V _{IN} ≤ V _{CC}	Commercial/ Industrial/ Automotive-A		-1	-	+1	μA
			Automotive-E		-10	-	+10	μA
I _{OZ}	Output leakage current	GND ≤ V _{IN} ≤ V _{CC} , Output Disabled	Commercial/ Industrial/ Automotive-A		-1	-	+1	μA
			Automotive-E		-10	-	+10	μA
I _{CC}	V _{CC} operating supply current	V _{CC} = 3.6 V, I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	All ranges		-	11	30	mA
I _{SB1}	Automatic CE power-down current - TTL inputs	V _{CC} = 3.6 V, $\overline{CE} \geq V_{IH}$, V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	All ranges		-	100	300	μA
I _{SB2}	Automatic CE power-down current - CMOS inputs	V _{CC} = 3.6 V, $\overline{CE} \geq V_{CC} - 0.3$ V, V _{IN} ≥ V _{CC} - 0.3 V or V _{IN} ≤ 0.3 V, f = 0	Commercial		-	0.1	5	μA
			Industrial/ Automotive-A		-		10	
			Automotive-E		-		130	

Notes

- V_{IL} (min) = -2.0 V for pulse durations of less than 20 ns.
- T_A is the "Instant-On" case temperature.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25 °C, and t_{AA} = 70 ns.

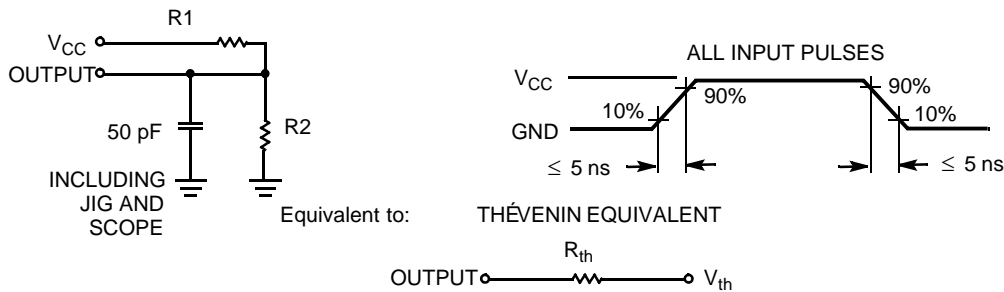
Capacitance

Parameter ^[5]	Description	Test Conditions	Max	Unit
C _{IN}	Input capacitance	T _A = 25 °C, f = 1 MHz, V _{CC} = 3.0 V	6	pF
C _{OUT}	Output capacitance		8	pF

Thermal Resistance

Parameter ^[5]	Description	Test Conditions	SOIC	TSOPI	RTSOPI	Unit
θ _{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	68.45	87.62	87.62	°C/W
θ _{JC}	Thermal resistance (junction to case)		26.94	23.73	23.73	°C/W

Figure 1. AC Test Loads and Waveforms



Parameter	Value	Units
R1	1100	Ohms
R2	1500	Ohms
R _{TH}	645	Ohms
V _{TH}	1.750	Volts

Data Retention Characteristics

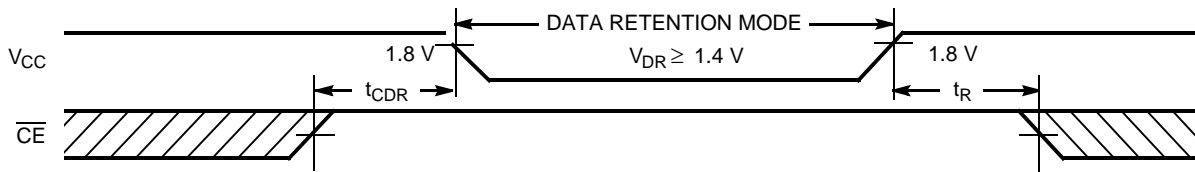
Over the Operating Range

Parameter	Description	Conditions ^[6]	Min	Typ ^[7]	Max	Unit
V _{DR}	V _{CC} for data retention		1.4	–	–	V
I _{CCDR}	Data retention current	V _{CC} = 1.4 V, CE ≥ V _{CC} – 0.3 V, V _{IN} ≥ V _{CC} – 0.3 V or V _{IN} ≤ 0.3 V	Commercial Industrial/ Automotive-A Automotive-E	– 0.1 –	3 6 50	μA
t _{CDR} ^[6]	Chip deselect to data retention time		0	–	–	ns
t _R ^[5]	Operation recovery time		70	–	–	ns

Notes

- Tested initially and after any design or process changes that may affect these parameters.
- No input may exceed V_{CC} + 0.3 V.
- Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25 °C, and t_{AA} = 70 ns.

Figure 2. Data Retention Waveform



Switching Characteristics

Over the Operating Range

Parameter ^[8]	Description	CY62256VN-70		Unit
		Min	Max	
Read Cycle				
t _{RC}	Read cycle time	70	–	ns
t _{AA}	Address to data valid	–	70	ns
t _{OHA}	Data hold from address change	10	–	ns
t _{ACE}	$\overline{\text{CE}}$ LOW to data valid	–	70	ns
t _{DOE}	$\overline{\text{OE}}$ LOW to data valid	–	35	ns
t _{LZOE}	$\overline{\text{OE}}$ LOW to low Z ^[9]	5	–	ns
t _{HZOE}	$\overline{\text{OE}}$ HIGH to high Z ^[9, 10]	–	25	ns
t _{LZCE}	$\overline{\text{CE}}$ LOW to low Z ^[9]	10	–	ns
t _{HZCE}	$\overline{\text{CE}}$ HIGH to high Z ^[9, 10]	–	25	ns
t _{PU}	$\overline{\text{CE}}$ LOW to power-up	0	–	ns
t _{PD}	$\overline{\text{CE}}$ HIGH to power-down	–	70	ns
Write Cycle^[11, 12]				
t _{WC}	Write cycle time	70	–	ns
t _{SCE}	$\overline{\text{CE}}$ LOW to write end	60	–	ns
t _{AW}	Address setup to write end	60	–	ns
t _{HA}	Address hold from write end	0	–	ns
t _{SA}	Address setup to write start	0	–	ns
t _{PWE}	$\overline{\text{WE}}$ pulse width	50	–	ns
t _{SD}	Data setup to write end	30	–	ns
t _{HD}	Data hold from write end	0	–	ns
t _{HZWE}	$\overline{\text{WE}}$ LOW to high Z ^[9, 10]	–	25	ns
t _{LZWE}	$\overline{\text{WE}}$ HIGH to low Z ^[9]	10	–	ns

Notes

8. Test conditions assume signal transition time of 5 ns or less timing reference levels of $V_{CC}/2$, input pulse levels of 0 to V_{CC} , and output loading of the specified I_{OL}/I_{OH} and 100-pF load capacitance.
9. At any temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any device.
10. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ± 200 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. The minimum write cycle time for write cycle #3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Figure 3. Read Cycle No. 1^[13, 14]

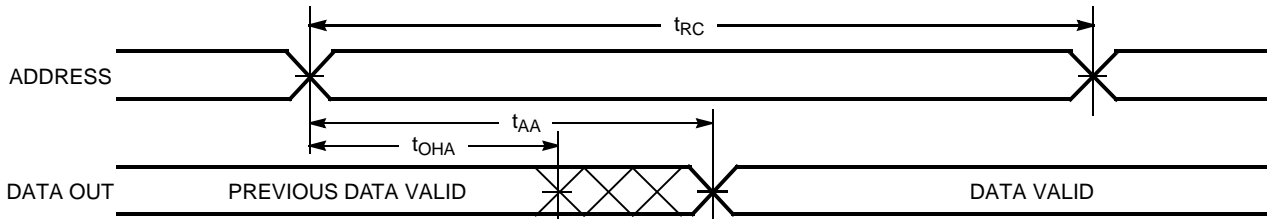


Figure 4. Read Cycle No. 2^[14, 15]

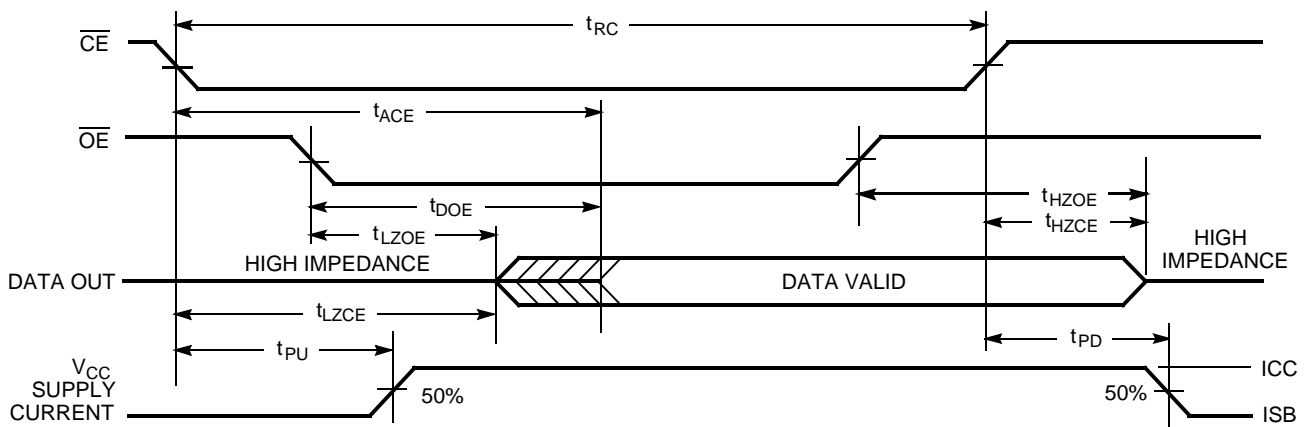
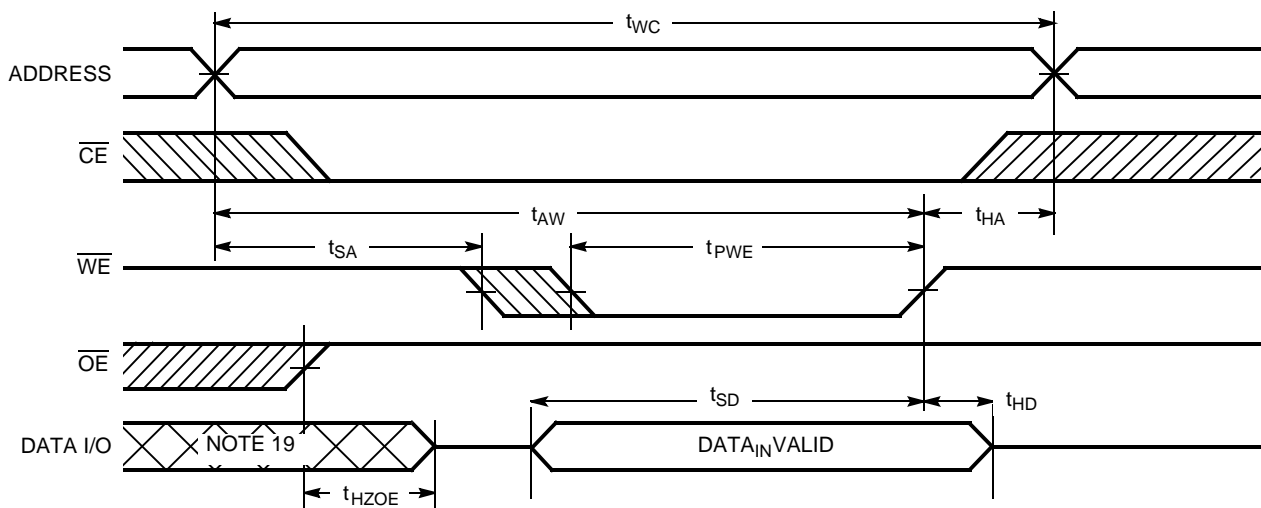


Figure 5. Write Cycle No. 1 (\overline{WE} Controlled)^[16, 17, 18]



Notes

- 13. Device is continuously selected. $\overline{OE}, \overline{CE} = V_{IL}$.
- 14. \overline{WE} is HIGH for read cycle.
- 15. Address valid prior to or coincident with \overline{CE} transition LOW.
- 16. The internal write time of the memory is defined by the overlap of \overline{CE} LOW and \overline{WE} LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 17. Data I/O is high impedance if $OE = V_{IH}$.
- 18. If \overline{CE} goes HIGH simultaneously with \overline{WE} HIGH, the output remains in a high impedance state.
- 19. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Figure 6. Write Cycle No. 2 ($\overline{\text{CE}}$ Controlled)^[20, 21, 22]

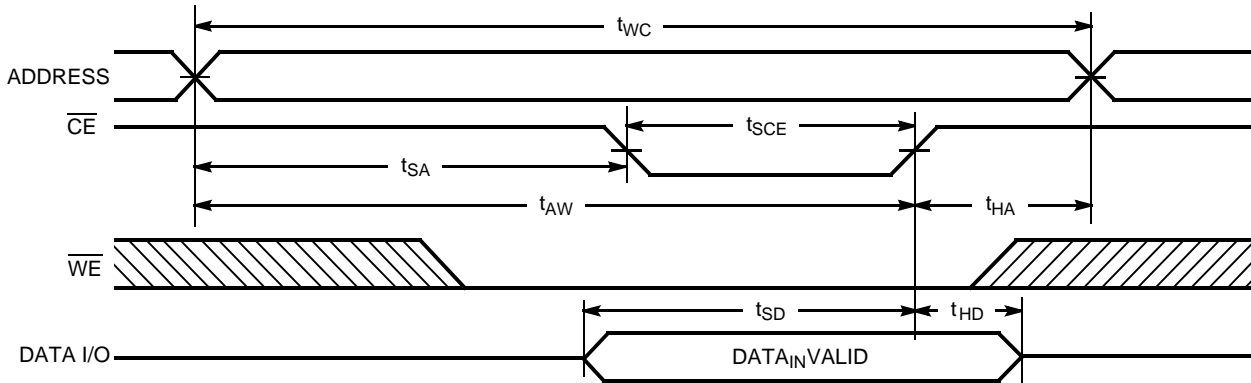
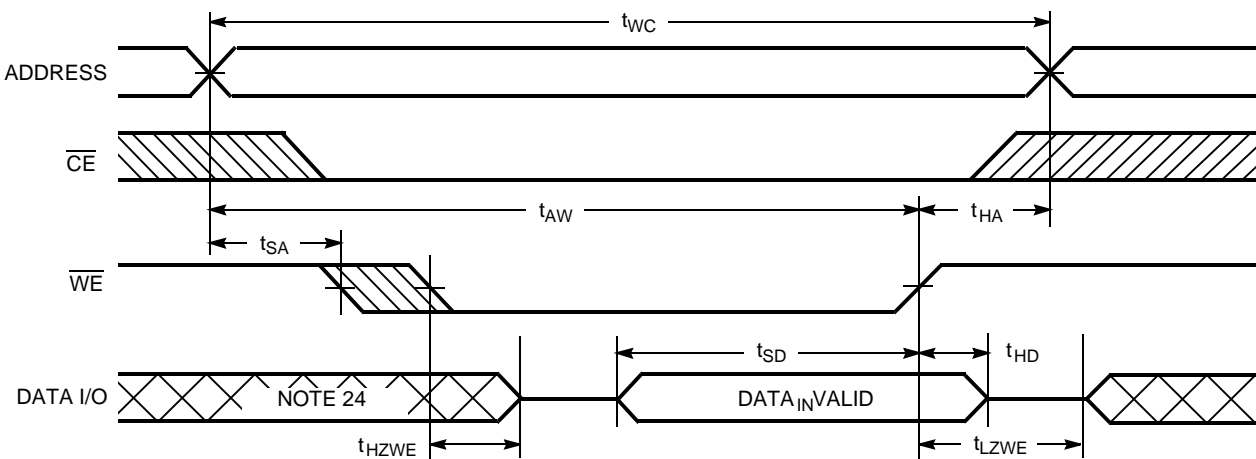


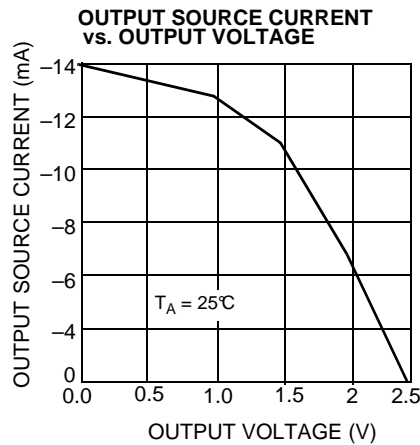
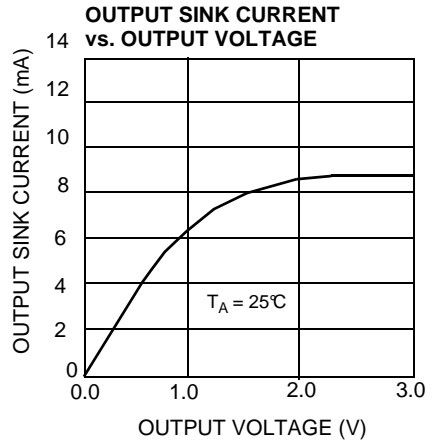
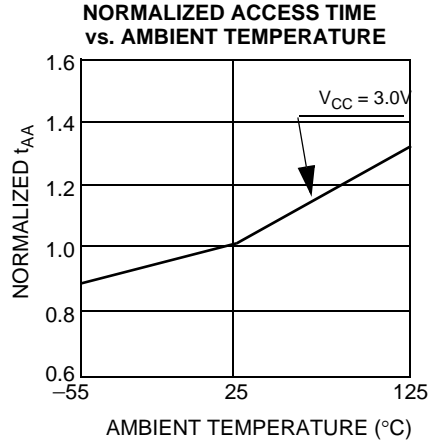
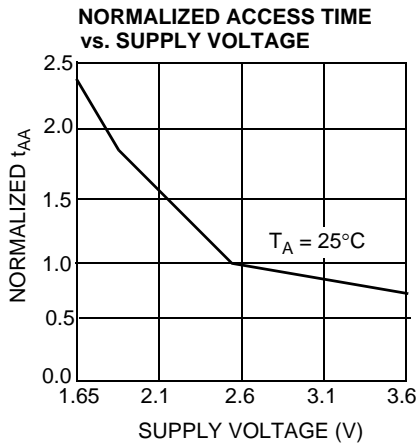
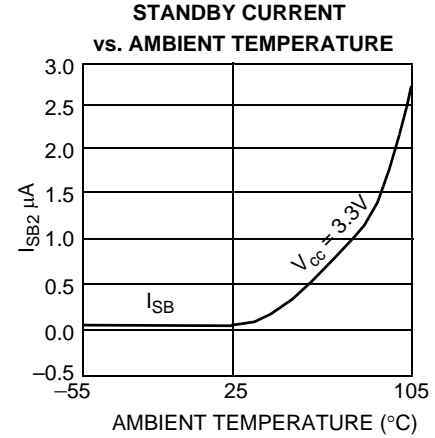
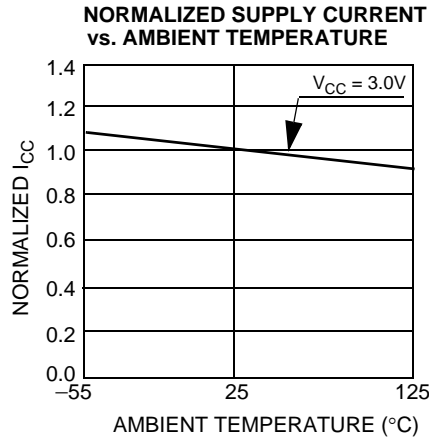
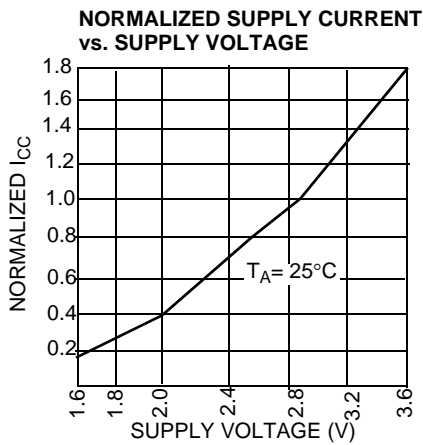
Figure 7. Write Cycle No. 3 ($\overline{\text{WE}}$ Controlled, $\overline{\text{OE}}$ LOW)^[22, 23]



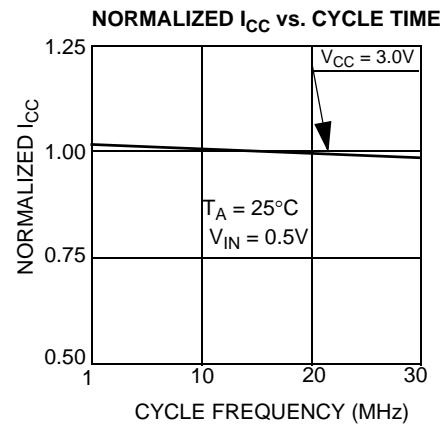
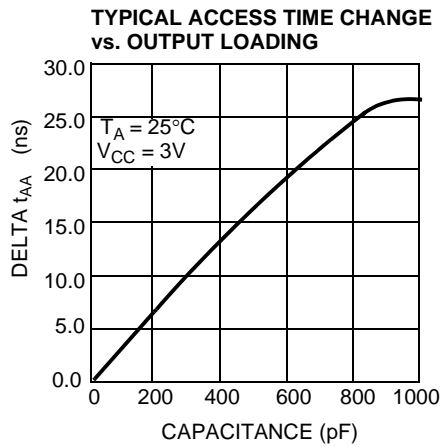
Notes

- 20. The internal write time of the memory is defined by the overlap of $\overline{\text{CE}}$ LOW and $\overline{\text{WE}}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
- 21. Data I/O is high impedance if $\text{OE} = V_{IH}$.
- 22. If $\overline{\text{CE}}$ goes HIGH simultaneously with $\overline{\text{WE}}$ HIGH, the output remains in a high impedance state.
- 23. The minimum write cycle time for write cycle #3 ($\overline{\text{WE}}$ controlled, $\overline{\text{OE}}$ LOW) is the sum of t_{HZWE} and t_{SD} .
- 24. During this period, the I/Os are in output state and input signals should not be applied.

Typical DC and AC Characteristics



Typical DC and AC Characteristics (continued)



Truth Table

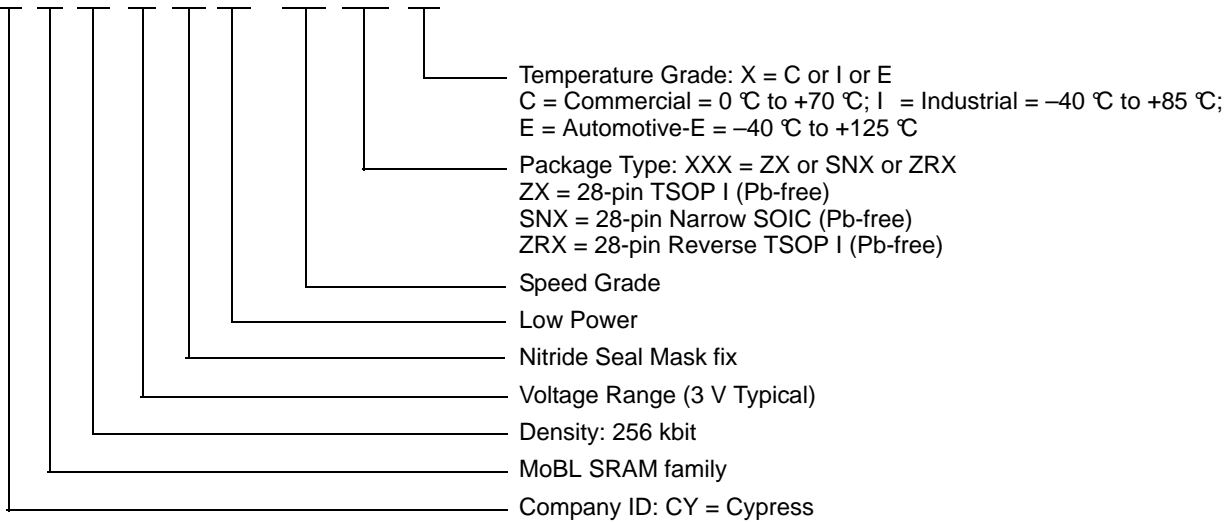
$\overline{\text{CE}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Inputs/Outputs	Mode	Power
H	X	X	High Z	Deselect/power-down	Standby (I _{SB})
L	H	L	Data out	Read	Active (I _{CC})
L	L	X	Data in	Write	Active (I _{CC})
L	H	H	High Z	Deselect, output disabled	Active (I _{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62256VNLL-70ZXC	51-85071	28-pin TSOP I (Pb-free)	Commercial
	CY62256VNLL-70SNXI	51-85092	28-pin (300-mil) narrow SOIC (Pb-free)	Industrial
	CY62256VNLL-70ZXI	51-85071	28-pin TSOP I (Pb-free)	
	CY62256VNLL-70ZRXI	51-85074	28-pin reverse TSOP I (Pb-free)	
	CY62256VNLL-70SNXE	51-85092	28-pin (300-mil) narrow SOIC (Pb-free)	Automotive-E
	CY62256VNLL-70ZXE	51-85071	28-pin TSOP I (Pb-free)	

Ordering Code Definitions

CY 62 256 V N LL - 70 XXX X



Package Diagrams

Figure 8. 28-pin (300-mil) SNC (Narrow Body), 51-85092

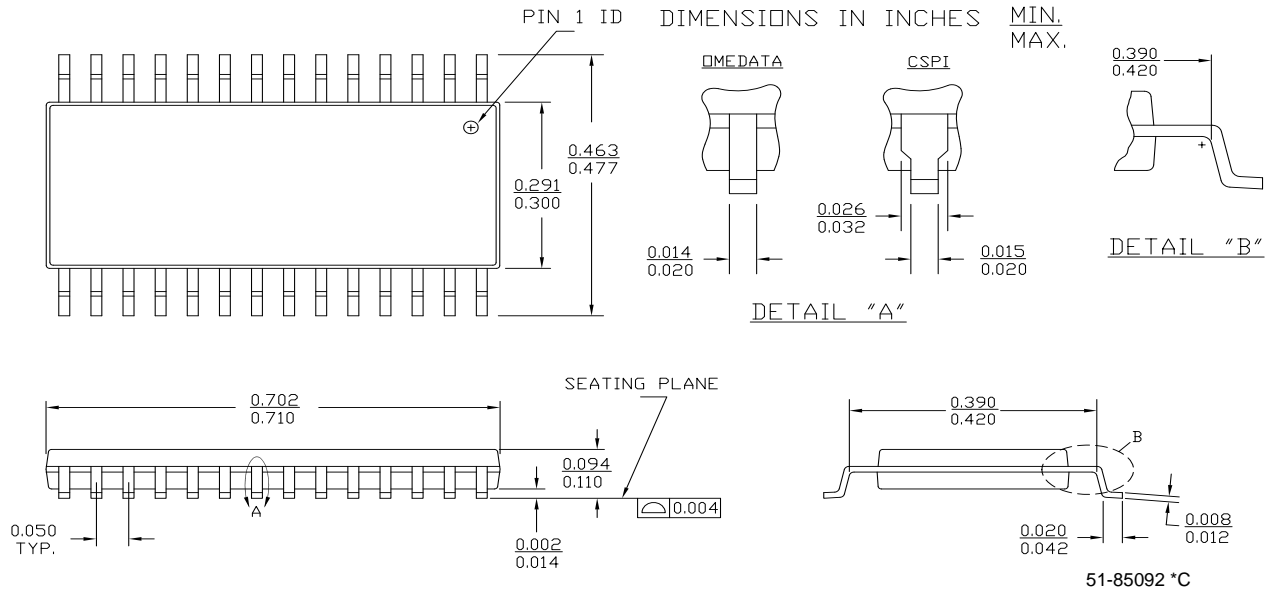


Figure 9. 28-pin TSOP 1 (8 x 13.4 mm), 51-85071

NOTE: ORIENTATION I.D. MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2

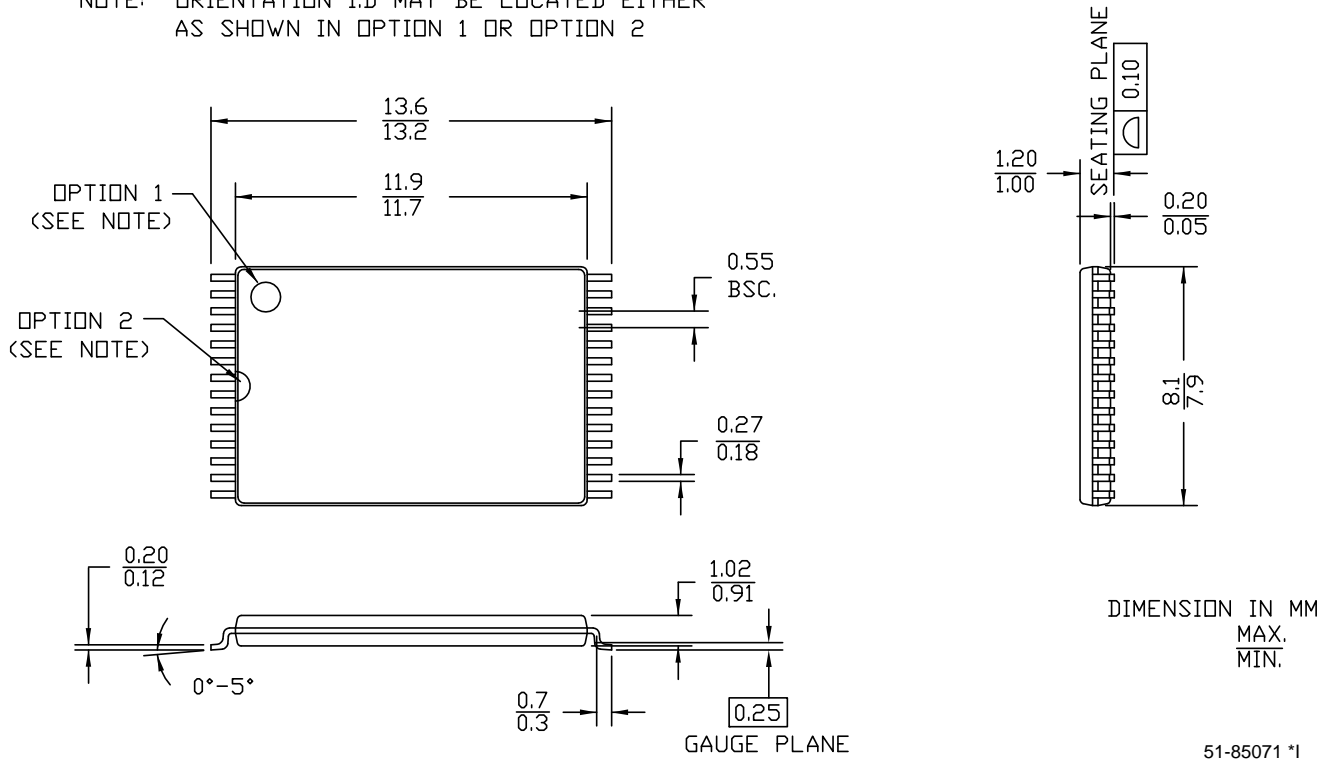
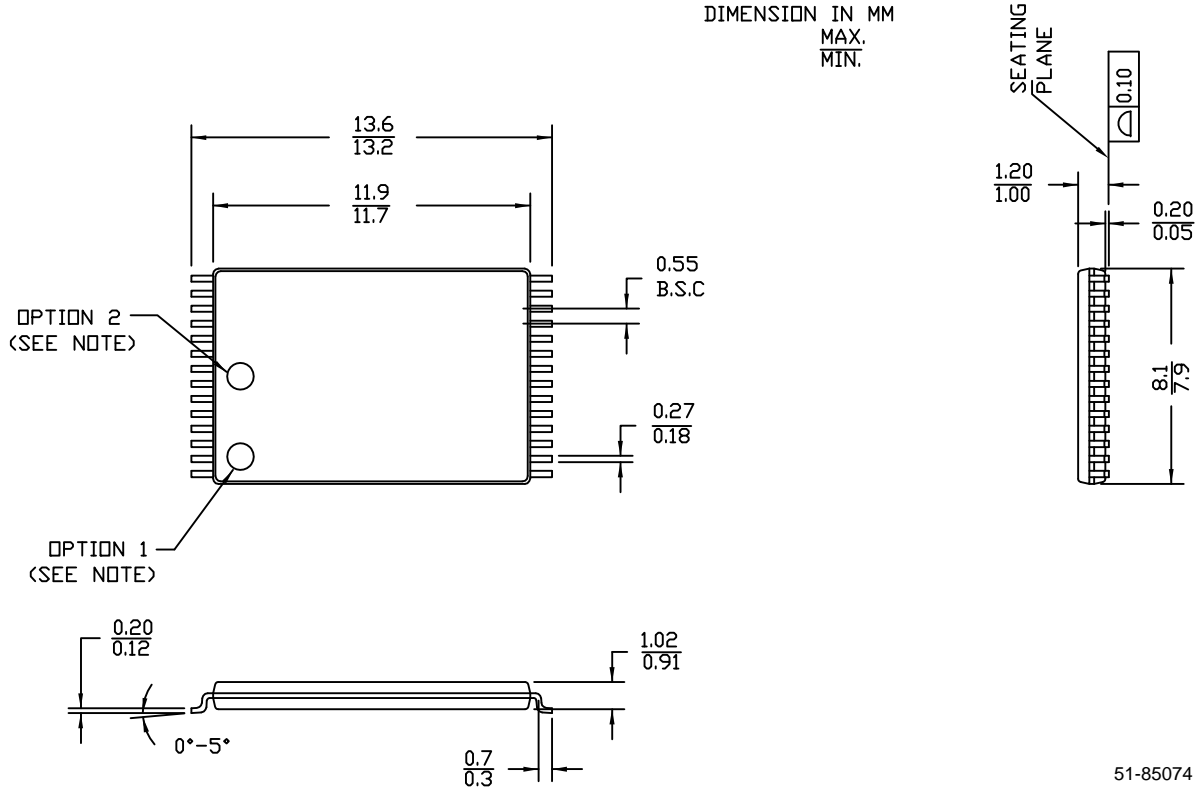


Figure 10. 28-pin Reverse TSOP 1 (8 x 13.4 mm), 51-85074

NOTE: ORIENTATION I.D MAY BE LOCATED EITHER AS SHOWN IN OPTION 1 OR OPTION 2



Reference Information

Acronyms

Acronym	Description
CMOS	complementary metal oxide semiconductor
I/O	input/output
SRAM	static random access memory
VFBGA	very fine ball grid array
TSOP	thin small outline package

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degrees Celsius
μA	microampere
mA	milliampere
MHz	megahertz
ns	nanosecond
pF	picofarad
V	volt
Ω	ohm
W	watt

Document History Page

Document Title: CY62256VN 256 K (32 K x 8) Static RAM Document Number: 001-06512				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	426504	NXR	See ECN	New Data Sheet
*A	488954	NXR	See ECN	Added Automotive product Updated ordering Information table
*B	2769239	VKN/AESA	09/25/09	Corrected V _{IL} description in the Electrical Characteristics table
*C	2901521	AJU	03/30/2010	Removed inactive parts from Ordering Information. Updated Package Diagram
*D	3119519	AJU	01/04/2011	Updated Ordering Information . Added Ordering Code Definitions .
*E	3329873	RAME	07/27/11	Updated template and styles according to current Cypress standards. Added acronyms and units. Removed reference to AN1064 SRAM system guidelines. Updated operation recovery time parameter under Data Retention Characteristics on page 5 .

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