CY62128EV30 MoBL®

1-Mbit (128 K × 8) Static RAM

Features

- Very high speed: 45 ns
- Temperature ranges:
  - Industrial: –40 °C to +85 °C
- Wide voltage range: 2.2 V to 3.6 V
- Pin compatible with CY62128DV30
- Ultra low standby power
  - Typical standby current: 1 µA
  - Maximum standby current: 4 µA
- Ultra low active power
  - Typical active current: 1.3 mA at f = 1 MHz
- Easy memory expansion with $\overline{CE}_1$, CE_2, and $\overline{OE}$ features
- Automatic power-down when deselected
- Complementary metal oxide semiconductor (CMOS) for optimum speed and power
- Offered in Pb-free 32-pin SOIC, 32-pin thin small outline package (TSOP) Type I, and 32-pin shrunk thin small outline package (STSOP) packages

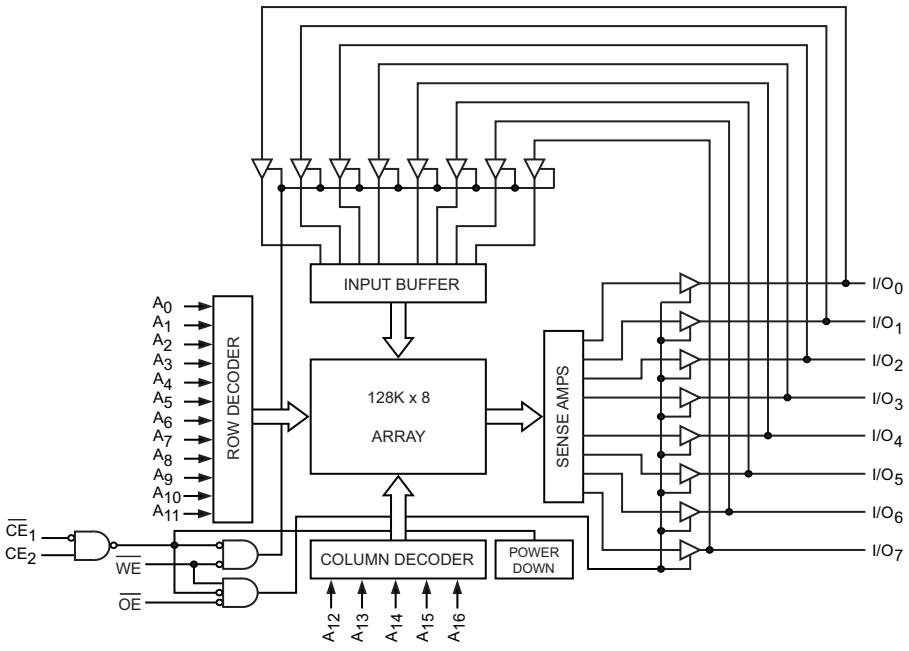
Functional Description

The CY62128EV30 is a high performance CMOS static RAM module organized as 128K words by 8-bits. This device features advanced circuit design to provide ultra low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. Placing the device in standby mode reduces power consumption by more than 99 percent when deselected ($\overline{CE}_1$ HIGH or CE_2 LOW). The eight input and output pins (I/O_0 through I/O_7) are placed in a high impedance state when the device is deselected ($\overline{CE}_1$ HIGH or CE_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or a write operation is in progress ($\overline{CE}_1$ LOW and CE_2 HIGH and $\overline{WE}$ LOW).

To write to the device, take chip enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and write enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins is then written into the location specified on the address pin (A_0 through A_{16}).

To read from the device, take chip enable ($\overline{CE}_1$ LOW and CE_2 HIGH) and output enable ($\overline{OE}$) LOW while forcing write enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins appear on the I/O pins.

Logic Block Diagram



Contents

Pin Configuration **3**
Product Portfolio **3**
Maximum Ratings **4**
Operating Range **4**
Electrical Characteristics **4**
Capacitance **5**
Thermal Resistance **5**
AC Test Loads and Waveforms **5**
Data Retention Characteristics **6**
Data Retention Waveform **6**
Switching Characteristics **7**
Switching Waveforms **8**
Truth Table **11**
Ordering Information **12**
Ordering Code Definitions 12
Package Diagrams **13**
Acronyms **16**
Document Conventions **16**
Units of Measure 16
Document History Page **17**
Sales, Solutions, and Legal Information **18**
Worldwide Sales and Design Support 18
Products 18
PSoC Solutions 18

Pin Configuration

Figure 1. 32-pin STSOP [1]

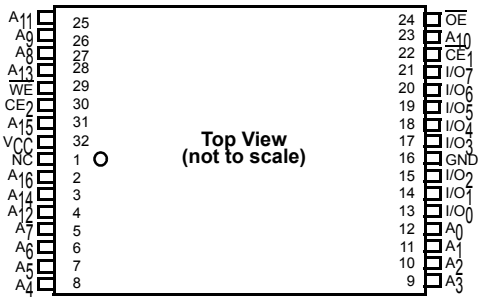


Figure 2. 32-pin TSOP I [1]

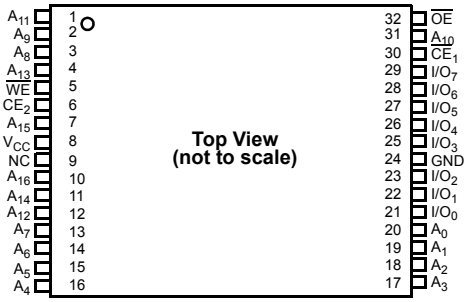
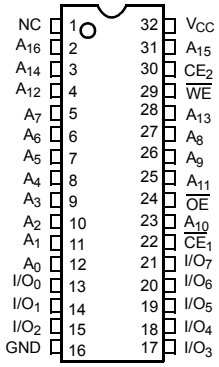


Figure 3. 32-pin SOIC [1]

Top View



Product Portfolio

Product	Range	V_{CC} Range (V)			Speed (ns)	Power Dissipation					
						Operating I_{CC} (mA)				Standby I_{SB2} (µA)	
						f = 1 MHz		f = f_{max}			
		Min	Typ [2]	Max		Typ [2]	Max	Typ [2]	Max	Typ [2]	Max
CY62128EV30LL	Industrial	2.2	3.0	3.6	45	1.3	2.0	11	16	1	4

Notes
1. NC pins are not connected on the die.
2. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. User guidelines are not tested.

Storage temperature ..... –65 °C to +150 °C

Ambient temperature with power applied ..... –55 °C to +125 °C

Supply voltage to ground potential .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC voltage applied to outputs in high Z State [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

DC input voltage [3, 4] .....–0.3 V to $V_{CC(max)}$ + 0.3 V

Output current into outputs (LOW) ..... 20 mA

Static discharge voltage (MIL-STD-883, method 3015) ..... > 2001 V

Latch-up current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}[5]
CY62128EV30LL	Industrial	–40 °C to +85 °C	2.2 V to 3.6 V

Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		45 ns (Industrial)			Unit
				Min	Typ [6]	Max	
V_{OH}	Output HIGH voltage	I_{OH} = –0.1 mA		2.0	–	–	V
		I_{OH} = –1.0 mA, $V_{CC} \geq$ 2.70 V		2.4	–	–	V
V_{OL}	Output LOW voltage	I_{OL} = 0.1 mA		–	–	0.4	V
		I_{OL} = 2.1 mA, $V_{CC} \geq$ 2.70 V		–	–	0.4	V
V_{IH}	Input HIGH voltage	V_{CC} = 2.2 V to 2.7 V		1.8	–	V_{CC} + 0.3 V	V
		V_{CC}= 2.7 V to 3.6 V		2.2	–	V_{CC} + 0.3 V	V
V_{IL}	Input LOW voltage	V_{CC} = 2.2 V to 2.7 V		–0.3	–	0.6	V
		V_{CC}= 2.7 V to 3.6 V		–0.3	–	0.8	V
I_{IX}	Input leakage current	GND $\leq V_I \leq V_{CC}$		–1	–	+1	µA
I_{OZ}	Output leakage current	GND $\leq V_O \leq V_{CC}$, output disabled		–1	–	+1	µA
I_{CC}	V_{CC} operating supply current	f = f_{max} = $1/t_{RC}$	V_{CC} = V_{CCmax}, I_{OUT} = 0 mA, CMOS levels	–	11	16	mA
		f = 1 MHz		–	1.3	2.0	mA
I_{SB1}[7]	Automatic CE power-down current — CMOS inputs	$\overline{CE_1} \geq V_{CC}$ – 0.2 V, CE_2 < 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V, $V_{IN} \leq$ 0.2 V, f = f_{max} (address and data only), f = 0 (OE and $\overline{WE}$), V_{CC} = 3.60 V		–	1	4	µA
I_{SB2}[7]	Automatic CE power-down current — CMOS inputs	$\overline{CE_1} \geq V_{CC}$ – 0.2 V, CE_2 < 0.2 V, $V_{IN} \geq V_{CC}$ – 0.2 V or V_{IN} < 0.2 V, f = 0, V_{CC} = 3.60 V		–	1	4	µA

Notes

3. $V_{IL(min)}$ = –2.0 V for pulse durations less than 20 ns.
4. $V_{IH(max)}$ = V_{CC} + 0.75 V for pulse durations less than 20 ns.
5. Full device AC operation assumes a 100 µs ramp time from 0 to $V_{CC(min)}$ and 200 µs wait time after V_{CC} stabilization.
6. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = $V_{CC(typ)}$, T_A = 25 °C.
7. Chip enables ($\overline{CE_1}$ and CE_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.

Capacitance

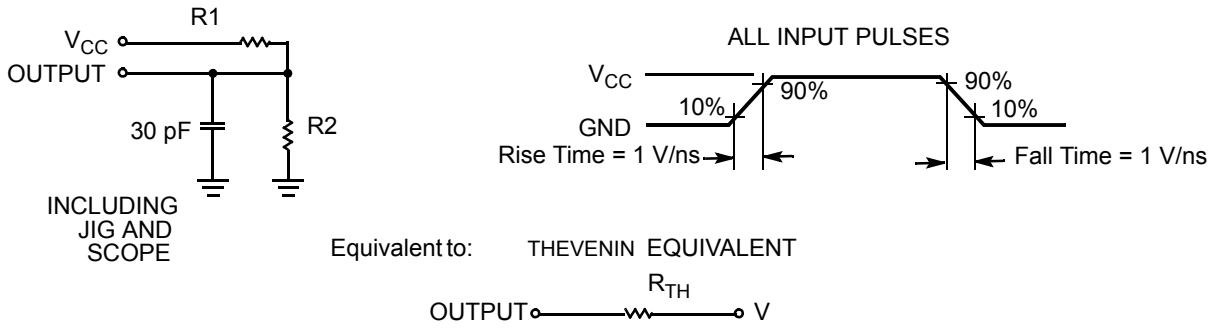
Parameter [8]	Description	Test Conditions	Max	Unit
C_{IN}	Input capacitance	T_A = 25 °C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	10	pF
C_{OUT}	Output capacitance		10	pF

Thermal Resistance

Parameter [8]	Description	Test Conditions	32-pin TSOP I	32-pin SOIC	32-pin STSOP	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Still air, soldered on a 3 × 4.5 inch, two-layer printed circuit board	33.01	48.67	32.56	°C/W
Θ_{JC}	Thermal resistance (junction to case)		3.42	25.86	3.59	°C/W

AC Test Loads and Waveforms

Figure 4. AC Test Loads and Waveforms



Parameters	2.50 V	3.0 V	Unit
R1	16667	1103	Ω
R2	15385	1554	Ω
R_{TH}	8000	645	Ω
V_{TH}	1.20	1.75	V

Note
8. Tested initially and after any design or process changes that may affect these parameters.

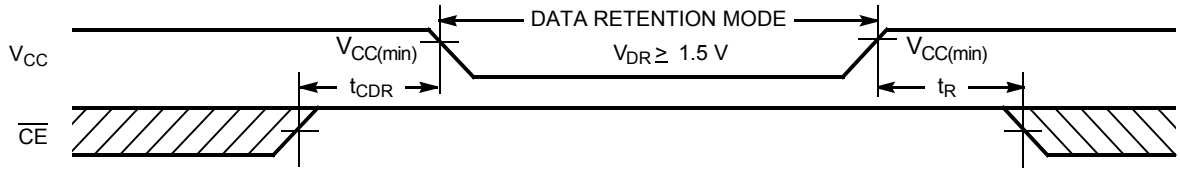
Data Retention Characteristics

Over the Operating Range

Parameter	Description	Conditions		Min	Typ [9]	Max	Unit
V_{DR}	V_{CC} for data retention			1.5	–	–	V
I_{CCDR}[10]	Data retention current	V_{CC} = 1.5 V, $\overline{CE}_1 \geq V_{CC} - 0.2$ V or $CE_2 \leq 0.2$ V, $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V	Industrial	–	–	3	µA
t_{CDR}[11]	Chip deselect to data retention time			0	–	–	ns
t_R[12]	Operation recovery time			45	–	–	ns

Data Retention Waveform

Figure 5. Data Retention Waveform [13]



Notes
9. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC} = V_{CC(typ)}$, T_A = 25 °C.
10. Chip enables ($\overline{CE}_1$ and CE_2) must be at CMOS level to meet the I_{SB1} / I_{SB2} / I_{CCDR} spec. Other inputs can be left floating.
11. Tested initially and after any design or process changes that may affect these parameters.
12. Full device AC operation requires linear V_{CC} ramp from V_{DR} to $V_{CC(min)} \geq$ 100 µs or stable at $V_{CC(min)} \geq$ 100 µs.
13. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.

Switching Characteristics

Over the Operating Range

Parameter [14, 15]	Description	45 ns (Industrial)		Unit
		Min	Max	
Read Cycle				
t_{RC}	Read cycle time	45	–	ns
t_{AA}	Address to data valid	–	45	ns
t_{OHA}	Data hold from address change	10	–	ns
t_{ACE}	$\overline{CE}$ LOW to data valid	–	45	ns
t_{DOE}	$\overline{OE}$ LOW to data valid	–	22	ns
t_{LZOE}	$\overline{OE}$ LOW to low Z [16]	5	–	ns
t_{HZOE}	$\overline{OE}$ HIGH to high Z [16, 17]	–	18	ns
t_{LZCE}	$\overline{CE}$ LOW to low Z [16]	10	–	ns
t_{HZCE}	$\overline{CE}$ HIGH to high Z [16, 17]	–	18	ns
t_{PU}	$\overline{CE}$ LOW to power-up	0	–	ns
t_{PD}	$\overline{CE}$ HIGH to power-down	–	45	ns
Write Cycle [18]				
t_{WC}	Write cycle time	45	–	ns
t_{SCE}	$\overline{CE}$ LOW to write end	35	–	ns
t_{AW}	Address setup to write end	35	–	ns
t_{HA}	Address hold from write end	0	–	ns
t_{SA}	Address setup to write start	0	–	ns
t_{PWE}	$\overline{WE}$ pulse width	35	–	ns
t_{SD}	Data setup to write end	25	–	ns
t_{HD}	Data hold from write end	0	–	ns
t_{HZWE}	$\overline{WE}$ LOW to high Z [16, 17]	–	18	ns
t_{LZWE}	$\overline{WE}$ HIGH to low Z [16]	10	–	ns

Notes

14. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
15. Test Conditions for all parameters other than tri-state parameters assume signal transition time of 3 ns or less (1 V/ns), timing reference levels of $V_{CC(typ)}/2$, input pulse levels of 0 to $V_{CC(typ)}$, and output loading of the specified I_{OL}/I_{OH} as shown in the AC Test Loads and Waveforms on page 5.
16. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
17. t_{HZOE}, t_{HZCE}, and t_{HZWE} transitions are measured when the output enter a high impedance state.
18. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE} = V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.

Switching Waveforms

Figure 6. Read Cycle 1 (Address Transition Controlled) [20, 21]

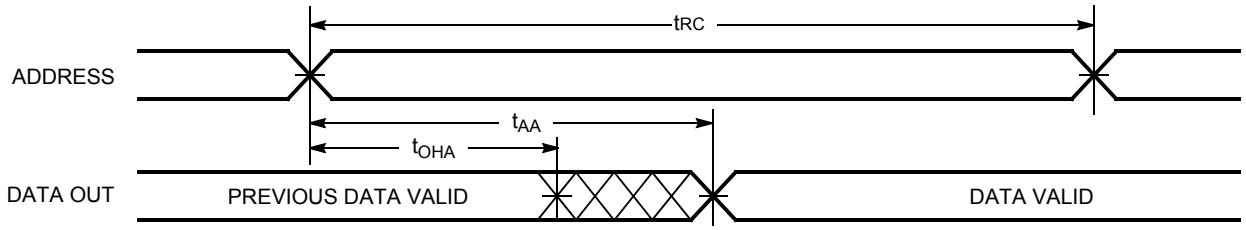
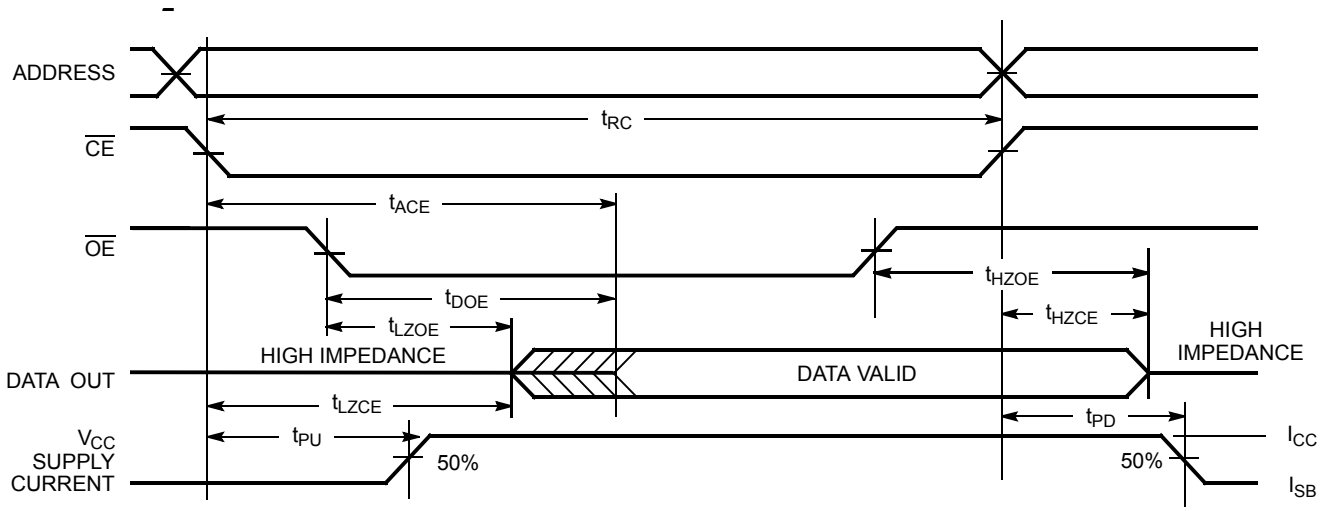


Figure 7. Read Cycle No. 2 ($\overline{OE}$ Controlled) [21, 22, 23]



Notes

19. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
20. The device is continuously selected. $\overline{OE}$, $\overline{CE_1}$ = V_{IL}, CE_2 = V_{IH}.
21. $\overline{WE}$ is HIGH for read cycle.
22. $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
23. Address valid before or similar to $\overline{CE_1}$ transition LOW and CE_2 transition HIGH.

Switching Waveforms (continued)

Figure 8. Write Cycle No. 1 ($\overline{WE}$ Controlled) [24, 25, 26, 27]

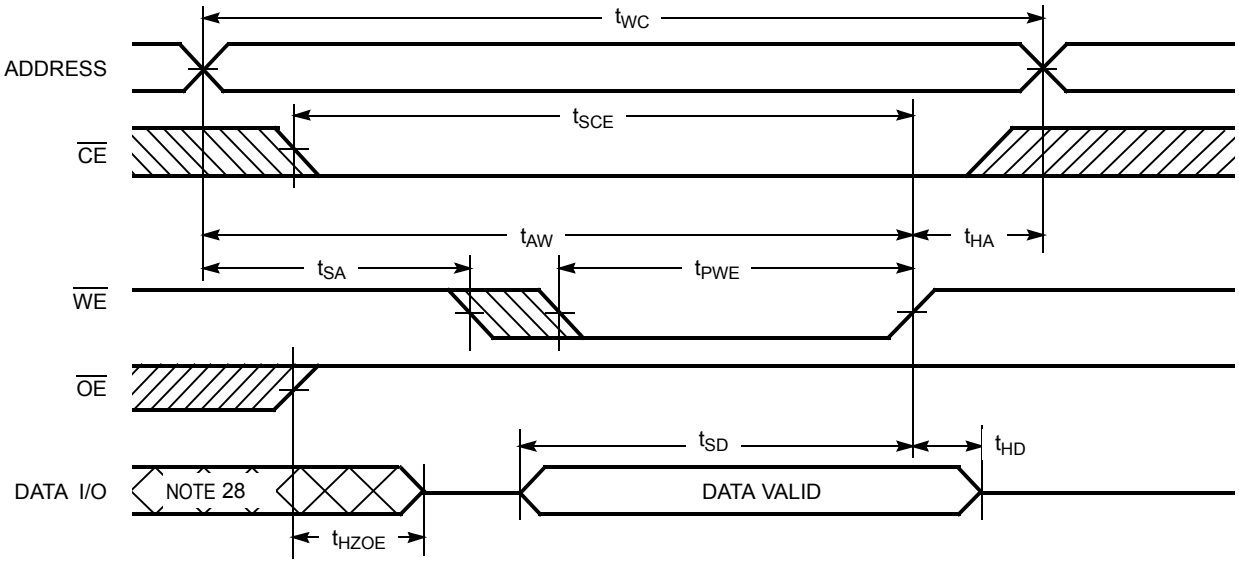
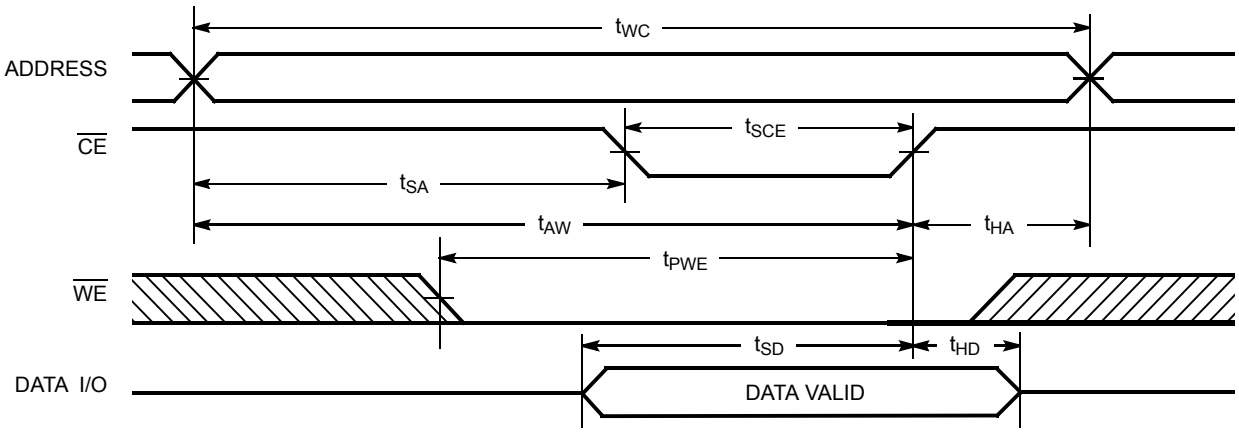


Figure 9. Write Cycle No. 2 ($\overline{CE_1}$ or CE_2 Controlled) [24, 25, 26, 27]

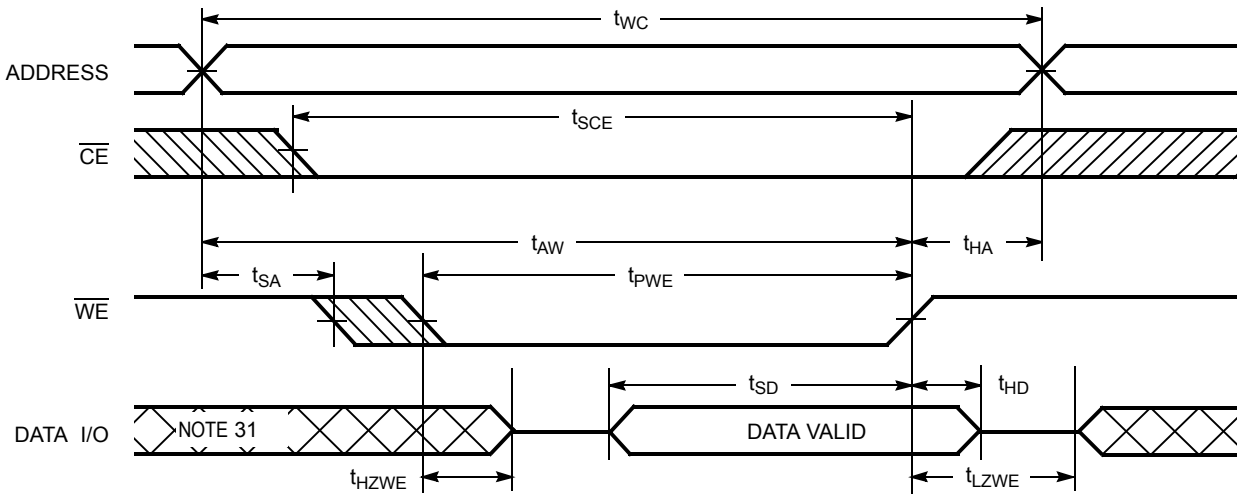


Notes

24. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = V_{IL}. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input setup and hold timing should be referenced to the edge of the signal that terminates the write.
25. $\overline{CE}$ is the logical combination of $\overline{CE_1}$ and CE_2. When $\overline{CE_1}$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE_1}$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
26. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
27. If $\overline{CE_1}$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
28. During this period, the I/Os are in output state. Do not apply input signals.

Switching Waveforms (continued)

Figure 10. Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW) [29, 30]



Notes
29. $\overline{CE}$ is the logical combination of $\overline{CE}_1$ and CE_2. When $\overline{CE}_1$ is LOW and CE_2 is HIGH, $\overline{CE}$ is LOW; when $\overline{CE}_1$ is HIGH or CE_2 is LOW, $\overline{CE}$ is HIGH.
30. If $\overline{CE}_1$ goes HIGH or CE_2 goes LOW simultaneously with $\overline{WE}$ HIGH, the output remains in high impedance state.
31. During this period, the I/Os are in output state. Do not apply input signals.

Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X [32]	X	X	High Z	Deselect/power-down	Standby (I_{SB})
X [32]	L	X	X	High Z	Deselect/power-down	Standby (I_{SB})
L	H	H	L	Data out	Read	Active (I_{CC})
L	H	L	X	Data in	Write	Active (I_{CC})
L	H	H	H	High Z	Selected, outputs disabled	Active (I_{CC})

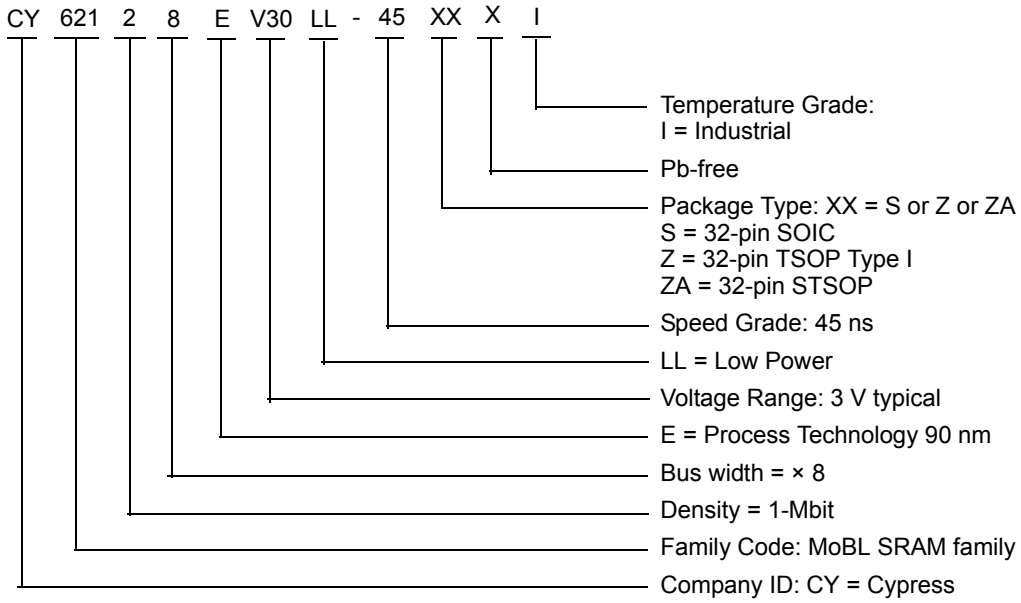
Note
32. The 'X' (Don't care) state for the Chip enables in the truth table refer to the logic state (either HIGH or LOW). Intermediate voltage levels on these pins is not permitted.

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62128EV30LL-45SXI	51-85081	32-pin 450-Mil SOIC (Pb-free)	Industrial
	CY62128EV30LL-45ZXI	51-85056	32-pin TSOP Type I (Pb-free)	
	CY62128EV30LL-45ZAXI	51-85094	32-pin STSOP (Pb-free)	

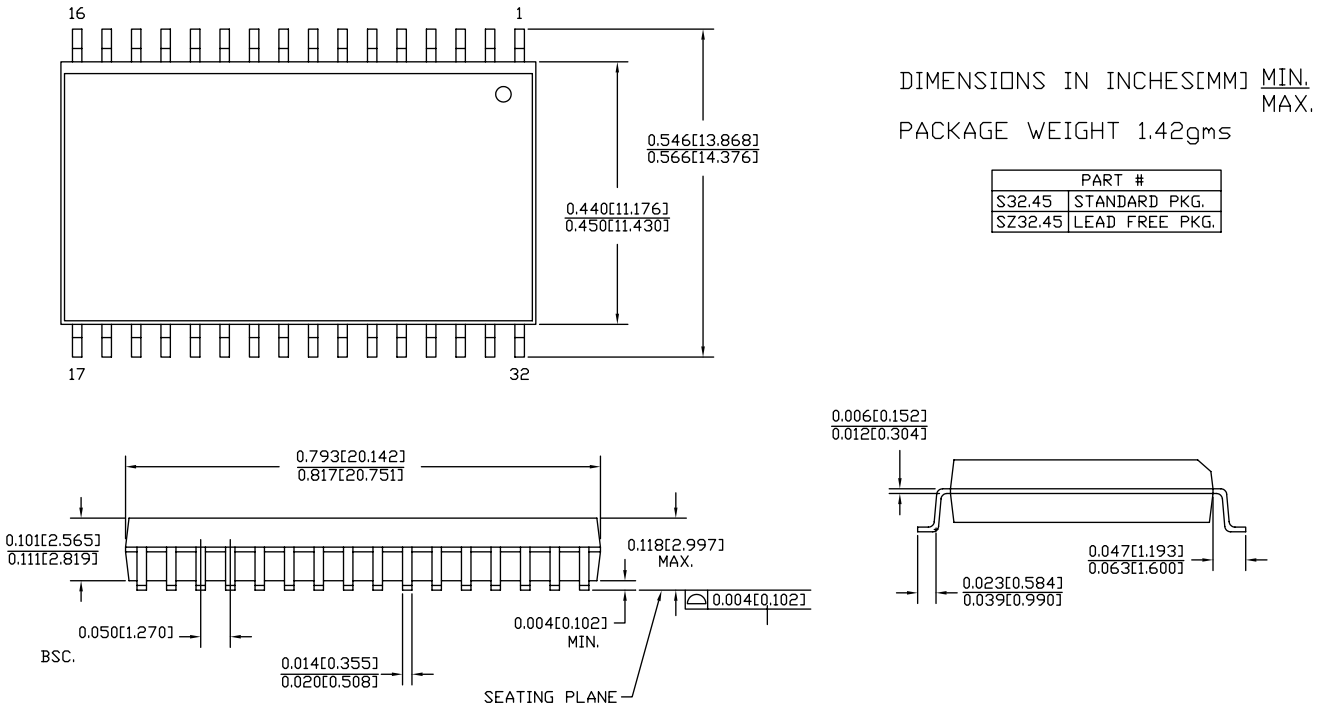
Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions



Package Diagrams

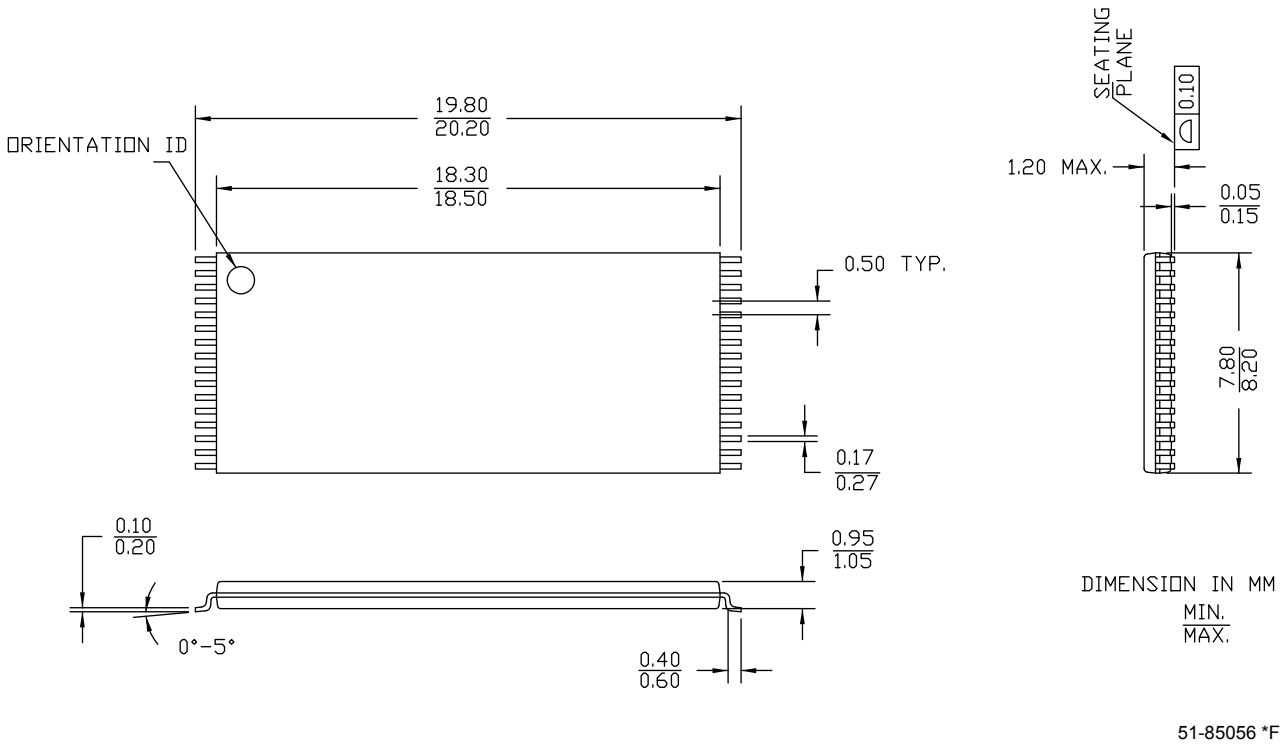
Figure 11. 32-pin Molded SOIC (450 Mil) S32.45/SZ32.45, 51-85081



51-85081 *C

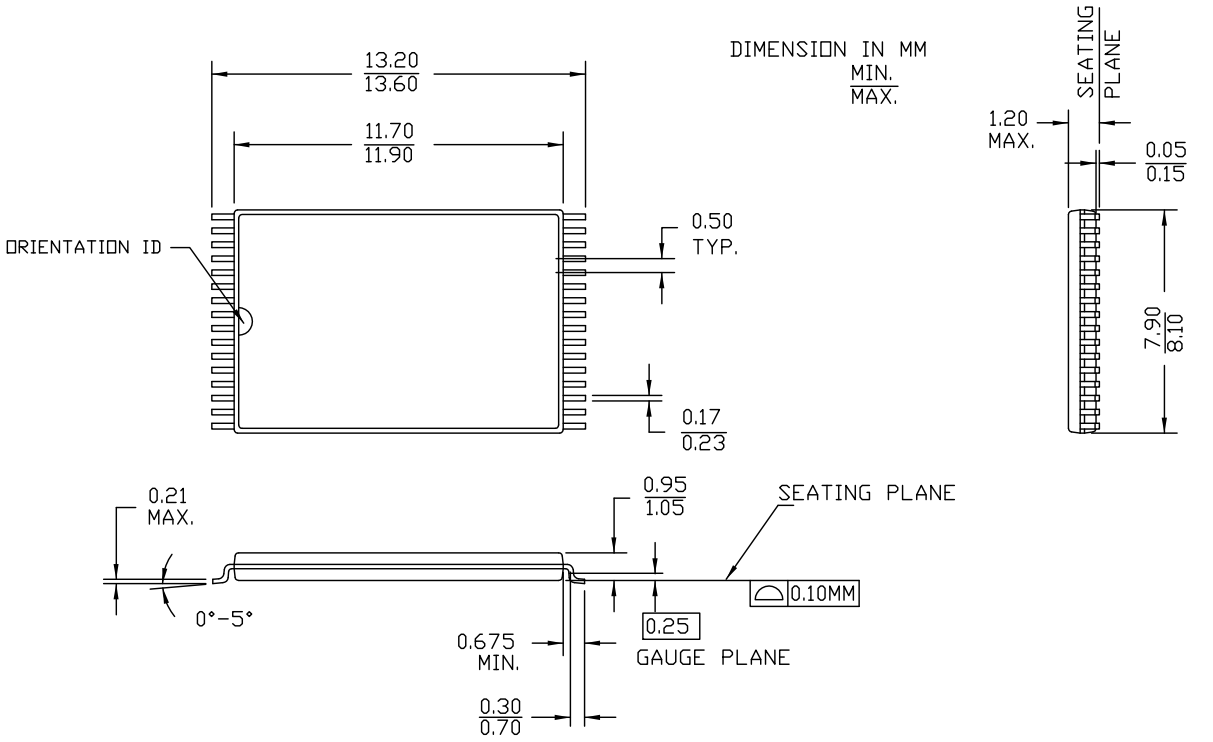
Package Diagrams (continued)

Figure 12. 32-pin TSOP I (8 × 20 × 1.0 mm) Z32, 51-85056



Package Diagrams (continued)

Figure 13. 32-pin Small TSOP (8 × 13.4 × 1.2 mm) ZA32, 51-85094



51-85094 *F

Acronyms

Acronym	Description
$\overline{BHE}$	byte high enable
$\overline{BLE}$	byte low enable
$\overline{CE}$	chip enable
CMOS	complementary metal oxide semiconductor
I/O	input/output
$\overline{OE}$	output enable
SOIC	small outline integrated circuit
SRAM	static random access memory
STSOP	shrunk thin small outline package
TSOP	thin small outline package
$\overline{WE}$	write enable

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
MHz	Mega Hertz
µA	micro Amperes
µs	micro seconds
mA	milli Amperes
mm	milli meter
ns	nano seconds
Ω	ohms
%	percent
pF	pico Farad
V	Volts
W	Watts

Document History Page

Document Title: CY62128EV30 MoBL®, 1-Mbit (128 K × 8) Static RAM Document Number: 38-05579				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	285473	See ECN	PCI	New Data Sheet
*A	461631	See ECN	NXR	Converted from Preliminary to Final Removed 35 ns Speed Bin Removed “L” version of CY62128EV30 Removed Reverse TSOP I package from Product offering. Changed $I_{CC\ (Typ)}$ from 8 mA to 11 mA and $I_{CC\ (Max)}$ from 12 mA to 16 mA for f = f_{max} Changed $I_{CC\ (max)}$ from 1.5 mA to 2.0 mA for f = 1 MHz Changed $I_{SB2\ (max)}$ from 1 μA to 4 μA Changed $I_{SB2\ (Typ)}$ from 0.5 μA to 1 μA Changed $I_{CCDR\ (max)}$ from 1 μA to 3 μA Changed the AC Test load Capacitance value from 50 pF to 30 pF Changed t_{LZOE} from 3 to 5 ns Changed t_{LZCE} from 6 to 10 ns Changed t_{HZCE} from 22 to 18 ns Changed t_{PWE} from 30 to 35 ns Changed t_{SD} from 22 to 25 ns Changed t_{LZWE} from 6 to 10 ns Updated the Ordering Information table.
*B	464721	See ECN	NXR	Updated the Block Diagram on page # 1
*C	1024520	See ECN	VKN	Added final Automotive-A and Automotive-E information Added footnote #9 related to I_{SB2} and I_{CCDR} Updated Ordering Information table
*D	2257446	See ECN	NXR	Changed the Maximum rating of Ambient Temperature with Power Applied from 55°C to +125°C to –55°C to +125°C.
*E	2702841	05/06/2009	VKN/PYRS	Added -45SXA part in the Ordering Information table Corrected “t_{PD}” spec description in the “Switching Characteristics” table.
*F	2781490	10/08/2009	VKN	Included “CY62128EV30LL-45ZAXA” part in the Ordering Information table
*G	2934428	06/03/10	VKN	Added footnote #21 related to chip enable Updated package diagrams Updated template
*H	3026548	09/12/2010	AJU	Updated Pin Configuration Added Ordering Code Definitions Added Acronyms and Units of Measure Minor edits
*I	3115909	01/06/2011	RAME	Separated Automotive and Industrial parts from this datasheet. Removed Automotive info completely
*J	3292906	06/25/2011	AJU	Removed the Note “For best practice recommendations, refer to the Cypress application note “System Design Guidelines” at http://www.cypress.com.” and its reference in Functional Description. Updated Package Diagrams. Updated in new template.

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