

Features

- Easy to use capacitive button controller
 - Hardware configurable 16-button solution
 - Easy to decode Truth table based Output mode
 - Mechanical key scan interface for backward compatibility
- Robust noise performance
 - High sensitivity, low noise capacitive sensing algorithm
 - Strong immunity to radio frequency (RF) and alternating current (AC) noise
 - Low radiated noise emission
- SmartSense™ auto tuning
 - No manual tuning required (reduces time to market)
 - All CapSense® parameters are automatically set in runtime
 - Ensures signal to noise ratio (SNR) of 5:1 or greater
 - Supports wide range of input capacitance (5 pF to 40 pF)
- Advanced features
 - Multiple sensitivity options
 - Multi touch sense (MTS) for simultaneous key detections
 - Supports three different output modes
 - Variable scan rate for power optimization
 - Configurable auto reset for stuck sensors during runtime.
 - Simplified production line testing
 - Failure mode effect analysis (FMEA) of CapSense buttons
- Wide operating range
 - 1.71 V to 5.5 V ideal for unregulated battery applications ^[1]
- Low power consumption
 - Supply current in run mode as low as 20 µA ^[2] per button
 - Deep sleep current: 100 nA
- Industrial temperature range: -40 °C to + 85 °C
- 48-pin quad flat no leads (QFN) package (6 × 6 × 0.6 mm)

Overview

CY8CMBR2016 is designed for simple and robust implementation of user interface solution using Cypress' CapSense technology with SmartSense auto-tuning. The device supports up to 16 capacitive touch buttons that can be organized in any format, such as a matrix array. With its backward compatible key scan interface, it can enable users to achieve quick-to-market (retrofit) designs in large keypad applications such as fire alarm control panels, security systems, and door locks. Any application that requires up to 16 CapSense buttons can utilize CY8CMBR2016.

Notes

1. Supply variation should not be more than 5% for proper CapSense operation.
2. Power consumption calculated with 250 ms scan time, 2% touch time and Cp of each sensor < 19 pF.

Contents

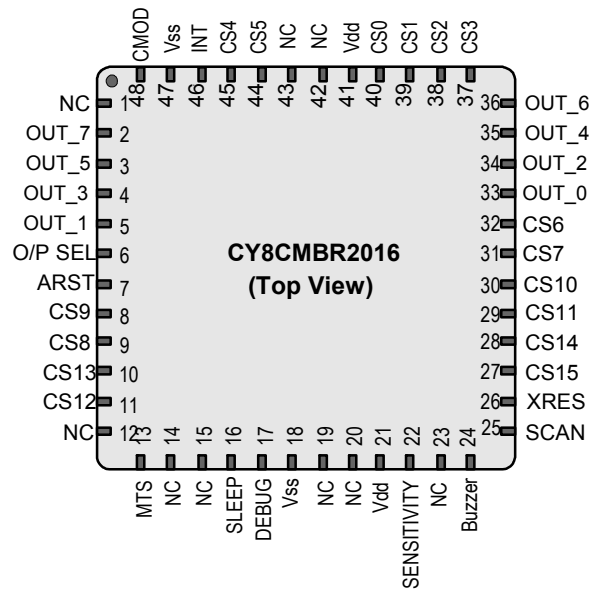
Pin Out	3	Sample Layout	16
Typical Circuits	4	Top	16
Device Features	6	Bottom	17
CapSense Buttons	6	Electrical Specifications	18
SmartSense Auto Tuning	6	Absolute Maximum Ratings	18
Multi Touch Sense	6	Operating Temperature	18
Key Scan Interface	6	DC Electrical Characteristics	18
Truth Table Output	7	AC Electrical Specifications	19
Encoded 4-bit Output	8	CapSense Specification	20
Buzzer Output	8	Package information	21
Interrupt Line	8	Thermal Impedances by Package	21
Hardware Configurability	8	Solder Reflow Peak Temperature	21
Auto Reset	8	Ordering information	22
Output Select	8	Ordering Code Definitions	22
Scan/Sleep Rate	9	Acronyms	23
Sensitivity	9	Document Conventions	23
Noise Filtering	9	Units of Measure	23
Failure Mode Analysis	9	Document History Page	24
Debug Data Out	10	Sales, Solutions, and Legal Information	25
Device Operating Modes	10	Worldwide Sales and Design Support	25
Deep Sleep Mode	10	Products	25
		PSoC Solutions	25

Pin Out

Table 1. Pin Out for the Device

Pin	Pin Name	Type	Description
1	NC	–	No connection
2	OUT_7	DO	READ_3/TT_ROW_3/EO_3/ FMEA_CLK line - Output port interface pin 7
3	OUT_5	DO	READ_1/TT_ROW_1/EO_1 - Output port interface pin 5
4	OUT_3	DIO	SCAN_3/TT_COL_3 - Output port interface pin 3
5	OUT_1	DIO	SCAN_1/TT_COL_1 - Output port interface pin 1
6	O/P SEL	AI	Selects the output interface
7	ARST	AI	Controls sensor auto reset time
8	CS9	AI	CapSense button 9
9	CS8	AI	CapSense button 8
10	CS13	AI	CapSense button 13
11	CS12	AI	CapSense button 12
12	NC	–	Reserved pin
13	MTS	DI	Selects multi touch sense feature
14	NC	–	No connection
15	NC	–	No connection
16	SLEEP	DI	Deep sleep pin of the device
17	DEBUG	DO	Debug out from the device (UART TX8 line)
18	Vss	–	GND
19	NC	–	No connection
20	NC	–	No connection
21	Vdd	–	Power supply
22	SENSITIVITY	AI	Selects the sensitivity of the CS system
23	NC	–	Reserved for shield out
24	BUZZER	DO	Connects to DC Buzzer for audio feedback
25	SCAN	AI	Controls the sleep rate of the system
26	XRES	DI	System reset pin
27	CS15	AI	CapSense button 15
28	CS14	AI	CapSense button 14
29	CS11	AI	CapSense button 11
30	CS10	AI	CapSense button 10
31	CS7	AI	CapSense button 7
32	CS6	AI	CapSense button 6
33	OUT_0	DIO	SCAN_0/TT_COL_0 - Output port interface pin 0

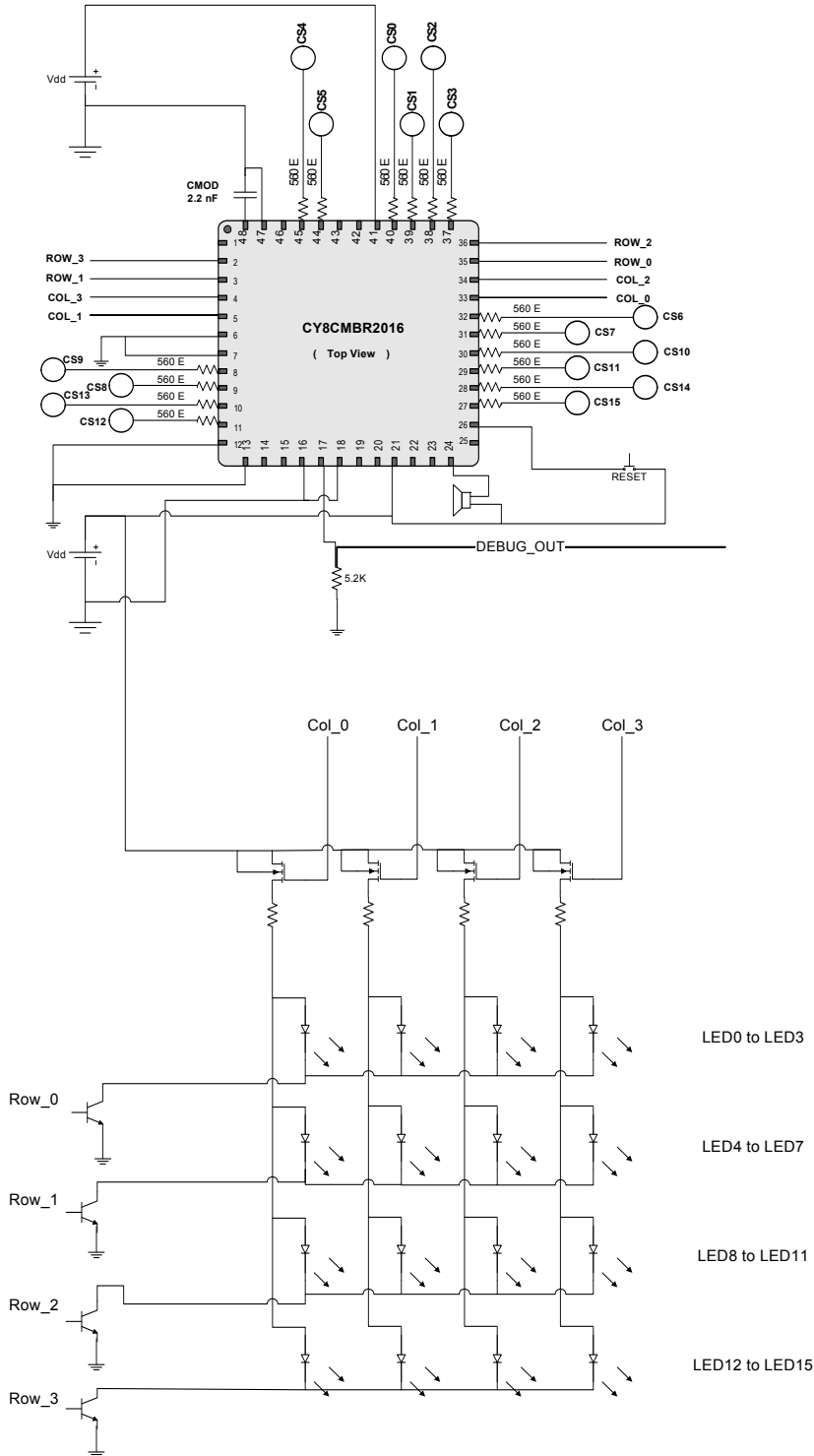
Figure 1. Device Pin Out



34	OUT_2	DIO	SCAN_2/TT_COL_2 - Output port interface pin 2
35	OUT_4	DO	READ_0/TT_ROW_0/EO_0 - Output port interface pin 4
36	OUT_6	DO	READ_0/TT_ROW_0/EO_2/FMEA_D ATA - Output port interface pin 6
37	CS3	AI	CapSense button 3
38	CS2	AI	CapSense button 2
39	CS1	AI	CapSense button 1
40	CS0	AI	CapSense button 0
41	Vdd	–	Power supply
42	NC	–	No connection
43	NC	–	No connection
44	CS5	AI	CapSense button 5
45	CS4	AI	CapSense button 4
46	INT	DO	Interrupt line to Host
47	Vss	–	GND
48	CMOD	AI	CMOD capacitor, 2.2 nF

Typical Circuits

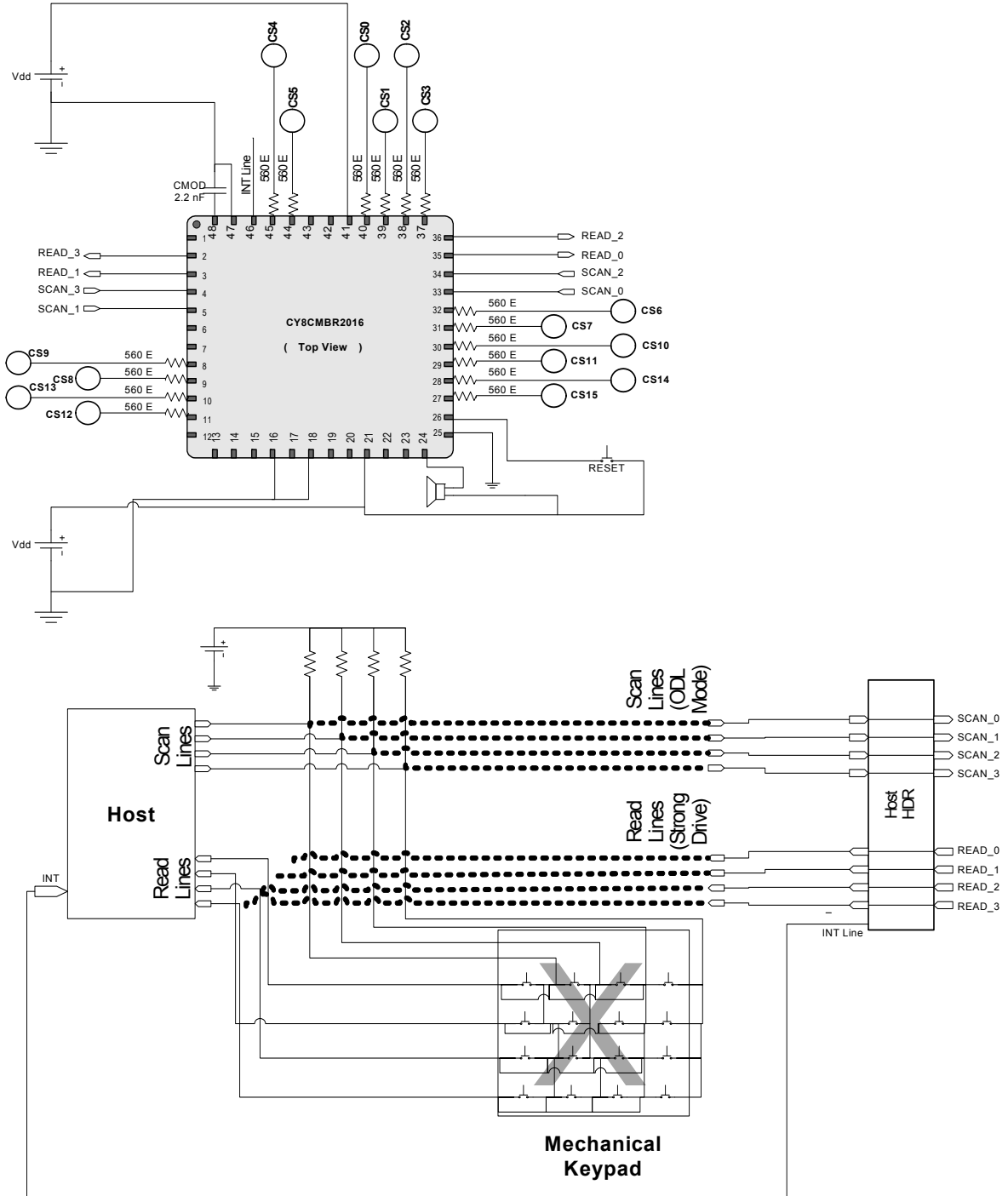
Figure 2. Sample Schematics - Example 1



Example 1 Configuration: Truth Table Mode + ARST 5 s + SCAN Continuous + Sensitivity 0.2 pF + MTS disabled

Figure 3. Sample Schematics - Example 2

Mechanical Matrix Retrofit - Key Scan mode + No auto reset + MTS enabled + Scan continuous + 0.2 pF sensitivity



Example Two Configuration: Mechanical Matrix Retrofit - Key Scan mode + No auto reset + MTS enabled + Scan continuous + 0.2 pF sensitivity.

Device Features

Table 2. Device Feature List

Feature	Description/Use
16 CapSense buttons	Mechanical button/keypad replacement
Multi touch sense	Report simultaneous button touches
Key scan interface	Mechanical matrix replacement
Truth table output	Easy to decode Truth table based Output mode
4 bit - Encoded output	Fewer number of Pins to output the button status
Sensor auto reset	Prevents sensors from getting stuck during run time
Scan/sleep rate	Configures the device based on power needs
Configurable sensitivity	Selects the sensitivity for the system – minimum change in capacitance to be detected
Deep sleep	Reduce power consumption by hibernating the device
Failure mode analysis	Supports for production testing and debugging

CapSense Buttons

- Device supports up to 16 CapSense Buttons.
- Ground the CSx Pin to disable CapSense input.
- 2.2 nF capacitor should be connected on CMOD pin for proper CapSense operation.

SmartSense Auto Tuning

- Device supports auto tuning of CapSense sensor parameters.
- No manual tuning is required; all parameters are set by device automatically.
- The Parasitic Capacitance (C_p) of each button should be less than 40 pF for proper CapSense operation.

Multi Touch Sense

- Enables simultaneous button touches.
- To enable the feature, connect the MTS pin to GND. Else connect to V_{DD} or leave floating to disable the feature.
- When disabled, helps discriminate between closely spaced sensors
- When disabled the first sensor pressed will be reported ON till it is released, even if other sensors are pressed (Figure 4)

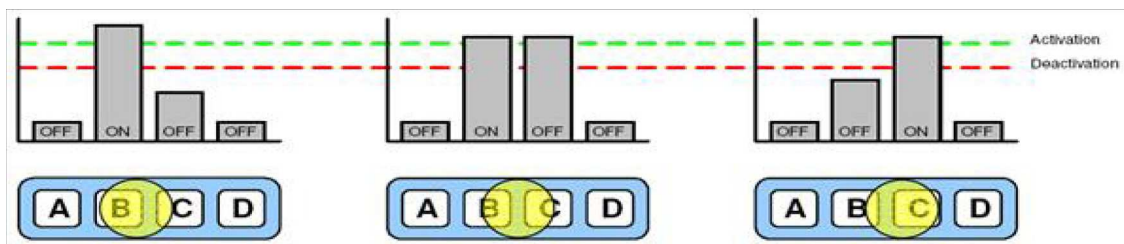
Key Scan Interface

- Mimics legacy mechanical keypads - 4 Scan lines (I/P) and 4 read lines (O/P)
- Reads the Scan lines and updates the Read lines based on the button status
- 'Plug' n 'Play' replacement for mechanical keypads.
- When sensors are disabled or found to be invalid, Table 3 helps identifying the scan and read lines.
- When the scan lines are not used, they should be connected to V_{DD}
- SCAN_0 to SCAN_3 in the pin out form the SCAN lines and READ_0 to READ_3 form the READ lines
- Refer Figure 6 for scan line waveform details.

Table 3. Key Scan interface Selection based on # of sensors

No. of Sensors	SCAN × READ Lines	Scan Lines
(>12)	4 × 4	SCAN 0 to 3
(<=12) && (>8)	3 × 4	SCAN 0 to 2
(<=8) && (>4)	2 × 4	SCAN 0 to 1
(<=4)	1 × 4	SCAN 0

Figure 4. Sensor Status ^[3]



Note

3. When finger moves from one button to other (MTS disabled).

Figure 5. Key Scan interface Retrofit

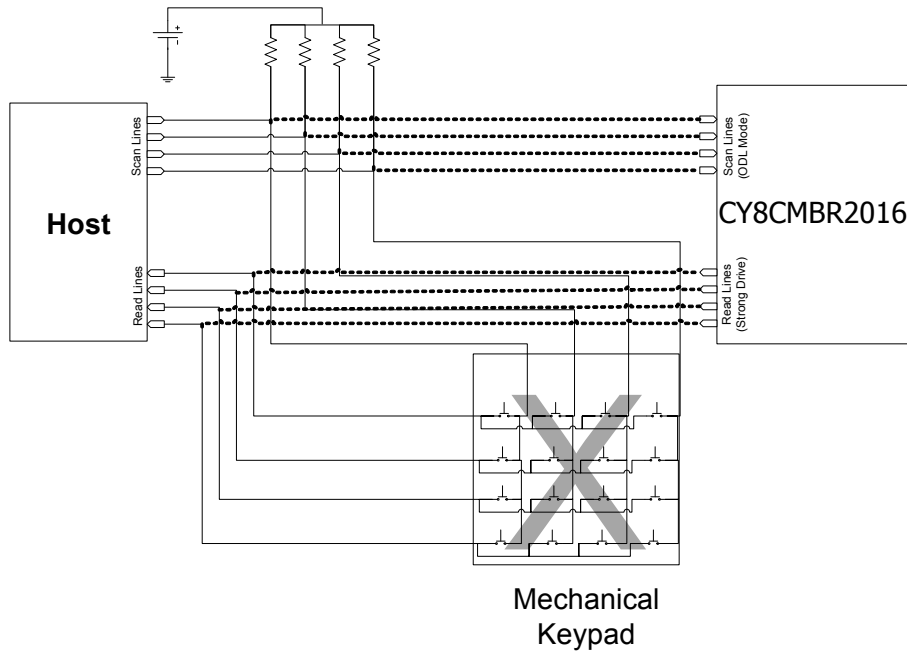
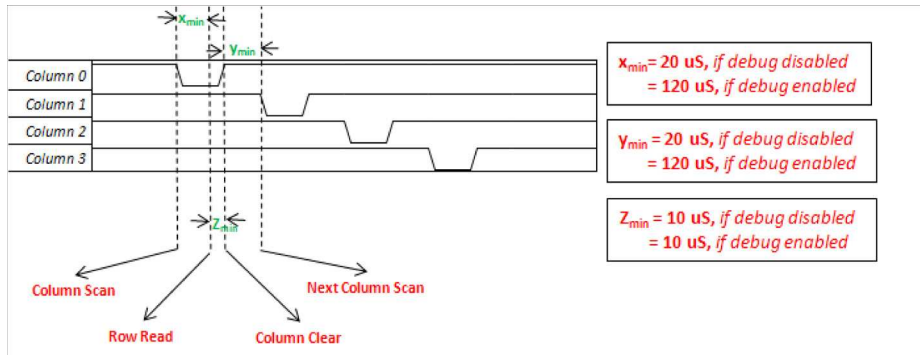


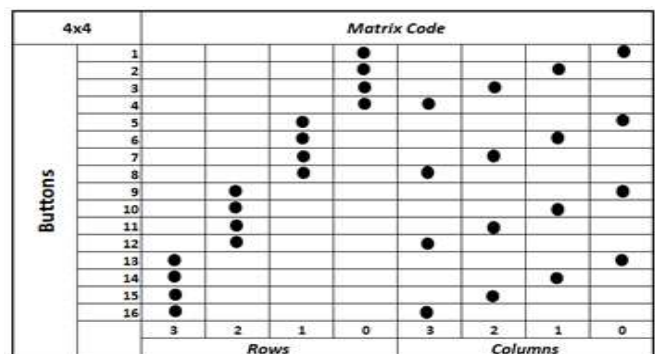
Figure 6. SCAN Line Waveform Details



Truth Table Output

- Another output interface providing matrix style output.
- All pins are output pins - divided into ROW/COLUMN.
- Only one button can be reported at a time - cannot be used in conjunction with MTS enabled.
- Button status is reported in an encoded ROW/COLUMN fashion as shown in Figure 7.
- Each button has its own ROW-COLUMN code.
- Easy to integrate into a system requiring a simple interface with single key press requirement.
- TT_ROW_0 to TT_ROW_3 in the pin out form the ROW lines and TT_COL_0 to TT_COL_3 form the COLUMN lines.

Figure 7. Truth Table Output



Encoded 4-bit Output

- Only 4 pins to report a button press out of 16 buttons.
- Each button has its own code.
- Only one button can be reported at a time using this interface.
- Table 4 define the decode table.

Table 4. Encoded Output

Keypress Detected By CapSense	EO[3:0]	Interrupt Time
Key #1	0000	1
Key #2	0001	1
Key #3	0010	1
Key #4	0011	1
...	...	1
Key #16	1111	1
No keys pressed	XXXX	0

Buzzer Output

- A dedicated pin for buzzer output is provided in the device.
- Buzzer output can be used to drive an p-type transistor driving a buzzer or directly a DC buzzer up to 10 mA sink current.

Interrupt Line

- An interrupt line to the host controller.
- The pin go high whenever one or more sensors are found active. And remains high till those sensors are released
- Can be used as a latch input at the host side to read the OUT lines.
- Can also be used as an interrupt line for the host controller to read the OUT lines.

Hardware Configurability

- Advanced features like auto reset, scan rate, output select are configured using an external resistor at predefined pins (refer Figure 1 and Table 1)
- These features are configured once on reset by reading/measuring the resistors connected at the pins.

Auto Reset

- The sensor auto reset time is controlled by the hardware configuration on the ARST pin. Refer Table 5 for details.
- This time dictates the maximum time for which the sensor will be treated as active from the time it was touched.
- After the sensor is released the CSx will be hold for 440 ms ^[4]

Table 5. ARST Pin Configuration

ARST pin	Auto Reset Delay
Pin connected to ground	5 sec
1.5 K(5%) ohms resistor to ground	20 sec
5 K (5%) resistor to ground	40 sec
Pin connected to V _{DD} or left floating	No auto reset

Figure 8. Sensor Auto Reset



Output Select

- One among the three output interfaces defined earlier in the section can be selected by the hardware configuration on the OUT_SEL pin. Refer Table 6 for details.
- Only one of the output can be used at a given time with a defined resistor.

Table 6. Output Select

Output Selection	Interface Selected
Pin connected to ground	Truth table I/F
1.5 K (5%) ohms resistor to ground	Encoded 4-bit output
Connected to V _{DD} or left floating	Keypad scanning interface output

Note

4. Power consumption calculated with 250 ms scan time, 2% touch time and Cp of each sensor < 19 pF.

Scan/Sleep Rate

- The device scan/sleep rate is defined by the hardware configuration on the SCAN pin. Refer [Table 7](#) for details.
- The scan rate or sleep rate dictates the rate at which the device sleeps, wakes up and then does a special scan of the sensors after being idle (no sensor active) for two seconds.
- The power consumed by the device is inversely proportional to the time for which the device sleeps (Refer the design guide tool for power info).

Table 7. Scan Rate Configuration

Scan Rate pin	Scan rate
Pin connected to ground	Low, 250 ms
1.5 K (5%) ohms resistor to ground	Medium, 150 ms
5 K (5%) resistor to ground	High, 40 ms
Pin connected to V _{DD} or left floating	Continuous

Sensitivity

- The sensitivity of the CapSense system is controlled by the hardware configuration on the SENSITIVITY pin. Refer to [Table 8](#) for details
- The sensitivity of the CapSense system dictates the smallest increase in capacitance that can be detected clearly as a signal by the CapSense
- While selecting this parameter, care should be taken and noise should be studied - with extreme sensitivity system can pick up noise and give false triggers.

Table 8. Sensitivity Configuration

Sensitivity pin	Sensitivity
Pin connected to ground	Low (0.4 pF)
1.5 K (5%) ohms resistor to ground	Medium (0.3 pF)
Connected to V _{DD} or left floating	High (0.2 pF)

Noise Filtering

- Device supports inbuilt noise filtering techniques.
- A second order IIR filter is applied to the raw counts before it is processed
- The feature is in built and not given to the user to configure the coefficients of the filter

Failure Mode Analysis

A built-in power on self test (POST) mechanism detects the following at power on reset (POR), which can be useful in production testing.

Sensor Shorted to Ground

If a sensor is disabled/found short to GND, then the corresponding bit field in the sensor mask is set and the same will be sent out serially through OUT_6 pin with the synchronizing clock at OUT_7. The clock is a 2 kHz clock, if no clock is sensed till 300 ms after power ON, then all the sensors are fine. If a clock is sensed, then starting from the first falling edge of the clock each sensor will occupy every clock slot. With the data line reading high during the falling edge, indicates a failure of the sensor in that clock slot. And the clock will stop after indicating the failure of the nth sensor in its clock slot - where 'n' is the highest index among the disabled sensor. For instance, if Sensor 1, 3 and 5 are disabled - then as shown in [Figure 9](#), the FMEA data will be transmitted. The first failure corresponding to Sensor 1 will be marked by a HIGH on OUT_6 in the 0.5 ms to 1 ms slot. Sensor 3 failure will be marked by a HIGH on OUT_6 in the 1.5 ms to 2 ms slot. And Sensor 5 will be marked in the 2.5 to 3 ms slot. After indicating the failure of Sensor 5, since no further sensors have failed - clock signal will be ceased in the subsequent cycles. [Figure 10](#) shows the scenario where 1, 3 and 15 fails.

Figure 9. FMEA of Disabled Sensor - Scenario 1

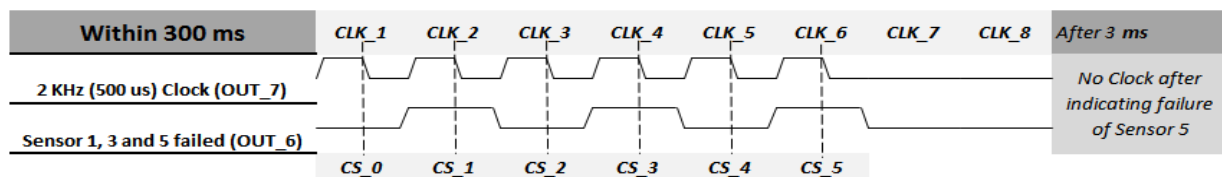


Figure 10. FMEA of Disabled Sensor - Scenario 2

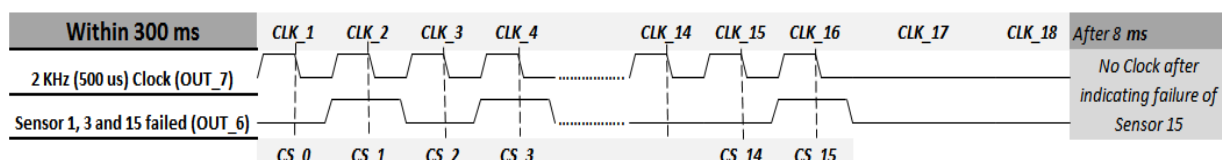
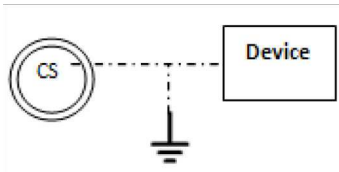


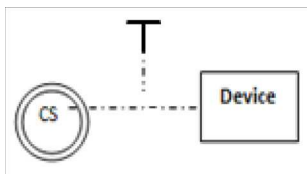
Figure 11. Sensor Shorted to GND



Sensor Shorted to VDD

If any sensor is shorted to VDD that sensor is disabled and the corresponding bit field is set and FMEA signal is sent as defined in Sensor to GND short section.

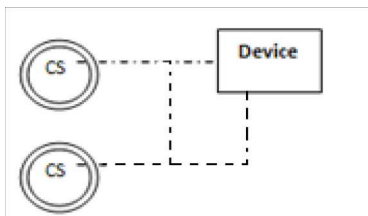
Figure 12. Sensor Shorted to VDD



Sensor to Sensor Short

Any Sensors that are shorted together is disabled and the corresponding bit field is set and FMEA signal is sent as defined in Sensor to GND short section.

Figure 13. Sensor to Sensor Short



Proper Value of CMOD

- Recommended value of CMOD is 2 nF to 2.4 nF.
- If CMOD of < 1 nF or > 4 nF is connected, all sensors are disabled and the status output will be logic high on all slots.

Sensor CP > 40 pF

If the parasitic capacitance (CP) of any sensor exceeds 40 pF that sensor is disabled and the corresponding bit field is set and FMEA signal is sent as defined in Sensor to GND short section.

Debug Data Out

- To enable this feature, the DEBUG pin is pulled down with a 5.6 K resistor.
- The Cypress multi chart tool ([AN2397](#)) can be used to view the debug data for each button
- Serial data is sent out at ~115,200 baud rate
- Firmware revision, CapSense status, baseline, raw counts, difference counts and parasitic capacitances of all sensors are sent out
- The Debug data sent out is defined in [Table 9](#) and [Table 10](#).

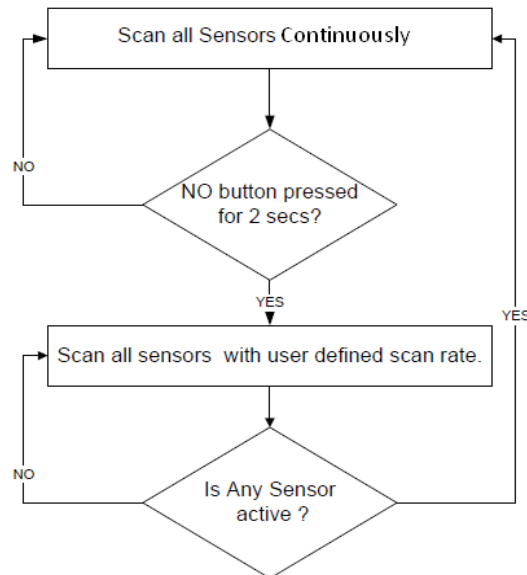
Device Operating Modes

There are two device operating modes:

- Low power sleep mode
- Deep sleep mode

Low Power Sleep Mode

The following flow chart describes the low power sleep mode operation.



For details on Low power sleep look at the scan rate section.

Deep Sleep Mode

- To enable the deep sleep mode, the hardware configuration pin Sleep should be connected to the master device.
- Sleep pin should be connected to VDD for the device to go into deep sleep.
- In deep sleep mode, all blocks are turned off and the device power consumption is 0.1 μ A.
- There is no CapSense scanning in deep sleep mode.
- Sleep pin should be pulled low for the device to wake up from deep sleep.
- When device comes out of deep sleep mode, the CapSense system is reinitialized. Typical time for re-initialization is 8 ms.Any button press within this time is not reported.
- After the device comes out of deep sleep, the device operates in low power sleep mode.
- If the Sleep pin is pulled high at power on, then the device does not go to deep sleep immediately. The device goes to deep sleep after initializing all internal blocks and scanning all sensors once.
- If the Sleep pin is pulled high at power on, then the scan rate is calculated when the device is taken out of Deep Sleep by the master.

Table 9. Data Format in Multi Chart

SI. No.	Raw Count Array		Baseline Array		Difference Count array	
	MSB	LSB	MSB	LSB	MSB	LSB
0	CS0_RC		CS0_BL		CS0_DIFF	
1	CS1_RC		CS1_BL		CS1_DIFF	
2	CS2_RC		CS2_BL		CS2_DIFF	
3	CS3_RC		CS3_BL		CS3_DIFF	
4	CS4_RC		CS4_BL		CS4_DIFF	
5	CS5_RC		CS5_BL		CS5_DIFF	
6	CS6_RC		CS6_BL		CS6_DIFF	
7	CS7_RC		CS7_BL		CS7_DIFF	
8	CS8_RC		CS8_BL		CS8_DIFF	
9	CS9_RC		CS9_BL		CS9_DIFF	
10	CS10_RC		CS10_BL		CS10_DIFF	
11	CS11_RC		CS11_BL		CS11_DIFF	
12	CS12_RC		CS12_BL		CS12_DIFF	
13	CS13_RC		CS13_BL		CS13_DIFF	
14	CS14_RC		CS14_BL		CS14_DIFF	
15	CS15_RC		CS15_BL		CS15_DIFF	
16	0x00	F/W Rev	CS_Status		0x00	CS10_CP
17	0x00	CS0_CP	0x00	CS5_CP	0x00	CS11_CP
18	0x00	CS1_CP	0x00	CS6_CP	0x00	CS12_CP
19	0x00	CS2_CP	0x00	CS7_CP	0x00	CS13_CP
20	0x00	CS3_CP	0x00	CS8_CP	0x00	CS14_CP
21	0x00	CS4_CP	0x00	CS9_CP	0x00	CS15_CP

Table 10. Serial Data Out

BYTE	DATA	Notes
0	0x0D	Dummy variables for multi chart tool
1	0x0A	
2	CS0_RC	CS0 Raw counts, unsigned 16-bit integer
3		
4	CS1_RC	CS1 Raw counts, unsigned 16-bit integer
5		
6	CS2_RC	CS2 Raw counts, unsigned 16-bit integer
7		
-----	-----	-----
32	CS15_RC	CS15 Raw counts, unsigned 16-bit integer
33		
34	0x00	-

Table 10. Serial Data Out (continued)

BYTE	DATA	Notes
35	FW_REV	Firmware revision
36	0x00	–
37	CS0_CP	Parasitic capacitance of CS0
38	0x00	–
39	CS1_CP	Parasitic capacitance of CS1
40	0x00	–
41	CS2_CP	Parasitic capacitance of CS2
42	0x00	–
43	CS3_CP	Parasitic capacitance of CS3
44	0x00	–
45	CS4_CP	Parasitic capacitance of CS4
46	CS0_BL	CS0 Baseline, unsigned 16-bit integer
47		
48	CS1_BL	CS1 Baseline, unsigned 16-bit integer
49		
50	CS2_BL	CS2 Baseline, unsigned 16-bit integer
51		
	-----	-----
76	CS15_BL	CS15 Baseline, unsigned 16-bit integer
77		
78	CS_Status	CapSense Status, unsigned 16 bit integer
79		
80	0x00	–
81	CS5_CP	Parasitic capacitance of CS5
82	0x00	–
83	CS6_CP	Parasitic capacitance of CS6
84	0x00	–
85	CS7_CP	Parasitic capacitance of CS7
86	0x00	–
87	CS8_CP	Parasitic capacitance of CS8
88	0x00	–
89	CS9_CP	Parasitic capacitance of CS9
90	CS0_DIFF	CS0 difference counts, unsigned 16-bit integer
91	CS1_DIFF	CS1 difference counts, unsigned 16-bit integer
92		
93	CS2_DIFF	CS2 difference counts, unsigned 16-bit integer
94		
	-----	-----
121	CS15_DIFF	CS15 difference counts, unsigned 16-bit integer
122		
123	0x00	–

Table 10. Serial Data Out (continued)

BYTE	DATA	Notes
124	CS10_CP	Parasitic capacitance of CS10
125	0x00	–
126	CS11_CP	Parasitic capacitance of CS11
127	0x00	–
128	CS12_CP	Parasitic capacitance of CS12
129	0x00	–
130	CS13_CP	Parasitic capacitance of CS13
131	0x00	–
132	CS14_CP	Parasitic capacitance of CS14
133	0x00	–
134	CS15_CP	Parasitic capacitance of CS15
135	0x00	Dummy variable for multi chart tool
136	0xFF	
137	0xFF	

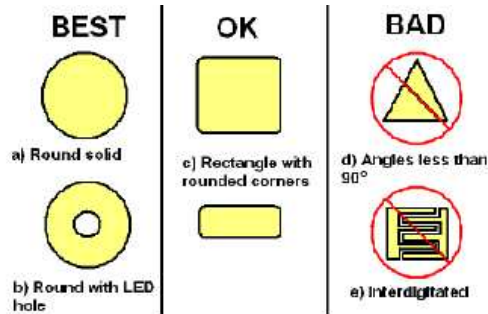
Table 11. Layout Guidelines

Sl. No.	Category	Min	Max	Recommendations/Remarks
1.	Button shape	–	–	Solid round pattern, Round with LED hole, rectangle with round corners
2.	Button size	5 mm	15 mm	Given in layout estimator sheet
3.	Button-Button spacing	equal to button ground clearance		8 mm
4.	Button ground clearance	0.5 mm	2 mm	Given in layout estimator sheet
5.	Ground flood - Top layer	–	–	Hatched ground 7 mil trace and 45 mil grid (15% filling)
6.	Ground flood - bottom layer	–	–	Hatched ground 7 mil trace and 70 mil grid (10% filling)
7.	Trace length from sensor to device pin	–	450	Given in layout estimator sheet
8.	Trace width	0.17 mm	0.20 mm	0.17 mm (7 mil)
9.	Trace routing	–	–	Traces should be routed on the non sensor side. If any non CapSense trace crosses CapSense trace, ensure that intersection is orthogonal.
10.	Via position for the sensors	–	–	Via should be placed near the edge of the button/slider to reduce trace length thereby increasing sensitivity.
11.	Via hole size for sensor traces	–	–	10 mil
12.	No. of via on sensor trace	1	2	1
13.	CapSense series resistor placement	–	10 mm	Place CapSense series resistors close to the device for noise suppression. CapSense resistors have highest priority compared to other resistors, so place them first.

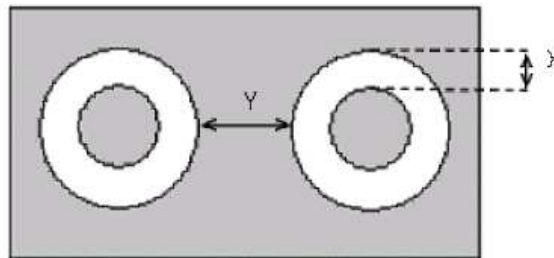
Table 11. Layout Guidelines (continued)

Sl. No.	Category	Min	Max	Recommendations/Remarks
14.	Distance between any CapSense trace to ground flood	0.243 mm	0.486 mm	0.486 mm
15.	Device placement	–	–	Mount the device on the layer opposite to sensor. The CapSense trace length between the device and sensors should be minimum (see trace length above)
16.	Placement of components in two layer PCB	–	–	Top layer-Sensors and bottom layer-device, other components and traces.
17.	Placement of components in four layer PCB	–	–	Top layer-Sensors, second layer – CapSense traces & Vdd and avoid the Vdd traces below the sensors, third layer-hatched ground, Bottom layer- device other components and non CapSense traces
18.	Overlay thickness	0 mm	5 mm	Use layout estimator sheet to decide on overlay, given maximum limit is for plastic overlay.
19.	Overlay material	–	–	Should to be non-conductive material. Glass, ABS Plastic, Formica, wood etc. No air gap should be there between PCB and overlay. Use adhesive to stick the PCB and overlay.
20.	Overlay adhesives	–	–	Adhesive should be non conductive and dielectrically homogenous. 467 MP and 468 MP adhesives made by 3 M are recommended.
21.	Board thickness	–	–	Standard board thickness for CapSense FR4 based designs is 1.6 mm.

CapSense Button Shapes



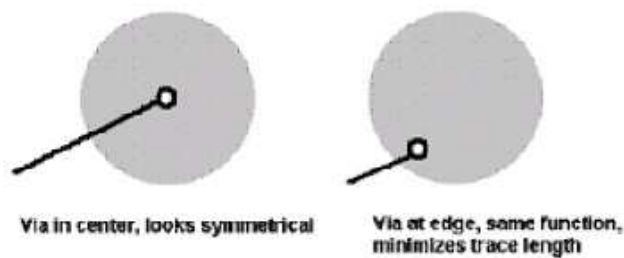
Button Layout Design



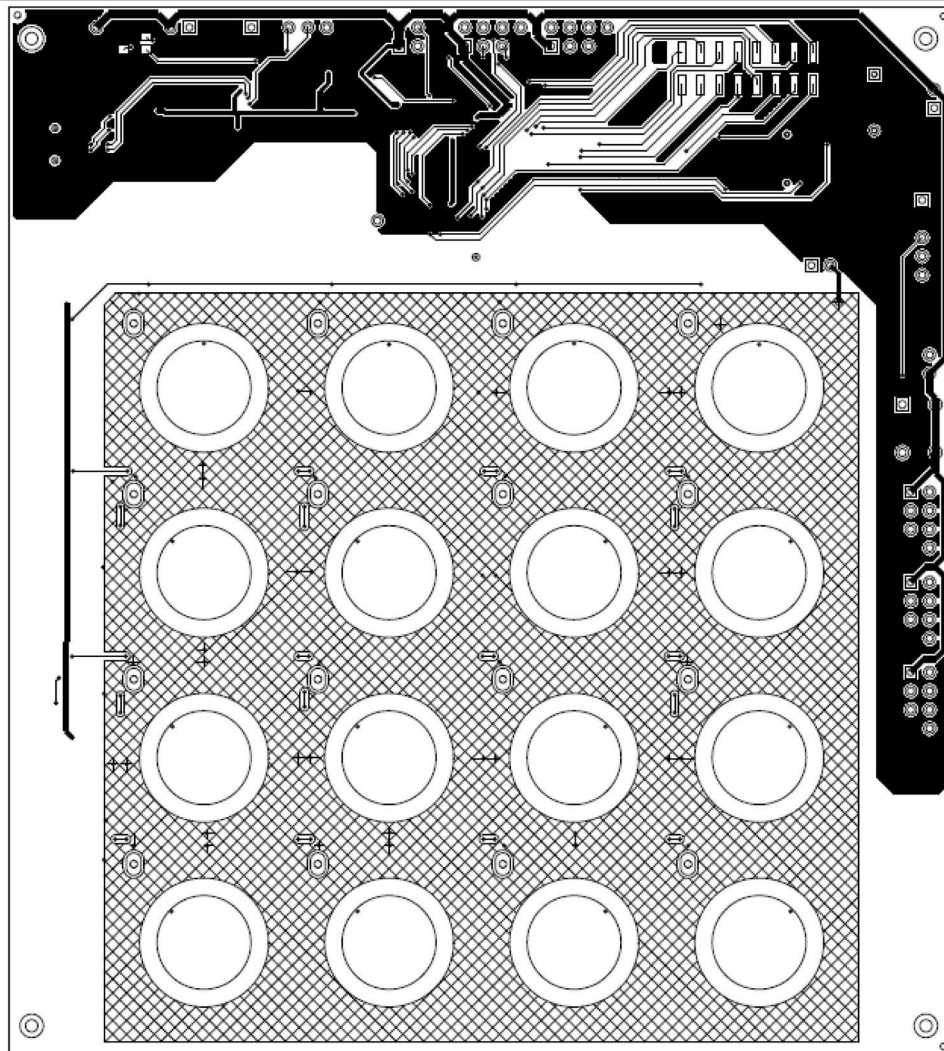
X: Button to ground clearance (Refer to [Layout Guidelines and Best Practices \(AN2292\)](#) on page 16)

Y: Button to button clearance (Refer to [Layout Guidelines and Best Practices \(AN2292\)](#) on page 16)

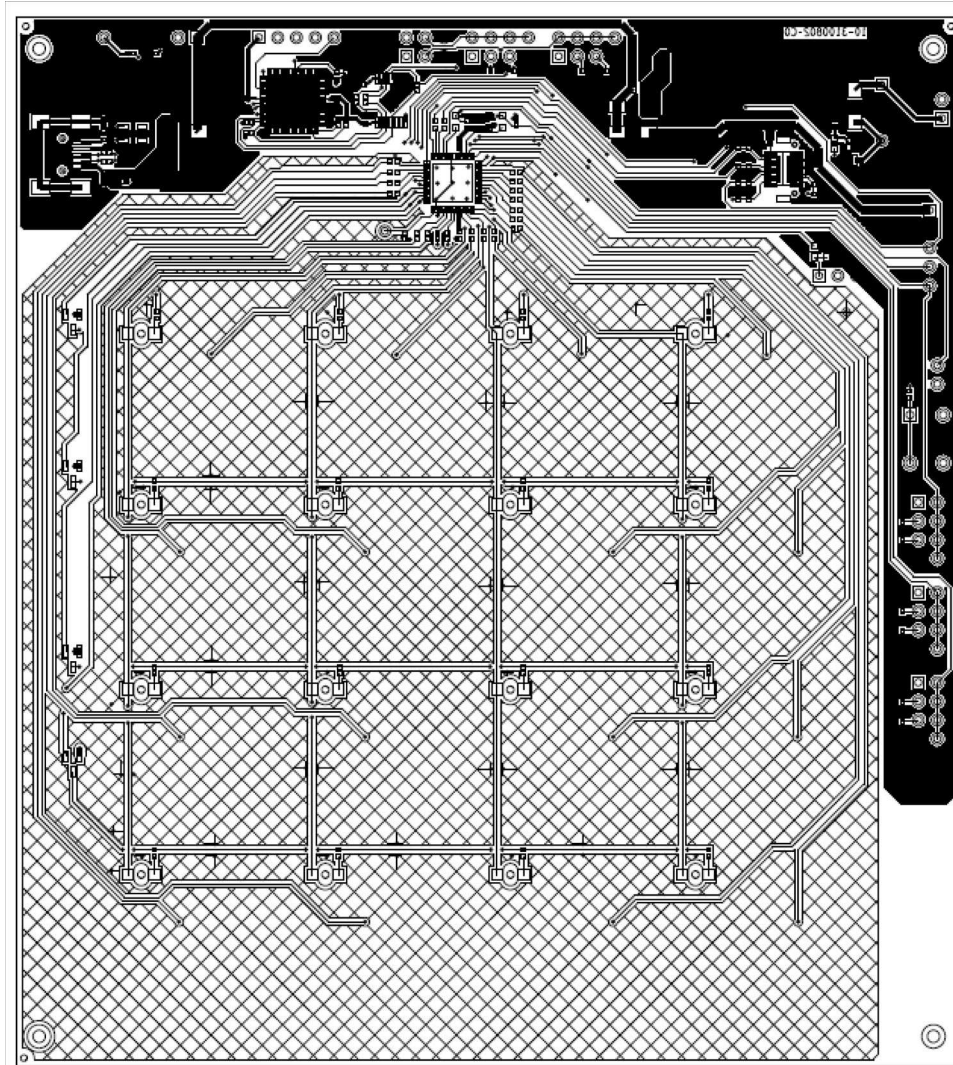
Recommended via Hole Placement



Sample Layout
Top



Bottom



Electrical Specifications

Absolute Maximum Ratings

Parameter	Description	Min	Typ	Max	Unit	Notes
TSTG	Storage temperature	-55	25	+125	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 85 °C degrade reliability.
VDD	Supply voltage relative to VSS	-0.5	-	+6.0	V	-
VIO	DC voltage on CapSense inputs and digital output pins	V _{SS} - 0.5	-	V _{DD} + 0.5	V	-
IMIG	Maximum current into any GPO output pin	-25	-	+50	mA	-
ESD	Electro static discharge voltage	2000	-	-	V	Human body model ESD
LU	Latch up current	-	-	200	mA	In accordance with JESD78 standard

Operating Temperature

Parameter	Description	Min	Typ	Max	Unit	Notes
TA	Ambient temperature	-40	-	+85	°C	-
TJ	Operational die temperature	-40	-	+100	°C	-

DC Electrical Characteristics

DC Chip Level Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
VDD ^[5, 6, 7]	Supply voltage	1.71	-	5.5	V	-
IDD	Supply current	-	3.3	4.0	mA	Conditions are V _{DD} = 3.0 V, TA = 25 °C
IDA	Active current	-	3.3	4.0	mA	Conditions are V _{DD} = 3.0 V, TA = 25 °C, continuous sensor scan
IDS	Deep sleep current	-	100	500	nA	Conditions are V _{DD} = 3.0 V, TA = 25 °C
I _{AV1}	Average current	-	0.25	-	mA	Conditions are V _{DD} = 3.0 V, TA = 25 °C and 16 buttons used, with 0% touch time, Cp of all sensors < 19 pF and scan rate = 250 ms
I _{AV2}	Average current	-	2.13	-	mA	Conditions are V _{DD} = 3.0 V, TA = 25 °C and 16 buttons used, with 50% touch time, Cp of all sensors < 19 pF and scan rate = 250 ms, Key Scan mode enabled
I _{AV3}	Average current	-	0.42	-	mA	Conditions are V _{DD} = 3.0 V, TA = 25 °C and 16 buttons used, with 0% touch time, Cp of all sensors > 19 pF and < 40 pF and scan rate = 250 ms
I _{AV4}	Average current	-	2.2	-	mA	Conditions are V _{DD} = 3.0 V, TA = 25 °C and 16 buttons used, with 50% touch time, Cp of all sensors > 19 pF and < 40 pF and scan rate = 250 ms, Key Scan mode enabled

Notes

- When VDD remains in the range from 1.75 V to 1.9 V for more than 50 μs, the slew rate when moving from the 1.75 V to 1.9 V range to greater than 2 V must be slower than 1 V/500 μs. This helps to avoid triggering POR. The only other restriction on slew rates for any other voltage range or transition is the SRPOWER_UP parameter.
- If you power down the device, make sure that VDD falls below 100 mV before powering backup.
- For proper CapSense block functionality, if the drop in VDD exceeds 5% of the base VDD, the rate at which VDD drops should not exceed 200 mV/s. Base VDD can be between 1.8 V and 5.5 V

DC General Purpose I/O Specifications

These tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 3.0 V to 5.5 V and $-40\text{ }^{\circ}\text{C} = T_A = 85\text{ }^{\circ}\text{C}$, 2.4 V to 3.0 V and $-40\text{ }^{\circ}\text{C} = T_A = 85\text{ }^{\circ}\text{C}$, or 1.71 V to 2.4 V and $-40\text{ }^{\circ}\text{C} = T_A = 85\text{ }^{\circ}\text{C}$, respectively. Typical parameters apply to 5 V and 3.3 V at 25 $^{\circ}\text{C}$ and are for design guidance only.

3.0 V to 5 V DC General Purpose I/O Specification

Parameter	Description	Min	Typ	Max	Unit	Notes
VOH1	High output voltage on all output pins	$V_{DD} - 0.2$	–	–	V	$I_{OH} < 10\text{ }\mu\text{A}$, Maximum of 40 μA source in all I/Os
VOH2	High output voltage on OUT pins	$V_{DD} - 0.9$	–	–	V	$I_{OH} = 1\text{ mA}$, Maximum of 2 mA source in all I/Os
VOH3	High output voltage on INT and BUZZ pins	$V_{DD} - 0.9$	–	–	V	$I_{OH} = 5\text{ mA}$, Maximum of 10 mA source in all I/Os
VOL	Low output voltage	–	–	0.75	V	$I_{OL} = 25\text{ mA/pin}$, $V_{DD} > 3.3\text{ V}$, Maximum of 60 mA source in all I/Os

2.4 V to 3.0 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
VOH1	High output voltage on all outputs	$V_{DD} - 0.2$	–	–	V	$I_{OH} < 10\text{ }\mu\text{A}$, Maximum of 40 μA Source in all I/Os
VOH2	High output voltage on OUT pins	$V_{DD} - 0.4$	–	–	V	$I_{OH} = 0.2\text{ mA}$, Maximum of 0.4 mA source in all I/Os
VOH3	High output voltage on INT and BUZZ	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 2\text{ mA}$, Maximum of 4 mA source in all I/Os
VOL	Low output voltage	–	–	0.72	V	$I_{OL} = 10\text{ mA/pin}$, $V_{DD} > 3.3\text{ V}$, Maximum of 30 mA source in all I/Os

1.71 V to 2.4 V DC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
VOH1	High output voltage on OUT pins	$V_{DD} - 0.2$	–	–	V	$I_{OH} = 10\text{ }\mu\text{A}$, maximum of 20 μA source in all I/Os
VOH2	High output voltage on OUT pins	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 0.5\text{ mA}$, maximum of 1 mA source in all I/Os
VOH3	High output voltage on INT and BUZZ	$V_{DD} - 0.2$	–	–	V	$I_{OH} = 100\text{ }\mu\text{A}$, maximum of 200 μA source in all I/Os
VOH4	High output voltage on INT and BUZZ	$V_{DD} - 0.5$	–	–	V	$I_{OH} = 2\text{ mA}$, maximum of 4 mA source in all I/Os
VOL	Low output voltage	–	–	0.4	V	$I_{OL} = 5\text{ mA/pin}$, $V_{DD} > 3.3\text{ V}$, maximum of 20 mA source in all I/Os

AC Electrical Specifications
AC Chip-Level Specifications

Parameter	Description	Min	Max	Unit	Notes
SRPOWER_UP	Power supply slew rate	–	250	V/ms	V_{DD} slew rate during power-up
TXRST	External reset pulse width at power-up	1	–	ms	After supply voltage is valid
TXRST2	External reset pulse width after power-up	10	–	?s	Applies after part has booted

AC General Purpose I/O Specifications

Parameter	Description	Min	Typ	Max	Unit	Notes
TRise1	Rise time on OUT pins, Cload = 50 pF	15	–	80	ns	VDD = 3.0 to 3.6 V, 10%–90%
TRise2	Rise time on INT and BUZZ pins, Cload = 50 pF	10	–	50	ns	VDD = 3.0 to 3.6 V, 10%–90%
TRise3	Rise time on OUT pins, Cload = 50 pF	15	–	80	ns	VDD = 1.71 to 3.0 V, 10%–90%
TRise2	Rise time on INT and BUZZ pins, Cload = 50 pF	10	–	80	ns	VDD = 1.71 to 3.0 V, 10%–90%
TFall	Fall time, Cload = 50 pF all outputs	10	–	50	ns	VDD = 3.0 to 3.6 V, 90%–10%
TFallL	Fall time, Cload = 50 pF all outputs	10	–	70	ns	VDD = 1.71 to 3.0 V, 90%–10%

CapSense Specification

Parameter	Description	Min	Typ	Max	Unit	Notes
CP	Parasitic capacitance	5.0	–	$(C_P + C_F) < 40$	pF	CP is the total capacitance seen by the pin when no finger is present. CP is sum of C_sensor, C_trace, and Capacitance of the vias and CPIN
CF	Finger capacitance	0.25	–	$(C_P + C_F) < 40$	pF	CF is the capacitance added by the finger touch
CPIN	Capacitive load on pins as input	0.5	1.7	7	pF	Mandatory for CapSense to work
CMOD	External integrating capacitor	2	2.2	2.4	nF	Mandatory for CapSense to work
Rs	Series resistor between pin and the sensor	–	560	616	Ω	Reduces the RF noise

Package information

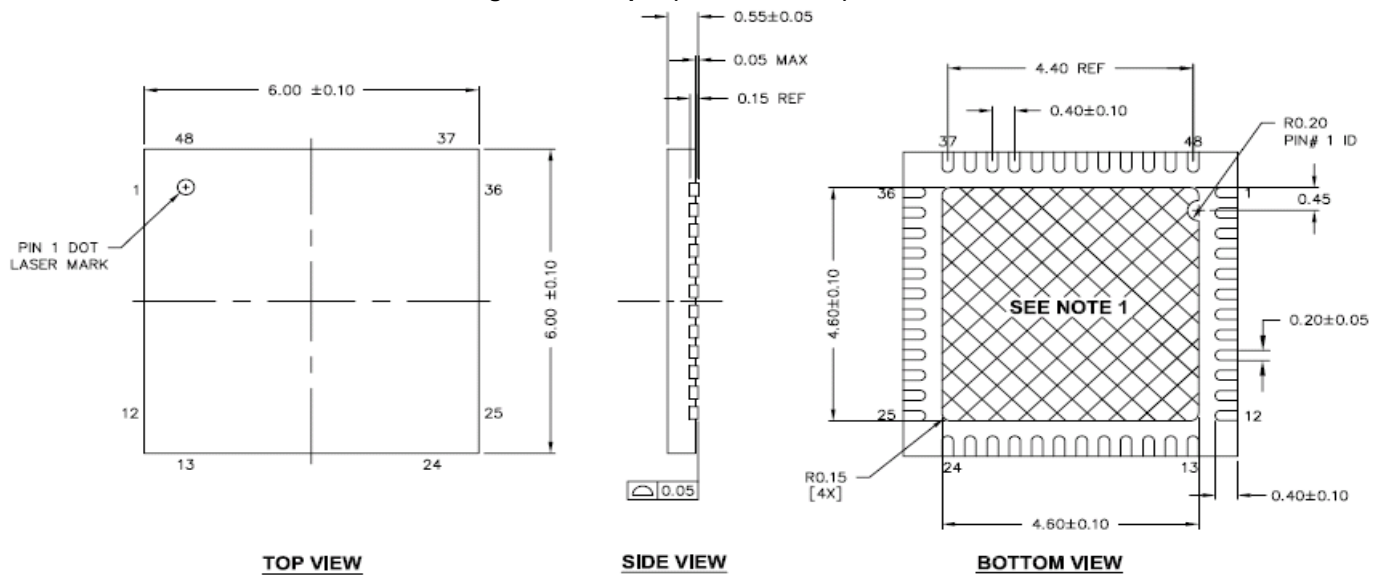
Thermal Impedances by Package

Package	Typical θ_{JA} ^[8]
48-pin QFN ^[9]	19 °C/W


Solder Reflow Peak Temperature

Package	Minimum Peak Temperature ^[10]	Maximum Peak Temperature	Time at Max Temperature
48-pin QFN	240 °C	260 °C	30 s

Figure 14. 48-pin (6 × 6 × 0.6 mm) QFN



NOTES:

1.  HATCH AREA IS SOLDERABLE EXPOSED PAD
2. BASED ON REF JEDEC # MO-220
3. PACKAGE WEIGHT: 0.068 grams
4. ALL DIMENSIONS ARE IN MILLIMETERS

001-57280 *B

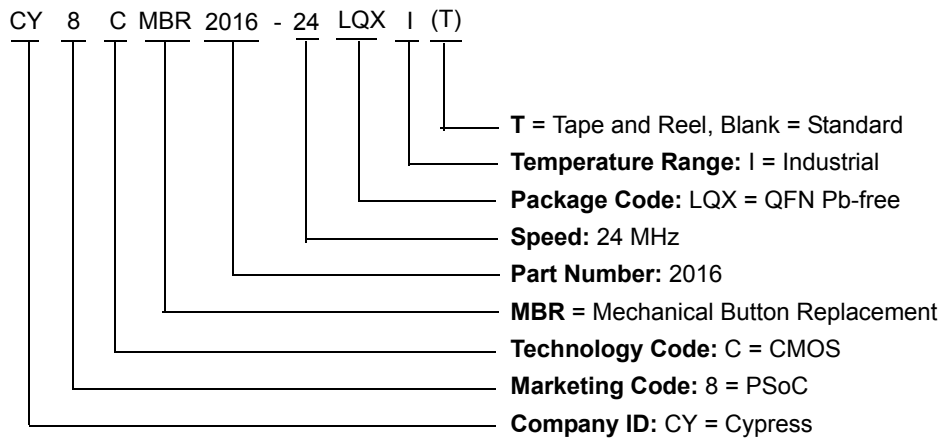
Notes

8. $T_J = T_A + \text{Power} \times \theta_{JA}$
9. To achieve the thermal impedance specified for the QFN package, the center thermal pad must be soldered to the PCB ground plane
10. Higher temperatures may be required based on the solder melting point. Typical temperatures for solder are 220 ± 5 °C with Sn-Pb or 245 ± 5 °C with Sn-Ag-Cu paste. Refer to the solder manufacturer specifications

Ordering information

Ordering Code	Package Type	Operating Temperature	CapSense Block	CapSense Inputs	Other I/Os	XRES pin
CY8CMBR2016-24LQXI	48-pin (6 × 6 × 0.6 mm) QFN	Industrial	Yes	17 ^[11]	17 ^[12]	Yes
CY8CMBR2016-24LQXIT	48-pin (6 × 6 × 0.6 mm) QFN (Tape & Reel)	Industrial	Yes	17 ^[11]	17 ^[12]	Yes

Ordering Code Definitions



Notes

- 11. 16 CapSense input + 1 CMOD pin
- 12. 8 Configurable GPIOs + 1 buzzer output + 1 Sleep line + 1 Interrupt line + 1 Debug line + 5 configuration pins

Acronyms

Acronym	Description
AC	alternating current
C _F	finger capacitance
C _{MOD}	Modulator capacitor
C _P	parasiitic capacitance
EO _x	Encoded Output - Bit 'x'
FMEA	Failure Mode Effect Analysis
MTS	multi touch sense
POR	power on reset
POST	power on self test
QFN	quad flat no leads
RF	radio frequency
READ _x	KeyScan Interface - 'x'th Read line
SCAN _x	KeyScan Interface - 'x'th Scan line
SNR	signal to noise ratio
TT_COL _x	Truth Table Column output - 'x'th Column
TT_ROW _x	Truth Table Row output - 'x'th Row

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
μA	microampere
μF	microfarad
μs	microsecond
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
nF	nanofarad
ns	nanosecond
Ω	ohm
pF	picofarad
ppm	parts per million
s	second
V	volt
W	watt

Document History Page

Document Title: CY8CMBR2016, Capacitive Button Controllers Document Number: 001-67921				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	3202566	MSUR	03/22/2011	New datasheet
*A	3387102	MSUR	10/10/2011	Changed status from Preliminary to Final. Added Char data into the table and some minor edits to the document.
*B	3473096	MSUR	12/22/2011	No technical updates.

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