

Features

2.450 GHz

Standard 3 Wire Interface

Small layout 0.6" × 0.6"



Applications

Digital Radio Equipment

Fixed Wireless Access

Satellite Communications Systems

Base Stations

Personal Communications Systems

Portable Radios

Test Instruments

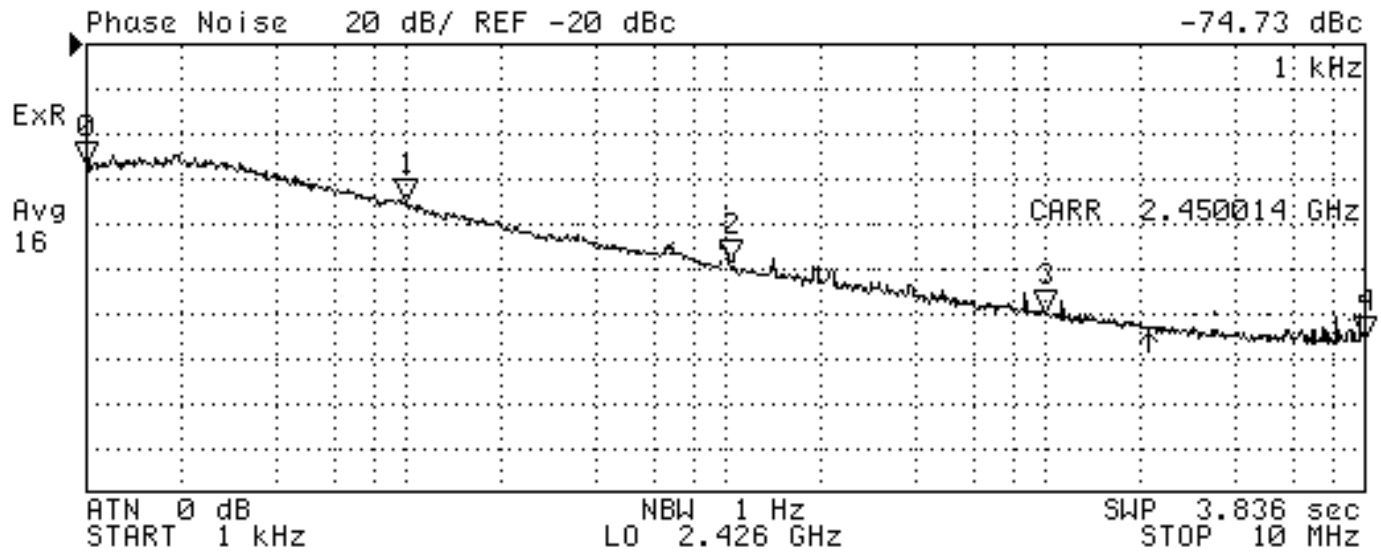
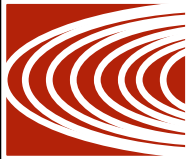
Wireless Infrastructure

The CPLL66 is a complete PLL/Synthesizer needing only an external frequency reference and supply voltages for the internal PLL (phase lock loop) and VCO (voltage controlled oscillator). The Crystek CPLL66 is programmed using a standard three line interface (Data, Clock and Load Enable).

The CPLL66 family has been initially released to cover 1 GHz to 5 GHz in bands. It is housed in a compact 0.6-in. × 0.6-in. × 0.15-in. SMD package which saves board space. Typical phase noise at 4 GHz is -90 dBc/Hz at 10 kHz offset with 0 dBm minimum output power.

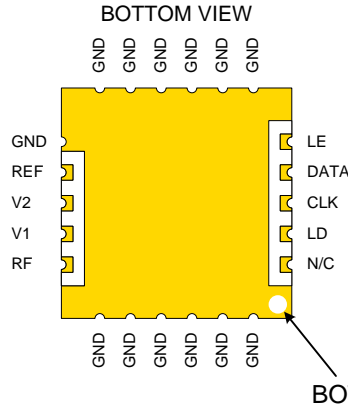
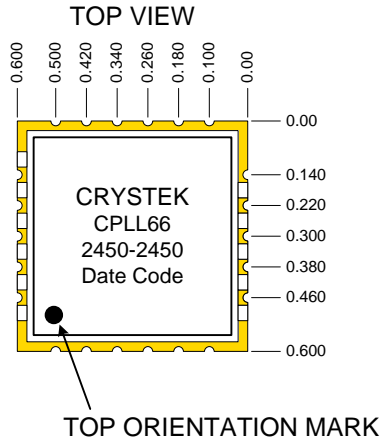
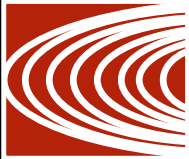


| PERFORMANCE SPECIFICATION | MIN | TYP | MAX | UNITS |
|--|------|-------|------|--------|
| Frequency Range: | | 2.450 | | GHz |
| Step Size: | | 100 | | kHz |
| Settling Time, to within ± 1kHz (Freq. step < 25MHz): | | 1 | | msec |
| Output Power: | 0 | +3.0 | +6.0 | dBm |
| Output Phase Noise: (See Plot Below) | | | | |
| @1kHz offset | | -75 | -70 | dBc/Hz |
| @10kHz offset | | -95 | -90 | dBc/Hz |
| @100kHz offset | | -120 | -115 | dBc/Hz |
| @1MHz offset | | -145 | -140 | dBc/Hz |
| Power Supply: | | | | |
| V1= VCO Supply | 4.75 | 5.0 | 5.25 | Volts |
| V2= PLL Supply | 2.7 | 3.0 | 3.3 | Volts |
| Supply Current: | | | | |
| I1= VCO Input Current | | 50 | | mA |
| I2= PLL Input Current | | 25 | | mA |
| Spurious Suppression | | | | dBc |
| PFDSpur | | -70 | -60 | dBc |
| Reference Feedthru | | -80 | -70 | dBc |
| Harmonic Suppression (2nd Harmonic): | | | | |
| 2 nd | | -15 | -10 | dBc |
| Reference Frequency | | 10 | | MHz |
| Input Reference Level | 0.8 | | V2 | Vp-p |
| RF Output Level | -5 | 0 | +5 | dBm |
| Input Impedance | | 100k | | Ohm |
| RF Output Impedance | | 50 | | Ohm |
| Operating Temperature Range: | -40 | | +85 | °C |
| Logic Inputs (Clock, Data, and LE): | | | | |
| Input "High" Voltage | 1.4 | | | |
| Input "Low" Voltage | | | 0.6 | Volts |
| Locked Detector (LD): | | | | |
| Locked | 1.4 | | | Volts |
| Un-Locked | | | 0.4 | Volts |

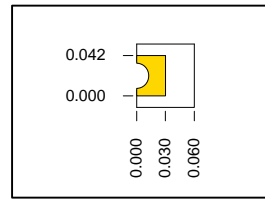
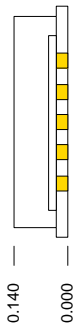


| N | SWP PARAM | VAL |
|---|-----------|-------------|
| 0 | 1 kHz | -74.73 dBc |
| 1 | 10 kHz | -91.553 dBc |
| 2 | 100 kHz | -118.44 dBc |
| 3 | 1 MHz | -140.38 dBc |
| 4 | 10 MHz | -152.17 dBc |



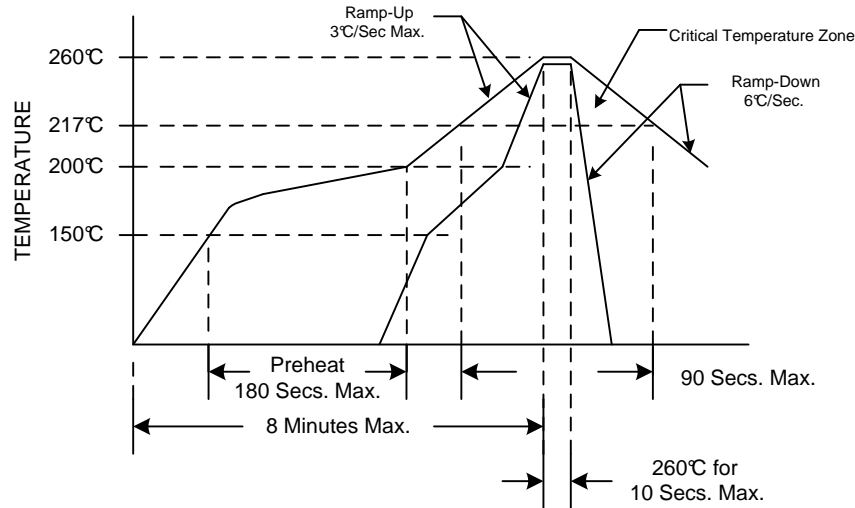


LE= Load Enable, CMOS Input
 DATA= Serial Data Input
 CLK= Clock
 LD= Lock Detect
 REF= Reference Input
 V1= Analog Supply Input (VCO)
 V2= Digital Supply Input (PLL)
 RF= RF Output



Pad Detail

RECOMMENDED REFLOW SOLDERING PROFILE



ENVIRONMENTAL COMPLIANCE

| Parameter | Conditions |
|------------------------|--------------------------|
| Mechanical Shock | MIL-STD-883, Method 2002 |
| Mechanical Vibration | MIL-STD-883, Method 2007 |
| Solderability | MIL-STD-883, Method 1014 |
| Resistance to Solvents | MIL-STD-883, Method 2016 |

Programming Guide for CPLL66-XXXX

Introduction

The CPLL66 uses a simple 3 wire interface to program four internal registers. See Figure 1.

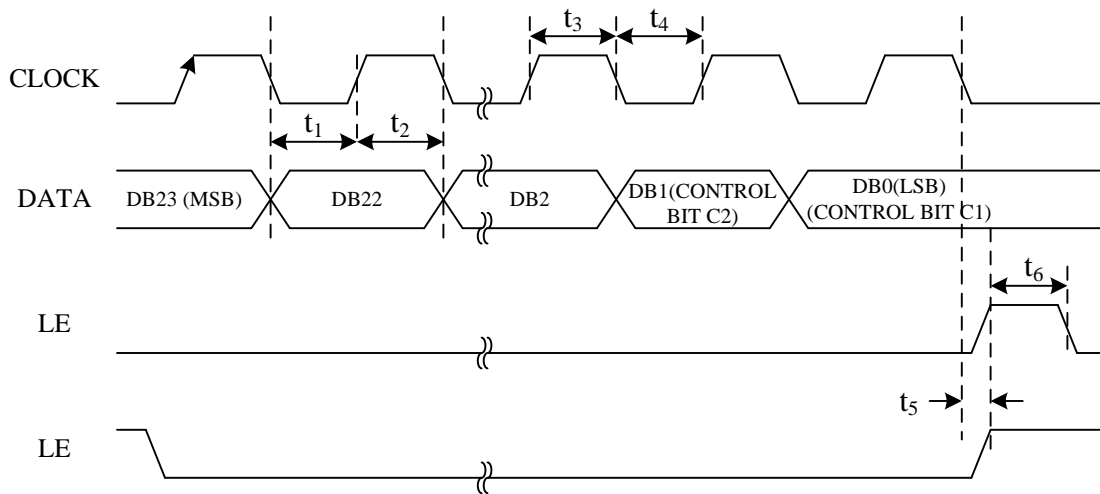


Figure 1. Timing Diagram

There are four 24 bit registers that need to be programmed. Which register is written into is simply controlled by Control Bits C1 and C2. Table I summarizes the Truth Table for Control Bits C1 and C2.

| Control Bits | | Data Latch |
|--------------|----|--------------------------------------|
| C2 | C1 | |
| 0 | 0 | R Counter |
| 0 | 1 | N Counter (A and B) |
| 1 | 0 | Function Latch (Including Prescaler) |
| 1 | 1 | Initialization Latch |

Table I. C2, C1 Truth Table

Table II shows the details of the four 24 bit registers.

| REFERENCE COUNTER LATCH | | | | | | | | | | | | | | | | | | | | | | | |
|-------------------------|------|------|-----------------------|----------------|------|------|---------------------|------|--------------------------|------|------|------|------|-----|-----|-----|-----|-----|-----|-----|-----|--------------|-------|
| RESERVED | | | LOCK DETECT PRECISION | TEST MODE BITS | | | ANTI-BACKLASH WIDTH | | 14-BIT REFERENCE COUNTER | | | | | | | | | | | | | CONTROL BITS | |
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | 0 | 0 | LDP | T2 | T1 | ABP2 | ABP1 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | C2(0) | C1(0) |

| N COUNTER LATCH | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|------|------|---------|----------------|------|------|------|------|------|------|------|------|------|-----|-----|-----|---------------|-----|-----|-----|-----|-------|--------------|--|
| RESERVED | | | CP GAIN | 13-BIT COUNTER | | | | | | | | | | | | | 6-BIT COUNTER | | | | | | CONTROL BITS | |
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| | | G1 | B13 | B12 | B11 | B10 | B9 | B8 | B7 | B6 | B5 | B4 | B3 | B2 | B1 | A6 | A5 | A4 | A3 | A2 | A1 | C2(0) | C1(1) | |

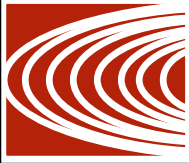
| FUNCTION LATCH | | | | | | | | | | | | | | | | | | | | | | | | |
|-----------------|------|-------------------------|------------------------------|------|------|------|------------------------------|------|------|-----------------------|------|------|------|---------------|-----------------|----------------|-------------|----------------|-----|-----|-------------------------|---------------|--------------|--|
| PRESCALER VALUE | | POWER-DOWN ₂ | CURRENT SETTING ₂ | | | | CURRENT SETTING ₁ | | | TIMER COUNTER CONTROL | | | | FASTLOCK MODE | FASTLOCK ENABLE | CP THREE-STATE | PD POLARITY | MUXOUT CONTROL | | | POWER-DOWN ₁ | COUNTER RESET | CONTROL BITS | |
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| P2 | P1 | PD2 | CP16 | CP15 | CP14 | CP13 | CP12 | CP11 | TC4 | TC3 | TC2 | TC1 | F5 | F4 | F3 | F2 | M3 | M2 | M1 | PD1 | F1 | C2(1) | C1(0) | |

| INITIALIZATION LATCH | | | | | | | | | | | | | | | | | | | | | | | | |
|----------------------|------|-------------------------|------------------------------|------|------|------|------------------------------|------|------|-----------------------|------|------|------|---------------|-----------------|----------------|-------------|----------------|-----|-----|-------------------------|---------------|--------------|--|
| PRESCALER VALUE | | POWER-DOWN ₂ | CURRENT SETTING ₂ | | | | CURRENT SETTING ₁ | | | TIMER COUNTER CONTROL | | | | FASTLOCK MODE | FASTLOCK ENABLE | CP THREE-STATE | PD POLARITY | MUXOUT CONTROL | | | POWER-DOWN ₁ | COUNTER RESET | CONTROL BITS | |
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| P2 | P1 | PD2 | CP16 | CP15 | CP14 | CP13 | CP12 | CP11 | TC4 | TC3 | TC2 | TC1 | F5 | F4 | F3 | F2 | M3 | M2 | M1 | PD1 | F1 | C2(1) | C1(1) | |

Table II. Latch Summary

When using the CPLL66 family in a synthesizer application, all four 24 bit registers need to be written into after power-up. After writing all four latches the first time, subsequent frequency step changes can be accomplished by changing the N Counter Latch only.

Specifications subject to change without notice.



Programming Crystek p/n: CPLL66-2450-2450

The following is specific programming for CPLL66-2450-2450 (2.450 GHz fixed freq. with 100 kHz Step Size and 10 MHz input reference frequency).

Program all three registers with the following:

R Counter Latch: 000190 H
N Counter Latch: 02FD51 H
Function Latch: 9F8083 H

The above values will set the CPLL66-2450-2450 to 2.450 GHz

