

**DESCRIPTION**

The LX5251 is a multimode SCSI terminator that is compatible with the SCSI SPI-2 (Ultra2), SCSI SPI-3 (Ultra3 or Ultra160), and SCSI SPI-4 (Ultra320) specifications developed by the T10 standards committee for low voltage differential (LVD) termination, while providing backwards compatibility to the SCSI, SCSI-2, and SPI single-ended specifications. Multimode compatibility permits the use of legacy devices on the bus without hardware alterations. Automatic mode selection is achieved through voltage detection on the DiffSense line.

The LX5251 utilizes an industry standard LVD architecture. The individual high bandwidth drivers maximize channel separation, reduce channel-to-channel noise and cross talk to insure Ultra320 performance.

When the LX5251 is enabled, the differential sense (DIFFSENSE) pin supplies a voltage between 1.2V and 1.4V. In

application, this pin is tied to the DIFFSENSE input of the corresponding LVD transceivers. This action enables the LVD transceiver function. DIFFSENSE is capable of supplying a maximum of 15mA.

Tying the DIFFSENSE pin high places the LX5251 in a HI-Z state indicating the presence of an HVD device. Tying the pin low places the part in a single-ended mode while also signaling the multimode transceiver to operate in a single-ended mode.

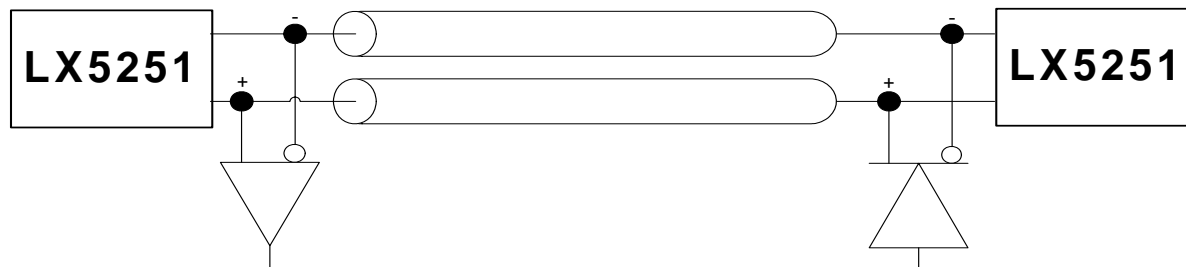
Recognizing the needs of portable and configurable peripherals, the LX5251 has a TTL compatible sleep/disable mode. During this sleep/disable mode, power dissipation is reduced to a meager 15uA while also placing all outputs in a HI-Z state. Also during sleep/disable mode, the DIFFSENSE function is disabled and is placed in a HI-Z state.

The LX5251 also provides a master / slave function. Driving this pin high or floating the pin enables the 1.3V DIFFSENSE reference. Driving the pin low disables the on board DIFFSENSE reference and enables use of an external master reference device.

**KEY FEATURES**

- Compliant with SCSI SPI-2 (Ultra2), SPI-3 (Ultra160), and SPI-4 (Ultra320)
- Auto-Selectable LVD or Single-Ended Termination
- Fast Response, No Output Capacitors Required
- Compatible with Active Negation Drivers
- 15µA Supply Current in Disconnect Mode
- Logic Command Disconnects All Termination Lines
- DiffSense Line Driver
- Ground Driver Integrated for Single-Ended Operation
- Current Limit and Thermal Protection
- Hot-Swap Compatible (Single-Ended)
- Available in 24-pin TSSOP Package

**IMPORTANT:** For the most current data, consult MICROSEMI's website: <http://www.microsemi.com>

**PRODUCT HIGHLIGHT**

**PACKAGE ORDER INFO**

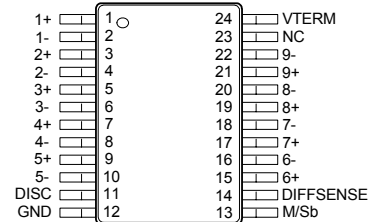
T <sub>A</sub> (°C)	<b>PW</b> Plastic TSSOP 24-Pin
	RoHS Compliant / Pb-free Transition DC: 0442
0 to 70	<b>LX5251CPW</b>

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX5251CPW-TR)

**ABSOLUTE MAXIMUM RATINGS**

Term Power ( $V_{TERM}$ ) ..... -0.3V to 7V  
 Operating Junction Temperature ..... 150°C  
 Storage Temperature Range ..... -65°C to 150°C  
 Peak Package Solder Reflow Temperature (40 second maximum exposure)..... 260°C (+0, -5)

Note: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

**PACKAGE PIN OUT**


**PW PACKAGE**  
(Top View)

N/C = Not internally connected

RoHS / Pb-free 100% Matte Tin Lead Finish

**THERMAL DATA**
**PW 24 Pin Plastic TSSOP**

**THERMAL RESISTANCE-JUNCTION TO AMBIENT,  $\theta_{JA}$**  **100°C/W**

Junction Temperature Calculation:  $T_J = T_A + (P_D \times \theta_{JA})$ .  
 The  $\theta_{JA}$  numbers are guidelines for the thermal performance of the device/pc-board system.  
 All of the above assume no ambient airflow.  $\theta_{JA}$  can vary significantly depending on mounting technique.

**MASTER/SLAVE FUNCTION TABLE**

Master/Slave	DIFFSENSE Status	
	DIFFSENSE	DIFFSENS
L*	HI Z	0mA
H	1.3V	10mA Source
Open (Pull-Up)	1.3V	10mA Source

\* When in Low state, terminator will sense state of DIFFSENS line.

**DIFFSENSE/POWER UP/POWER DOWN FUNCTION TABLE**

DISCONNECT	DIFFSENSE	Outputs		Quiescent Current
		Status	Type	
L	< 0.5V	Enable	SE	55mA
L	0.7V – 1.9V	Enable	LVD	35mA
L	> 2.4V	Disable	HI-Z	8mA
H or Open	X	Disable	HI-Z	10µA

**RECOMMENDED MAX OPERATING CONDITIONS**

Parameter	Symbol	LX5251			Units
		Min	Typ	Max	
VTerm	V <sub>TERM</sub>	2.9		5.25	V
LVD SE		3.5		5.25	
Signal Line Voltage		0		5.0	V
Disconnect Input Voltage		0		V <sub>TERM</sub>	V
Operating Junction Temperature	T <sub>J</sub>	0		125	°C

**ELECTRICAL CHARACTERISTICS**

Unless otherwise specified, the following specifications apply over the operating ambient temperature  $0^{\circ}\text{C} \leq T_A \leq 70^{\circ}\text{C}$ , VTerm = 4.75V, and DISC = L.

Parameter	Symbol	Test Conditions	LX5251			Units
			Min	Typ	Max	
<b>LVD Terminator Section</b>						
VTerm Supply Current	LVD <sub>ICC</sub>	All term lines open		35	45	mA
		DISC > 2.0V		15	35	μA
Common Mode Voltage	V <sub>CM</sub>		1.125	1.25	1.375	V
Offset Voltage	V <sub>OS</sub>	Open circuit between (-) and (+) terminals	100	112	125	mV
Differential Terminator Impedance	Z <sub>O</sub>	V <sub>OUT</sub> Differential = -1V to +1V	100	105	110	Ω
Common Mode Impedance	Z <sub>CM</sub>	0.5V to 2V	110	150	195	Ω
Output Capacitance (Note 1)	C <sub>O</sub>	DISC > 2.0V			3	pF
Mode Change Delay	t <sub>DF</sub>	DiffSense = 1.4V to 0V	100	115	300	ms
<b>DiffSense Section</b>						
DiffSense Output Voltage	V <sub>DIFF</sub>		1.2	1.3	1.4	V
DiffSense Output Source Current	I <sub>DIFF</sub>	V <sub>DIFF</sub> = 0V	5		15	mA
DiffSense Sink Current	I <sub>SINK(DIFF)</sub>	V <sub>DIFF</sub> = 2.75V	20		200	μA
<b>Single Ended Section</b>						
VTerm Supply Current	SE <sub>ICC</sub>	All tem lines = Open, Master/Slave = 0V		55	75	mA
		All tem lines = 0.2V, Master/Slave = 0V		250	290	mA
		DISC > 2.0V; T <sub>A</sub> = 25°		15	35	μA
Termination Output High Voltage	V <sub>O</sub>		2.5	2.7	3.1	V
Output Current	I <sub>O</sub>	V <sub>OUT</sub> = 0.2V	18.5	22.5	24	mA
Sink Current	I <sub>SINK</sub>	V <sub>OUT</sub> = 4V, All lines	40	65		mA
Output Capacitance (Note 1)	C <sub>O</sub>	DISC > 2.0V			3	pF
Output Leakage	I <sub>DDQ</sub>	DISC > 2.0V ; V <sub>LINE</sub> = 0 to 4V, T <sub>A</sub> = 25°			2	μA
	I <sub>HP</sub>	DISC > 2.0V ; V <sub>TERM</sub> = Open, V <sub>LINE</sub> = 2.7V, T <sub>A</sub> = 25°		1		μA
Ground Driver Impedance	Z <sub>G</sub>	I = 1mA			100	Ω

**ELECTRICAL CHARACTERISTICS (CONTINUED)**

Unless otherwise specified, the following specifications apply over the operating ambient temperature  $0^{\circ}\text{C} \leq T_A \leq 125^{\circ}\text{C}$ ,  $V_{\text{Term}} = 4.75\text{V}$ , and DISCONNECT = L.

Parameter	Symbol	Test Conditions	LX5251			Units
			Min	Typ	Max	
<b>DISCONNECT Section</b>						
Disconnect Thresholds	$V_{\text{TH}}$		0.8		2.0	V
Input Current	$I_{\text{IL}}$	DISC = 0V		100		nA
	$I_{\text{IH}}$	DISC = 2.4V			10	$\mu\text{A}$
<b>MASTER/SLAVE Section</b>						
Master/Slave Thresholds	$V_{\text{TH(MS)}}$		0.8		2.0	V
Input Current	$I_{\text{IL(MS)}}$	Master/Slave = 0V			10	$\mu\text{A}$
	$I_{\text{IH(MS)}}$	Master/Slave = 2.4V		100		nA

Note 1: Guaranteed by design.

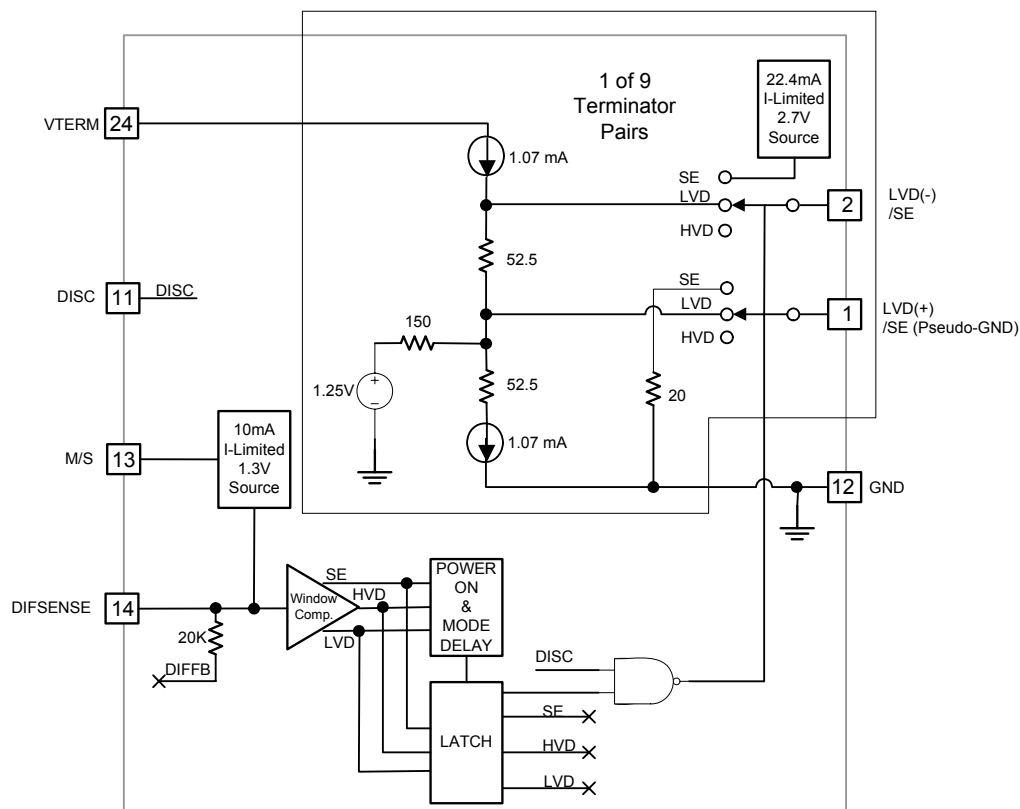
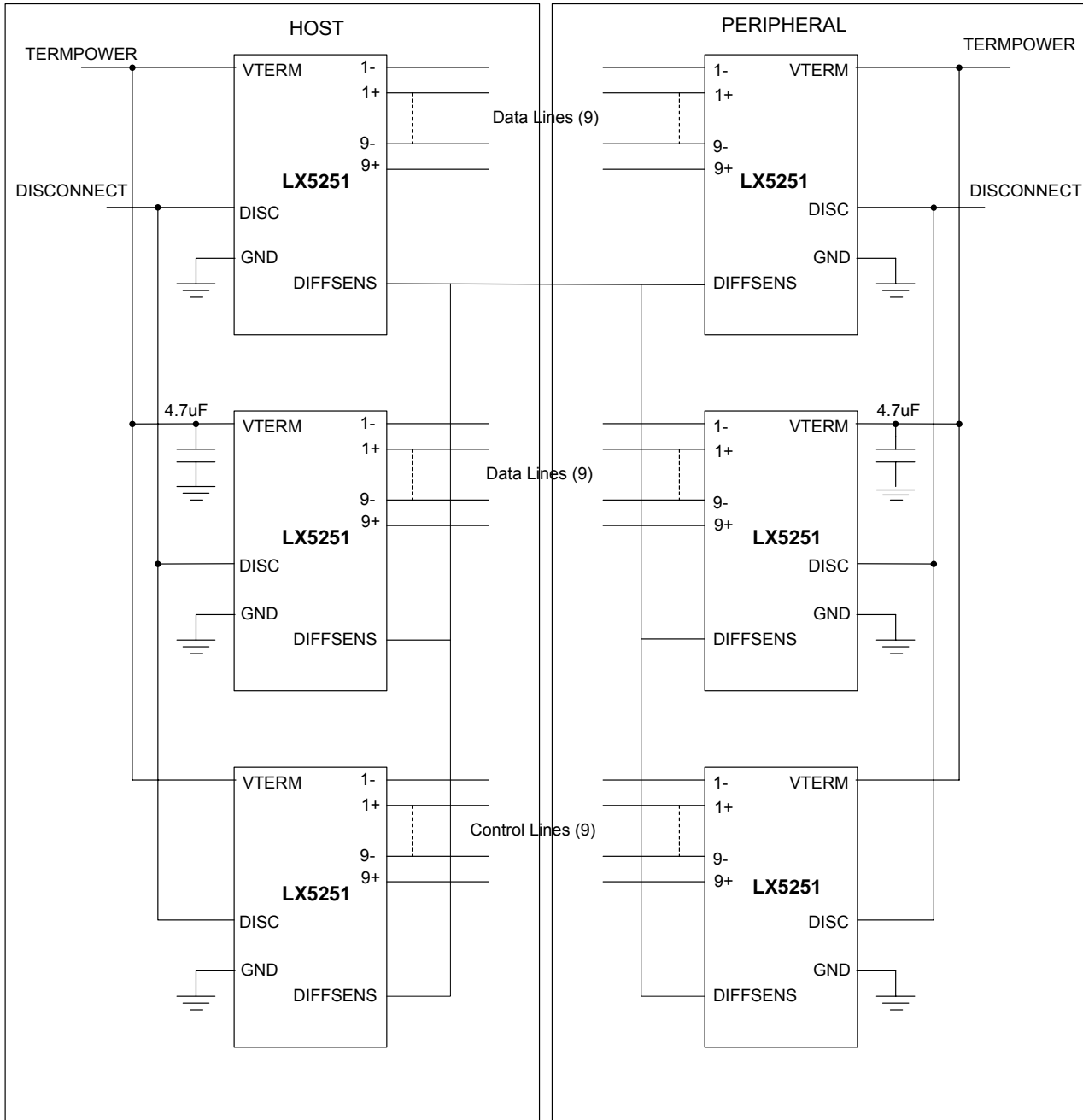
**BLOCK DIAGRAM**


Figure 1 – LX5251 Block Diagram

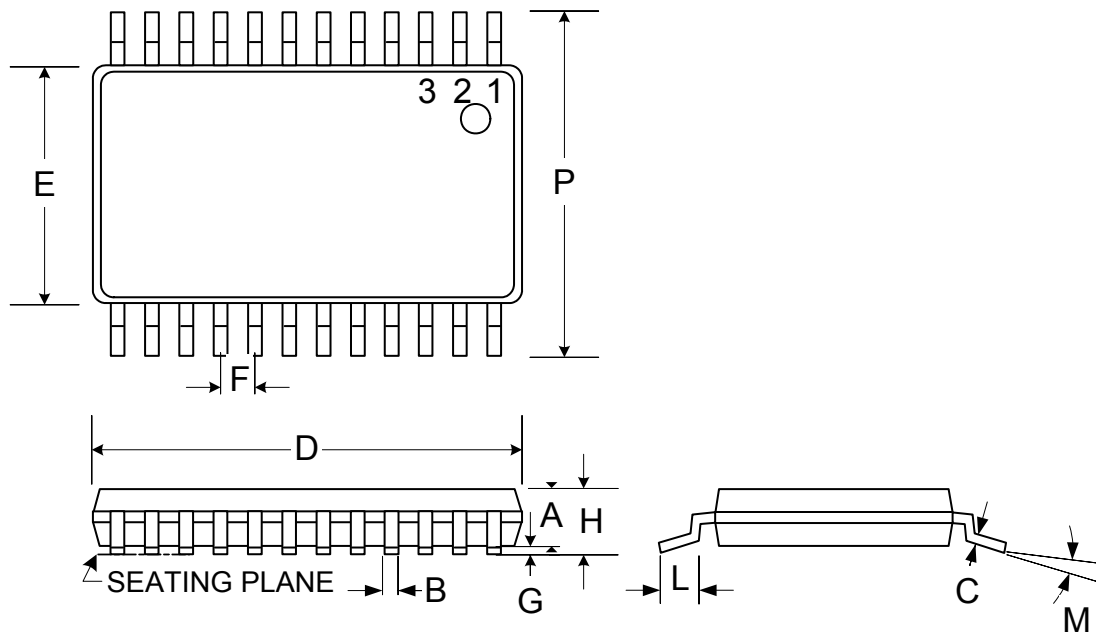
**FUNCTIONAL PIN DESCRIPTION**

PIN NAME	DESCRIPTION
1-, 2-, 3-, 4-, 5-, 6-, 7-, 8-, 9-	Negative signal termination lines for LVD mode. Signal termination lines for SE mode.
1+, 2+, 3+, 4+, 5+, 6+, 7+, 8+, 9+	Positive signal termination lines for LVD mode. Psuedo-ground lines for SE mode.
V <sub>TERM</sub>	Power supply pin for terminator. Connect to SCSI bus VTERM. Musts be decoupled by one 4.7 $\mu$ F low-ESR capacitor for every three terminator devices. It is absolutely necessary to connect this pin to the decoupling capacitor through a very low impedance (big traces to PCB). Keeping distances very short from the decoupling capacitors is somewhat layout dependent and some applications may benefit from high frequency decoupling with 0.1 $\mu$ F capacitors at V <sub>TERM</sub> pin.
DISCONNECT	Enables/Disables terminator. See Power Down Function Table for logic levels.
GND	Terminator ground pin. Connect to ground.
MASTER/SLAVE	Sometimes referred to as M/S pin in this datasheet. Used to select which terminator is the controlling device. M/S pin High or Open enables the DIFFSENSE output drive. Please see MASTER/SLAVE Function Table.
DIFFSENSE	This is a dual function pin. It drives the SCSI bus DIFFSENS line. It is also the sense pin to detect the SCSI bus mode (LVD, SE, or HVD). DIFFSENSE output drive can be disabled with low level on the M/S pin. Please see DIFFSENSE and MASTER/SLAVE Function Tables. Note: Must connect Diffsense signal to Diffsense pin of LX5251.

**APPLICATION SCHEMATIC**


\* DIFFB pin not present on the LX5251CPW. Must connect DiffSense signal to DiffSens pin of each terminator.

**Figure 2 – Microsemi Application Schematic**

**MECHANICAL DRAWINGS**
**PW 24-Pin Thin Small Shrink Outline (TSSOP)**


Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.85	0.95	0.033	0.037
B	0.19	0.30	0.007	0.012
C	0.09	0.20	0.0035	0.008
D	7.70	7.90	0.303	0.311
E	4.30	4.50	0.169	0.177
F	0.65 BSC		0.025 BSC	
G	0.05	0.15	0.002	0.005
H	—	1.10	—	.0433
L	0.50	0.75	0.020	0.030
M	0°	8°	0°	8°
P	6.25	6.55	0.246	0.256
*LC	—	0.10	—	0.004

\* Lead Coplanarity

**Note:**

1. Dimensions do not include mold flash or protrusions; these shall not exceed 0.155mm(.006") on any side. Lead dimension shall not include solder coverage.



**Microsemi**<sup>®</sup>

**LX5251**

**9-Line Multimode SCSI Terminator**

**PRODUCTION DATA SHEET**

**NOTES**

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