

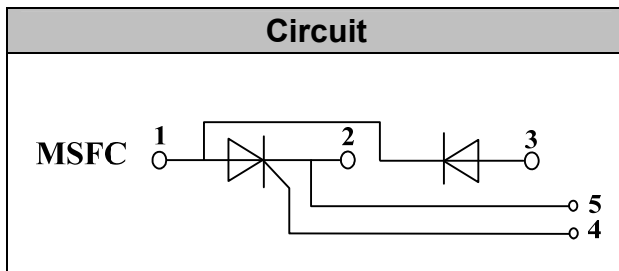
Thyristor/Diode Modules



VRRM / VDRM 800 to 1600V
IFAV / ITAV 160Amp

Applications

- Power Converters
- Lighting Control
- DC Motor Control and Drives
- Heat and temperature control



Features

- International standard package
- High Surge Capability
- Glass passivated chip
- Simple Mounting
- Heat transfer through aluminum oxide DBCceramic isolated metal baseplate
- UL E243882 approved

Module Type

TYPE	VRRM/VDRM	VRSM
MSFC160-08	800V	900V
MSFC160-12	1200V	1300V
MSFC160-16	1600V	1700V

◆Diode

Maximum Ratings

Symbol	Item	Conditions	Values	Units
ID	Output Current(D.C.)	Tc=85°C	160	A
IFSM	Surge forward current	t=10mS Tvj =45°C	5400	A
i ² t	Circuit Fusing Consideration		145000	A ² s
Visol	Isolation Breakdown Voltage(R.M.S)	a.c.50HZ;r.m.s.;1min	3000	V
Tvj	Operating Junction Temperature		-40 to +125	°C
Tstg	Storage Temperature		-40 to +125	°C
Mt	Mounting Torque	To terminals(M6)	3±15%	Nm
Ms		To heatsink(M6)	5±15%	Nm
Weight	Module (Approximately)		165	g

Thermal Characteristics

Symbol	Item	Conditions	Values	Units
Rth(j-c)	Thermal Impedance, max.	Junction to Case	0.085	°C/W
Rth(c-s)	Thermal Impedance, max.	Case to Heatsink	0.05	°C/W

Electrical Characteristics

Symbol	Item	Conditions	Values			Units
			Min.	Typ.	Max.	
VFM	Forward Voltage Drop, max.	T=25°C IF =500A			1.70	V
I _{RRM}	Repetitive Peak Reverse Current, max.	Tvj =25°C VRD=VRRM Tvj =125°C VRD=VRRM		≤0.5 ≤9		mA mA

◆ Thyristor

Maximum Ratings

Symbol	Item	Conditions	Values	Units
I_{TAV}	Average On-State Current	Sine 180°; $T_c=85^\circ\text{C}$	160	A
I_{TSM}	Surge On-State Current	$T_{VJ}=45^\circ\text{C}$ $t=10\text{ms}$, sine $T_{VJ}=125^\circ\text{C}$ $t=10\text{ms}$, sine	5400 5000	A
i^2t	Circuit Fusing Consideration	$T_{VJ}=45^\circ\text{C}$ $t=10\text{ms}$, sine $T_{VJ}=125^\circ\text{C}$ $t=10\text{ms}$, sine	145000 125000	A ² s
Visol	Isolation Breakdown Voltage(R.M.S)	a.c.50HZ;r.m.s.;1min	3000	V
T_{vj}	Operating Junction Temperature		-40 to +130	°C
T_{stg}	Storage Temperature		-40 to +125	°C
M_t	Mounting Torque	To terminals(M6)	$3 \pm 15\%$	Nm
M_s		To heatsink(M6)	$5 \pm 15\%$	Nm
di/dt	Critical Rate of Rise of On-State Current	$T_{VJ}=T_{VJM}$, $2/3V_{DRM}$, $I_G=500\text{mA}$ $T_r < 0.5\mu\text{s}$, $t_p > 6\mu\text{s}$	200	A/ μs
dv/dt	Critical Rate of Rise of Off-State Voltage, min.	$T_J=T_{VJM}$, $2/3V_{DRM}$ linear voltage rise	1000	V/ μs
a	Maximum allowable acceleration		50	m/s^2

Thermal Characteristics

Symbol	Item	Conditions	Values	Units
$R_{th(j-c)}$	Thermal Impedance, max.	Junction to Case	0.17	°C/W
$R_{th(c-s)}$	Thermal Impedance, max.	Case to Heatsink	0.10	°C/W

Electrical Characteristics

Symbol	Item	Conditions	Values			Units
			Min.	Typ.	Max.	
V_{TM}	Peak On-State Voltage, max.	$T=25^\circ\text{C}$ $I_T=500\text{A}$			1.70	V
I_{RRM}/I_{DRM}	Repetitive Peak Reverse Current, max. / Repetitive Peak Off-State Current, max.	$T_{VJ}=T_{VJM}$, $V_R=V_{RRM}$, $V_D=V_{DRM}$			40	mA
V_{TO}	On state threshold voltage	For power-loss calculations only ($T_{VJ}=125^\circ\text{C}$)			0.85	V
r_T	Value of on-state slope resistance. max	$T_{VJ}=T_{VJM}$			1.5	m Ω
V_{GT}	Gate Trigger Voltage, max.	$T_{VJ}=25^\circ\text{C}$, $V_D=6\text{V}$			3	V
I_{GT}	Gate Trigger Current, max.	$T_{VJ}=25^\circ\text{C}$, $V_D=6\text{V}$			150	mA
V_{GD}	Non-triggering gate voltage, max.	$T_{VJ}=125^\circ\text{C}$, $V_D=2/3V_{DRM}$			0.25	V
I_{GD}	Non-triggering gate current, max.	$T_{VJ}=125^\circ\text{C}$, $V_D=2/3V_{DRM}$			10	mA
I_L	Latching current, max.	$T_{VJ}=25^\circ\text{C}$, $R_G=33\Omega$		300	1000	mA
I_H	Holding current, max.	$T_{VJ}=25^\circ\text{C}$, $V_D=6\text{V}$		150	400	mA
tg _d	Gate controlled delay time	$T_{VJ}=25^\circ\text{C}$, $I_G=1\text{A}$, $di/dt=1\text{A}/\mu\text{s}$		1		μs
tq	Circuit commutated turn-off time	$T_{VJ}=T_{VJM}$		100		μs

Performance Curves

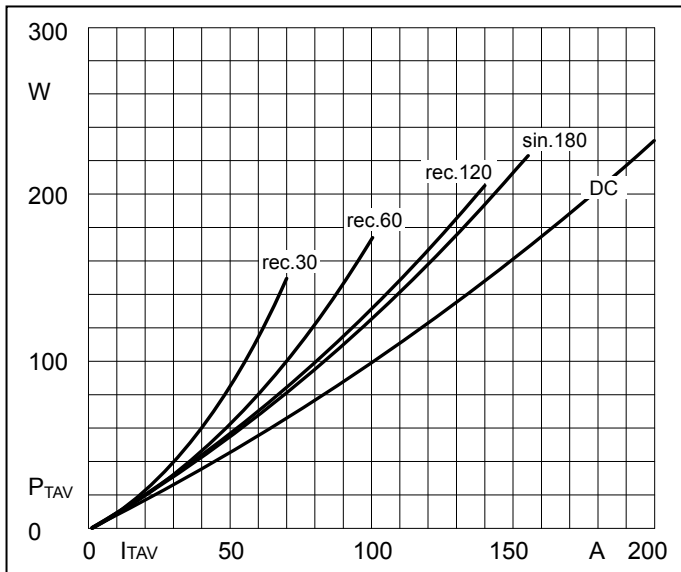


Fig1. Power dissipation

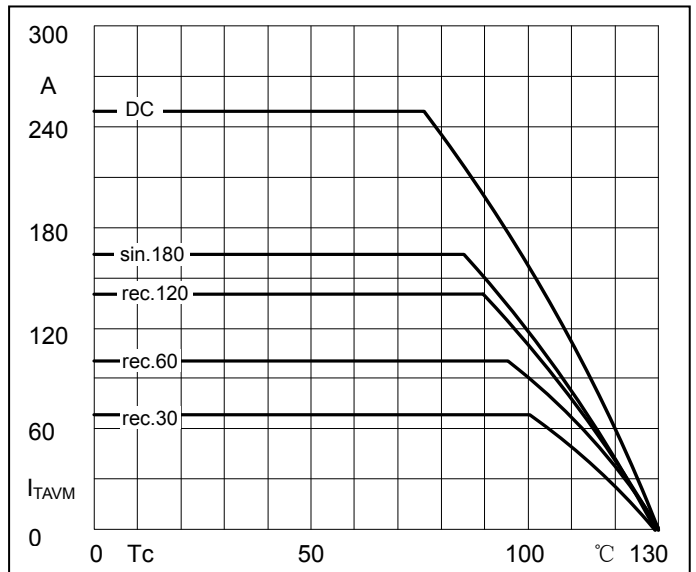


Fig2. Forward Current Derating Curve

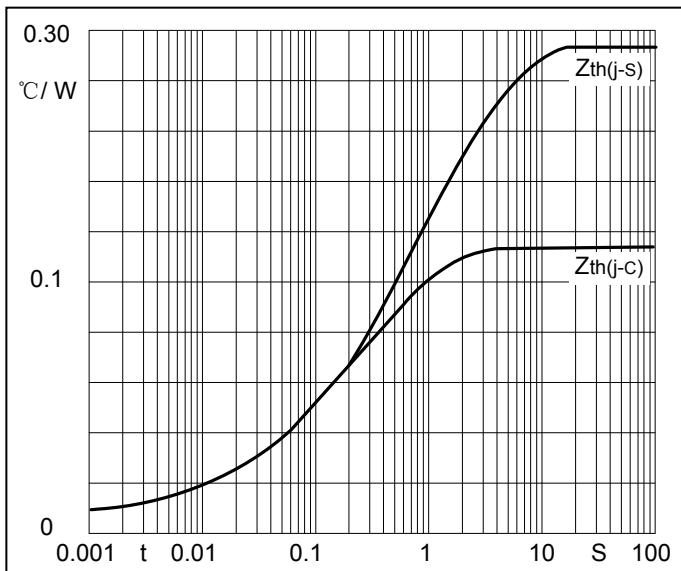


Fig3. Transient thermal impedance

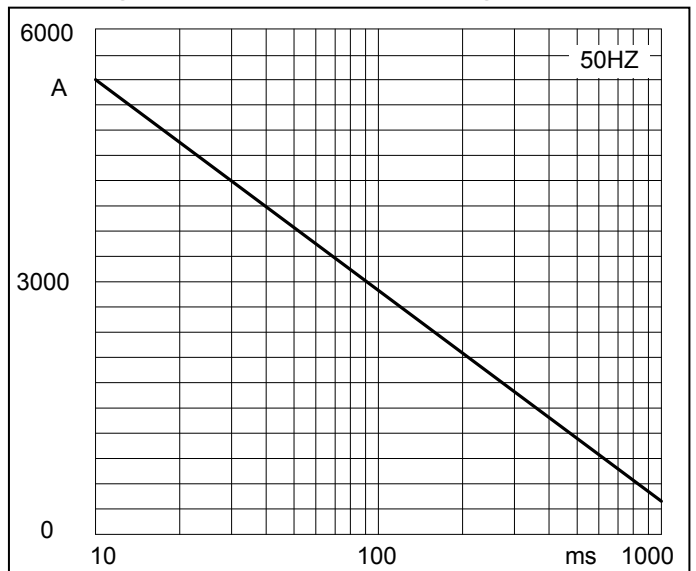


Fig4. Max Non-Repetitive Forward Surge Current

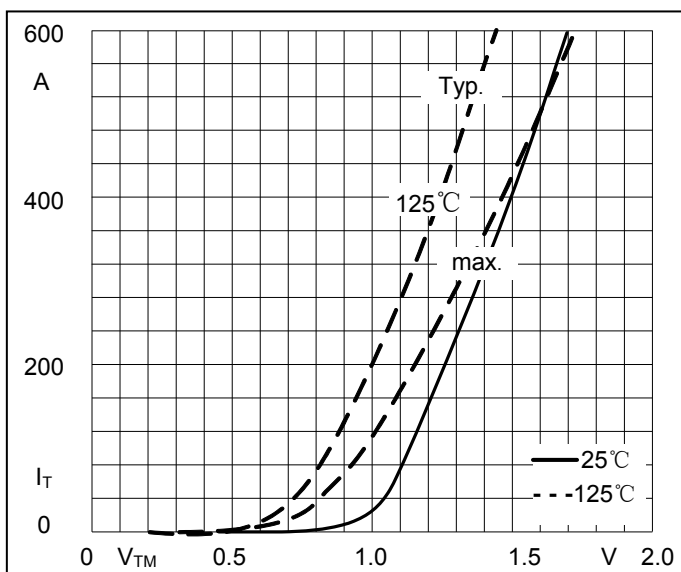


Fig5. Forward Characteristics

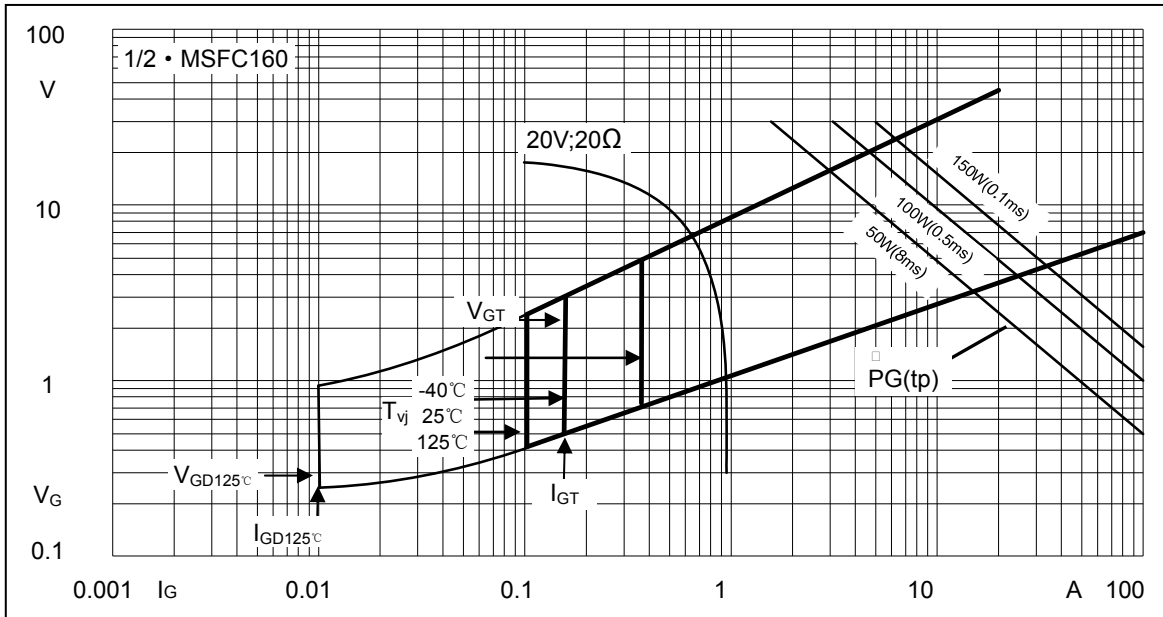


Fig6. Gate trigger Characteristics

Package Outline Information

