TH71112
868/915MHz FSK/ASK Receiver

Features

Double-conversion superhet architecture for high degree of image rejection
FSK demodulation with phase-coincidence demodulator
Low current consumption in active mode and very low standby current
Switchable LNA gain for improved dynamic range
RSSI allows signal strength indication and ASK detection
32-pin Low profile Quad Flat Package (LQFP)

Ordering Code

Product Code	Temperature Code	Package Code	Option Code	Packing Form Code
TH71112	E	NE	BAA-000	RE
TH71112	E	NE	BAA-000	TR
TH71112	C	NE	BAA-000	RE
TH71112	C	NE	BAA-000	TR

Legend:

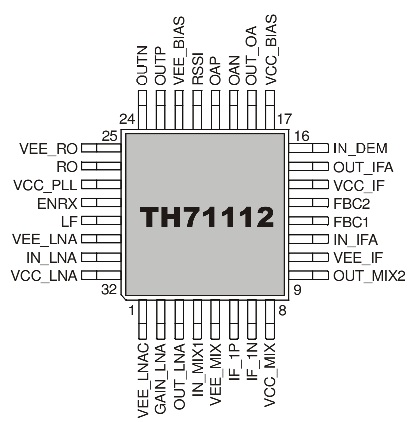
Temperature Code:	E for Temperature Range -40°C to 85°C
	C for Temperature Range 0°C to 70°C
Package Code:	NE for LQFP
Packing Form:	RE for Reel, TR for Tray
Ordering example:	TH71112ENE-BAA-000-RE

Application Examples

- ❑ General digital data transmission
- ❑ Tire Pressure Monitoring Systems (TPMS)
- ❑ Remote Keyless Entry (RKE)
- ❑ Wireless access control
- ❑ Alarm and security systems
- ❑ Garage door openers
- ❑ Remote Controls
- ❑ Home and building automation

Low-power telemetry systems

Pin Description



General Description

The TH71112 FSK/ASK double-conversion superheterodyne receiver IC is designed for applications in the European 868 MHz industrial-scientific-medical (ISM) band, according to the EN 300 220 telecommunications standard. It can also be used for any other system with carrier frequencies ranging from 750 MHz to 990 MHz (e.g. for applications according to FCC part 15).

Document Content

1 Theory of Operation

1.1 General

With the TH71112 receiver chip, various circuit configurations can be arranged in order to meet a number of different customer requirements. For FSK reception the IF tank used in the phase coincidence demodulator can be constituted by an external ceramic discriminator. In ASK configuration, the RSSI signal is fed to an ASK detector, which is constituted by the operational amplifier.

The superheterodyne configuration is double conversion where MIX1 and MIX2 are driven by the internal local oscillator signals LO1 and LO2, respectively. This allows a high degree of image rejection, achieved in conjunction with an RF front-end filter. Efficient RF front-end filtering is realized by using a SAW, ceramic or helix filter in front of the LNA and by adding an LC filter at the LNA output.

A single-conversion variant, called TH71111, is also available. Both Receiver ICs have the same die. At the TH71111 the second mixer MIX2 operates as an amplifier.

The TH71112 receiver IC consists of the following building blocks:

PLL synthesizer (PLL SYNTH) for generation of the first and second local oscillator signals LO1 and LO2, parts of the PLL SYNTH are: the high-frequency VCO1, the feedback dividers DIV_16 and DIV_2, a phase-frequency detector (PFD) with charge pump (CP) and a crystal-based reference oscillator (RO)
Low-noise amplifier (LNA) for high-sensitivity RF signal reception
First mixer (MIX1) for down-conversion of the RF signal to the first IF (IF1)
Second mixer (MIX2) for down-conversion of the IF1 to the second IF (IF2)
IF amplifier (IFA) to amplify and limit the IF2 signal and for RSSI generation
Phase coincidence demodulator (DEMOD) with third mixer (MIX3) to demodulate the IF signal
Operational amplifier (OA) for data slicing, filtering and ASK detection
Bias circuitry for bandgap biasing and circuit shutdown

1.2 Technical Data Overview

Input frequency range: 750 MHz to 990 MHz
Power supply range: 2.3 V to 5.5 V @ ASK
Temperature range: -40 °C to +85 °C
Standby current: 50 nA
Operating current: 7.5 mA @ low gain mode
9.2 mA @ high gain mode
Sensitivity: -112 dBm @ ASK 1)
-106 dBm @ FSK 2)
Maximum data rate: 260 kbps NRZ @ ASK
180 kbps NRZ @ FSK
Range of IF1: 10 MHz to 80 MHz

Range of IF2: 400 kHz to 22 MHz
Maximum input level: -10 dBm @ ASK
0 dBm @ FSK
Image rejection: > 60 dB (e.g. with 868.3 MHz SAW front-end filter and at 10.7 MHz IF2)
Spurious emission: < -70 dBm
Input frequency acceptance range: up to ±100 kHz
RSSI range: 70 dB
FSK deviation range: ±2.5 kHz to ±80 kHz

at 4 kbps NRZ, BER = $3 \cdot 10^{-3}$, 180 kHz IF filter BW, without SAW front-end-filter loss
at 4 kbps NRZ, BER = $3 \cdot 10^{-3}$, ± 20 kHz FSK deviation, 180 kHz IF filter BW, without SAW front-end-filter loss

1.3 Block Diagram

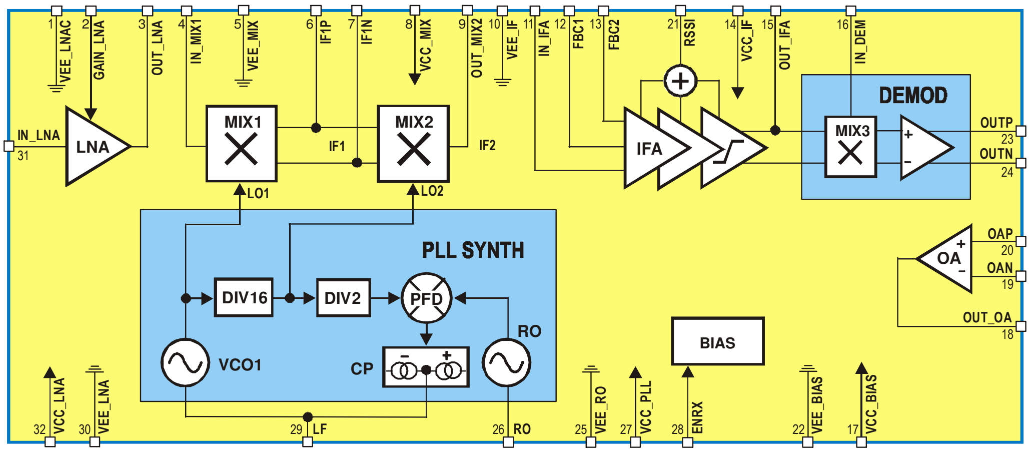


Fig. 1: TH71112 block diagram

1.4 Mode Configurations

ENRX	Mode	Description
0	RX standby	RX disabled
1	RX active	RX enable

Note: ENRX are pulled down internally

1.5 LNA GAIN Control

V_{GAIN_LNA}	Mode	Description
< 0.8 V	HIGH GAIN	LNA set to high gain
> 1.4 V	LOW GAIN	LNA set to low gain

Note: hysteresis between gain modes to ensure stability

1.6 Frequency Planning

Frequency planning is straightforward for single-conversion applications because there is only one IF that can be chosen, and then the only possible choice is low-side or high-side injection of the LO signal (which is now the one and only LO signal in the receiver).

The receiver’s double-conversion architecture requires careful frequency planning. Besides the desired RF input signal, there are a number of spurious signals that may cause an undesired response at the output. Among them are the image of the RF signal (that must be suppressed by the RF front-end filter), spurious signals injected to the first IF (IF1) and their images which could be mixed down to the same second IF (IF2) as the desired RF signal (they must be suppressed by the LC filter at IF1 and/or by low-crosstalk design).

By configuring the TH71112 for double conversion and using its internal PLL synthesizer with fixed feedback divider ratios of N1 = 16 (DIV_16) and N2 = 2 (DIV_2), four types of down-conversion are possible: low-side injection of LO1 and LO2 (**low-low**), LO1 low-side and LO2 high-side (**low-high**), LO1 high-side and LO2 low-side (**high-low**) or LO1 and LO2 high-side (**high-high**). The following table summarizes some equations that are useful to calculate the crystal reference frequency (REF), the first IF (IF1) and the VCO1 or first LO frequency (LO1), respectively, for a given RF and second IF (IF2).

Injection type	high-high	low-low	high-low	low-high
REF	(RF – IF2)/30	(RF – IF2)/34	(RF + IF2)/30	(RF + IF2)/34
LO1	32•REF	32•REF	32•REF	32•REF
IF1	LO1 – RF	RF – LO1	LO1 – RF	RF – LO1
LO2	2•REF	2•REF	2•REF	2•REF
IF2	LO2 – IF1	IF1 – LO2	IF1 – LO2	LO2 – IF1

1.6.1 Selected Frequency Plans

The following table depicts crystal, LO and image signals considering the examples of 868.3 MHz and 915 MHz RF reception at IF2 = 10.7 MHz. The columns in bold depict the selected frequency plans to receive at 868.3 MHz and 915 MHz, respectively.

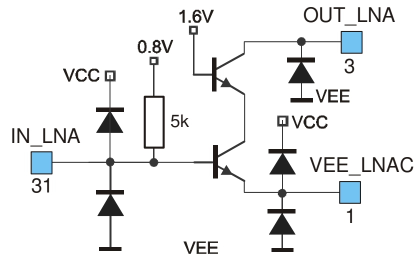
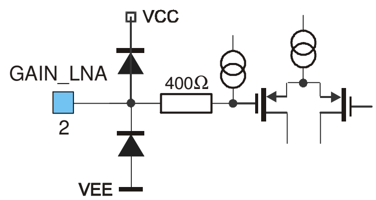
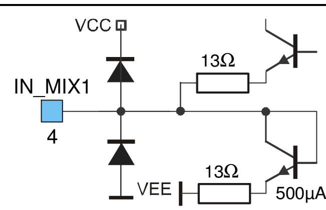
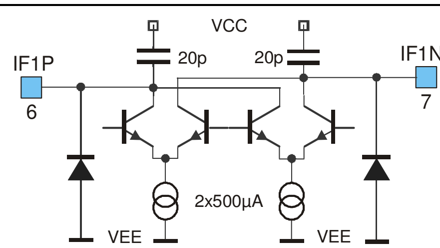
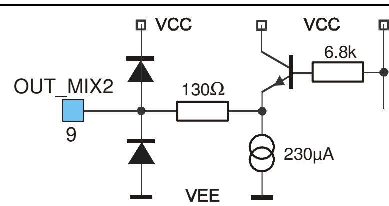
Signal type	RF = 868.3 MHz	RF = 868.3 MHz	RF = 868.3 MHz	RF = 868.3 MHz	RF = 915 MHz	RF = 915 MHz	RF = 915 MHz	RF = 915 MHz
Injection type	high-high	**low-low**	high-low	low-high	high-high	**low-low**	high-low	low-high
REF / MHz	28.58667	**25.22353**	29.3	25.85294	30.14333	**26.59706**	30.85667	27.22647
LO1 / MHz	914.77333	**807.15294**	937.6	827.29412	964.58667	**851.10588**	987.41333	871.24706
IF1 / MHz	46.47333	**61.14706**	69.3	41.00588	49.58667	**63.89412**	72.41333	43.75294
LO2 / MHz	57.17333	**50.44706**	58.6	51.70588	60.28667	**53.19412**	61.71333	54.45294
RF image/MHz	961.24667	**746.00588**	1006.9	786.28824	1014.17	**787.21176**	1059.83	827.49412
IF1 image/MHz	67.87333	**39.74706**	47.9	62.40588	70.98667	**42.49412**	51.01333	65.15294

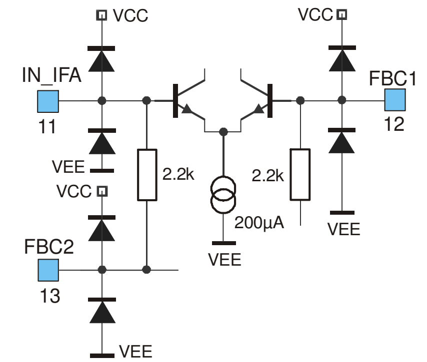
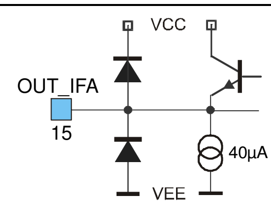
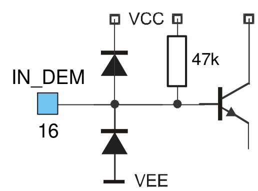
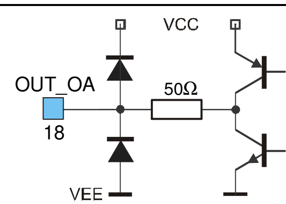
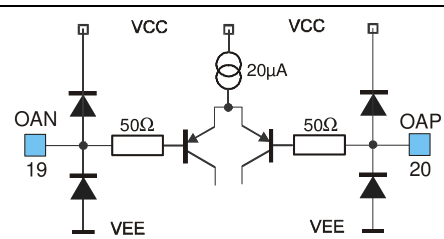
1.6.2 Maximum Frequency Coverage

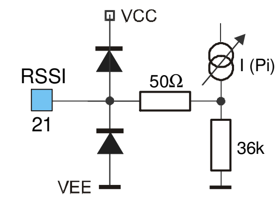
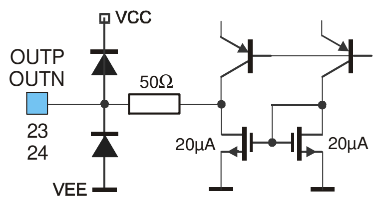
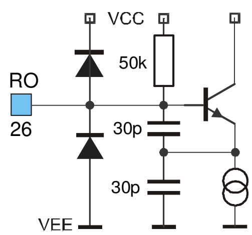
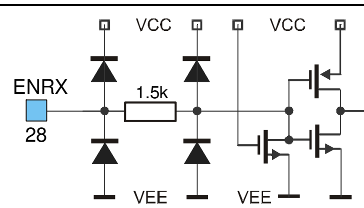
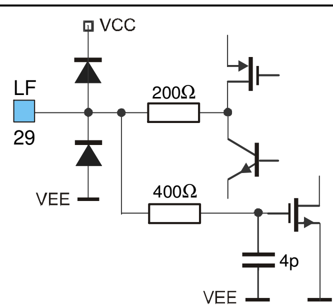
Parameter	f_{min}	f_{max}
Injection type	high-low	low-low
RF / MHz	739.3	998.825
REF / MHz	25.0	29.0625
LO1 / MHz	800	930
IF1 / MHz	60.7	68.825
LO2 / MHz	50.0	58.125
IF2/ MHz	10.7	10.7

The selection of the reference crystal frequency is based on some assumptions. As for example: the first IF and the image frequencies should not be in a radio band where strong interfering signals might occur (because they could represent parasitic receiving signals), the LO1 signal should be in the range of 800 MHz to 930 MHz (because this is the optimum frequency range of the VCO1). Furthermore the first IF should be as high as possible to achieve highest RF image rejection.

2 Pin Definitions and Descriptions

Pin No.	Name	I/O Type	Functional Schematic	Description
3	OUT_LNA	analog output		LNA open-collector output, to be connected to external LC tank that resonates at RF
31	IN_LNA	analog input		LNA input, approx. 26Ω single-ended
1	VEE_LNAC	ground		ground of LNA core (cas-code)
2	GAIN_LNA	analog input		LNA gain control (input with hysteresis) RX standby: no pull-up RX active: pull-up
4	IN_MIX1	analog input		MIX1 input, approx. 33Ω single-ended
5	VEE_MIX	ground		ground of MIX1 and MIX2
6	IF1P	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
7	IF1N	analog I/O		open-collector output, to be connected to external LC tank that resonates at first IF
8	VCC_MIX	supply		positive supply of MIX1 and MIX2
9	OUT_MIX2	analog output		MIX2 output, approx. 330Ω output impedance
10	VEE_IF	ground		ground of IFA and DEMOD

<table>
<tr><th>Pin No.</th><th>Name</th><th>I/O Type</th><th>Functional Schematic</th><th>Description</th></tr>
<tr><td>11</td><td>IN_IFA</td><td>analog input</td><td rowspan="3">
</td><td>IFA input, approx. 2.2kΩ input impedance</td></tr>
<tr><td>12</td><td>FBC1</td><td>analog I/O</td><td>to be connected to external IFA feedback capacitor</td></tr>
<tr><td>13</td><td>FBC2</td><td>analog I/O</td><td>to be connected to external IFA feedback capacitor</td></tr>
<tr><td>14</td><td>VCC_IF</td><td>supply</td><td></td><td>positive supply of IFA and DEMOD</td></tr>
<tr><td>15</td><td>OUT_IFA</td><td>analog I/O</td><td>
</td><td>IFA output and MIX3 input (of DEMOD)</td></tr>
<tr><td>16</td><td>IN_DEM</td><td>analog input</td><td>
</td><td>DEMOD input, to MIX3 core</td></tr>
<tr><td>17</td><td>VCC_BIAS</td><td>supply</td><td></td><td>positive supply of general bias system and OA</td></tr>
<tr><td>18</td><td>OUT_OA</td><td>analog output</td><td>
</td><td>OA output, 40uA current drive capability</td></tr>
<tr><td>19</td><td>OAN</td><td>analog input</td><td rowspan="2">
</td><td>negative OA input</td></tr>
<tr><td>20</td><td>OAP</td><td>analog input</td><td>positive OA input</td></tr>
</table>

Pin No.	Name	I/O Type	Functional Schematic	Description
21	RSSI	analog output		RSSI output, for RSSI and ASK detection, approx. 36kΩ output impedance
22	VEE_BIAS	ground		ground of general bias system and OA
23	OUTP	analog output		FSK positive output, output impedance of 100kΩ to 300kΩ
24	OUTN	analog output		FSK negative output, output impedance of 100kΩ to 300kΩ
25	VEE_RO	ground		ground of DIV, PFD, RO and charge pump
26	RO	analog input		RO input, Colpitts type oscillator with internal feed-back capacitors
27	VCC_PLL	supply		positive supply of DIV, PFD, RO and charge pump
28	ENRX	digital input		mode control input, CMOS-compatible with internal pull-down circuit
29	LF	analog I/O		charge pump output and VCO1 control input
30	VEE_LNA	ground		ground of LNA biasing
32	VCC_LNA	supply		positive supply of LNA biasing

3 Technical Data

3.1 Absolute Maximum Ratings

Parameter	Symbol	Condition / Note	Min	Max	Unit
Supply voltage	V_{CC}		0	7.0	V
Input voltage	V_{IN}		- 0.3	V_{cc}+0.3	V
Input RF level	P_{iRF}	@ LNA input		10	dBm
Storage temperature	T_{STG}		-40	+125	°C
Junction temperature	T_J			+150	°C
Thermal Resistance	R_{thJA}			60	K/W
Power dissipation	P_{diss}			0.1	W
Electrostatic discharge	V_{ESD1}	human body model, 3)	-1.0	+1.0	kV
	V_{ESD2}	human body model, 4)	-0.75	+0.75	

all pins except OUT_LNA, IF1P and IF1N
pin OUT_LNA, IF1P and IF1N

3.2 Normal Operating Conditions

Parameter	Symbol	Condition	Min	Max	Unit
Supply voltage	$V_{CC,\ FSK}$	0 °C to 85 °C	2.5	5.5	V
		-20 °C to 85 °C	2.6	5.5	
		-40 °C to 85 °C	2.7	5.5	
	$V_{CC,\ ASK}$	-40 °C to 85 °C	2.3	5.5	
Operating temperature	T_A	TH71112 E	-40	+85	ºC
		TH71112 C	-10	+70	
Input low voltage (CMOS)	V_{IL}	ENRX pin		0.3*V_{CC}	V
Input high voltage (CMOS)	V_{IH}	ENRX pin	0.7*V_{CC}		V
Input frequency range	f_i		739.3	998.8	MHz
First IF range	f_{IF1}		10	80	MHz
Second IF range	f_{IF2}		0.4	22	MHz
XOSC frequency	f_{ref}	set by the crystal	25	29.063	MHz
VCO frequency	f_{LO}	$f_{LO} = 16 \bullet f_{ref}$	800	930	MHz
Frequency deviation	Δf		$\pm$2.5	$\pm$80	kHz
FSK data rate	R_{FSK}	NRZ, C15 = NIP, 5)		180	kbps
ASK data rate	R_{ASK}	NRZ, C16 = NIP, 5)		260	kbps

B_{IF} = 400 kHz, P_{IN} = -90 dBm

3.3 Crystal Parameters

Parameter	Symbol	Condition	Min	Max	Unit
Crystal frequency	f_0	fundamental mode, AT	25	29.063	MHz
Load capacitance	C_L		10	15	pF
Static capacitance	C_0			7	pF
Series resistance	R_1			50	Ω

3.4 DC Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at T_A= 23 °C and V_{CC} = 3 V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Operating Currents						
Standby current	I_{SBY}	ENRX=0		50	100	nA
Supply current at low gain	$I_{CC, low}$	ENRX=1, GAIN_LNA=1, TH71112 E	4.5	7.5	12.0	mA
		ENRX=1, GAIN_LNA=1, TH71112 C			11.6	
Supply current at high gain	$I_{CC, high}$	ENRX=1, GAIN_LNA=0, TH71112 E	5.0	9.2	14.0	mA
		ENRX=1, GAIN_LNA=0, TH71112 C			13.5	
Digital Pin Characteristics						
Input low voltage CMOS	V_{IL}	ENRX pin	-0.3		0.3*V_{cc}	V
Input high voltage CMOS	V_{IH}	ENRX pin	0.7*V_{CC}		V_{CC}+0.3	V
Pull down current ENRX pin	I_{PDEN}	ENRX=1	0.1	2	10	µA
Low level input current ENRX pin	I_{INLEN}	ENRX=0			0.05	µA
Analog Pin Characteristics						
High level input current GAIN_LNA pin	$I_{INHGAIN}$	GAIN_LNA=1			0.05	µA
Pull up current GAIN_LNA pin active	$I_{PUGAINa}$	GAIN_LNA=0 ENRX=1	0.08	0.15	0.3	µA
Pull up current GAIN_LNA pin standby	$I_{PUGAINs}$	GAIN_LNA=0 ENRX=0			0.05	µA
High gain input voltage	V_{IHGAIN}	ENRX=1			0.7	V
Low gain input voltage	V_{ILGAIN}	ENRX=1	1.5			V
Opamp Characteristics						
Opamp input offset voltage	V_{offs}		-35		35	mV
Opamp input offset current	I_{offs}	$I_{OAP} - I_{OAN}$	-50		50	nA
Opamp input bias current	I_{bias}	$0.5 * (I_{OAP} + I_{OAN})$	-150		150	nA
RSSI Characteristics						
RSSI voltage at low input level	$V_{RSSI, low}$	P_i = -65 dBm, GAIN_LNA=1	0.5	1.0	1.5	V
RSSI voltage at high input level	$V_{RSSI, high}$	P_i = -35 dBm, GAIN_LNA=1	1.2	1.9	2.5	V

3.5 AC System Characteristics

all parameters under normal operating conditions, unless otherwise stated;
typical values at $T_A = 23$ °C and $V_{CC} = 3$ V,
RF at 868.3 MHz; SAW frond-end filter loss and IF at 10.7 MHz;
all parameters based on test circuits as shown in Fig. 2, Fig.3 and Fig. 5

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Receive Characteristics						
Input sensitivity – FSK (standard)	$P_{min, ST}$	B_{IF} = 180kHz, Δf = ±20kHz, 4kbps NRZ, BER ≤ $3{\cdot}10^{-3}$, 6)		-103		dBm
Input sensitivity – FSK (narrow band)	$P_{min, NB}$	B_{IF} = 30kHz, Δf = ±5kHz, 4kbps NRZ, BER ≤ $3{\cdot}10^{-3}$, 6)		-105		dBm
Input sensitivity – ASK	$P_{min, ASK}$	B_{IF} = 180kHz, 4kbps NRZ, BER ≤ $3{\cdot}10^{-3}$, 6)		-109		dBm
Maximum input signal – FSK	$P_{max, FSK}$	BER ≤ $3{\cdot}10^{-3}$ GAIN_LNA = 1		0		dBm
Maximum input signal – ASK	$P_{max, ASK}$	BER ≤ $3{\cdot}10^{-3}$ GAIN_LNA = 1		-10		dBm
Spurious emission	P_{spur}				-70	dBm
Image rejection	ΔP_{imag}			60		dB
Start-up Parameters						
Crystal start-up time	T_{XTL}	ENRX from 0 to 1			0.9	ms
Receiver start-up time	T_{RX}	ENRX from 0 to 1, depends on data slicer time constant, valid data at output			T_{XTL} + R4 · C17	
PLL Parameters						
VCO gain	K_{VCO}			350		MHz/V
Charge pump current	I_{CP}			60		µA

incl. 3 dB loss of front-end SAW filter

4 Test Circuits

4.1 Standard FSK Reception

4.1.1 Standard FSK Application Circuit

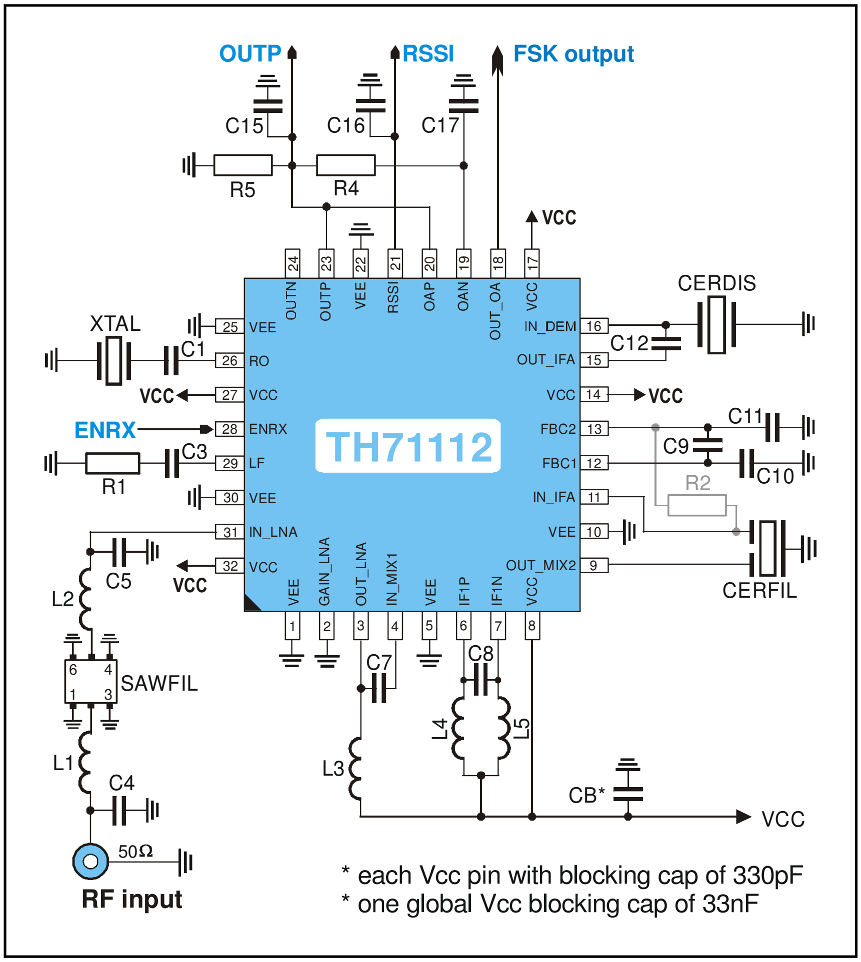


Fig. 2: Test circuit for FSK reception

Circuit Features

- Tolerates input frequency variations
- Well-suited for NRZ, Manchester and similar codes

4.1.2 Standard FSK Component List

Part	Size	Value @ 868.3 MHz	Tolerance	Description
C1	0805	22 pF	±5%	crystal series capacitor
C3	0603	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match SAW filter output
C7	0603	1.0 pF	±5%	MIX1 input matching capacitor
C8	0603	22 pF	±5%	IF1 tank capacitor
C9	0603	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0805	10 pF	±5%	DEMOD phase-shift capacitor
C15	0805	100 pF	±5%	demodulator output low-pass capacitor, this value for data rates < 20 kbps NRZ
C16	0805	1.5 nF	±10%	RSSI output low-pass capacitor
C17	0805	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ
R1	0603	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	±5%	data slicer resistor
R5	0805	220 kΩ	±5%	loading resistor
L1	0603	22 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	22 nH	±5%	
L3	0603	10 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
L4	0805	100 nH	±5%	IF1 tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L5	0805	100 nH	±5%	
XTAL	SMD 6x3.5	25.22353 MHz @ RF = 868.3 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon or equivalent par
SAWFIL	SMD 3x3	SAFCC868MSL0X00 (f_0 =868.3 MHz)	B_{3dB} = 2 MHz	low-loss SAW filter from Murata, or equivalent part
CERFIL	SMD 3.45x3.1	SFECF10M7HA00	B_{3dB} = 180 kHz	ceramic filter from Murata, or equivalent part
CERDIS	SMD 4.5x2	CDSCB10M7GA135		ceramic discriminator from Murata, or equivalent part

- For component values for other frequencies, please refer to the EVB descriptions

4.2 Narrow Band FSK Reception

4.2.1 Narrow Band FSK Application Circuit

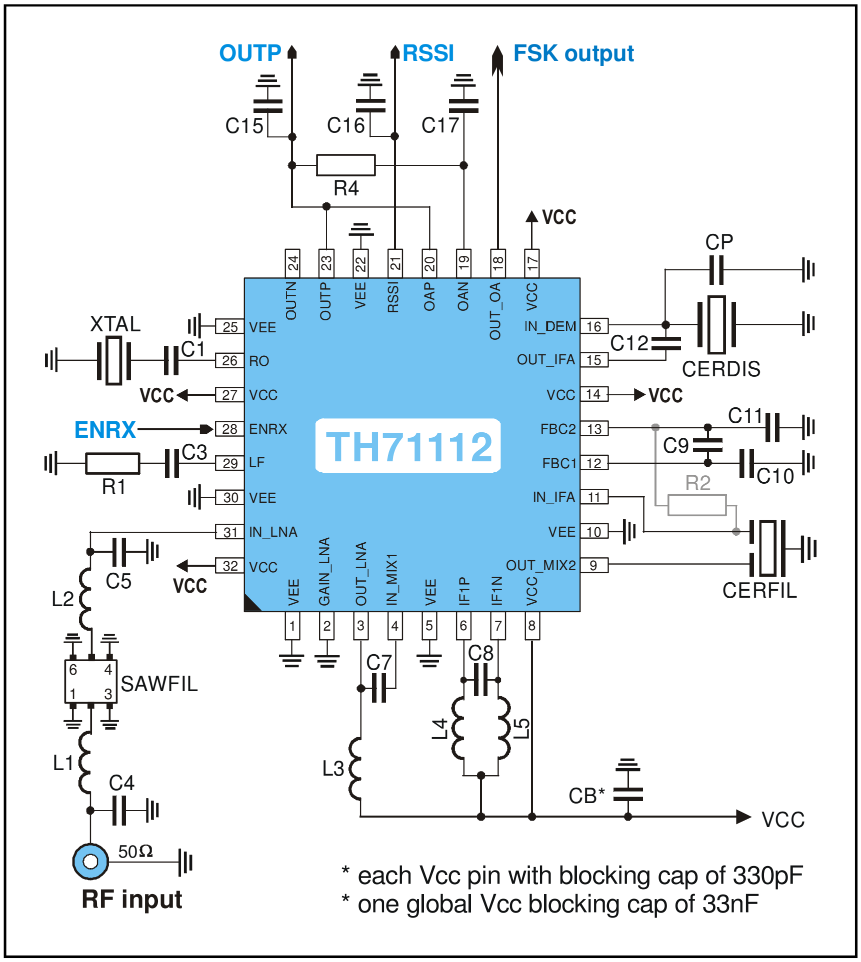


Fig. 3: Test circuit for FSK reception (narrow band)

Circuit Features

- Applicable for narrow band FSK

4.2.2 Narrow Band FSK Component List

Part	Size	Value @ 868.3 MHz	Tolerance	Description
C1	0805	22 pF	±5%	crystal series capacitor
C3	0603	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match SAW filter output
C7	0603	1.0 pF	±5%	MIX1 input matching capacitor
C8	0603	22 pF	±5%	IF1 tank capacitor
C9	0603	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C12	0805	1.5 pF	±5%	DEMOD phase-shift capacitor
C15	0805	220 pF	±5%	demodulator output low-pass capacitor, this value for data rates < 10 kbps NRZ
C16	0805	1.5 nF	±10%	RSSI output low-pass capacitor
C17	0805	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ
CP	0603	6.8 - 8.2 pF	±5%	ceramic resonator loading capacitor
R1	0603	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	±5%	data slicer resistor, this value for 0.4 to 10 kbps NRZ
L1	0603	22 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	22 nH	±5%	
L3	0603	10 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
L4	0805	100 nH	±5%	IF1 tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L5	0805	100 nH	±5%	
XTAL	SMD 6x3.5	25.22353 MHz @ RF = 868.3 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon or equivalent par
SAWFIL	SMD 3x3	SAFCC868MSL0X00 (f_0 =868.3 MHz)	B_{3dB} = 2 MHz	low-loss SAW filter from Murata, or equivalent part
CERFIL	Leaded type	SFKLA10M7NL00	B_{3dB} = 30 kHz	ceramic filter from Murata, or equivalent part
		SFVLA10M7LF00	B_{3dB} = 80 kHz	optional, ceramic filter from Murata, or equivalent part
CERDIS	SMD 4.5x2	CDSCB10M7GA135		ceramic discriminator from Murata, or equivalent part

- For component values for other frequencies, please refer to the EVB descriptions

4.3 ASK Reception

4.3.1 ASK Application Circuit

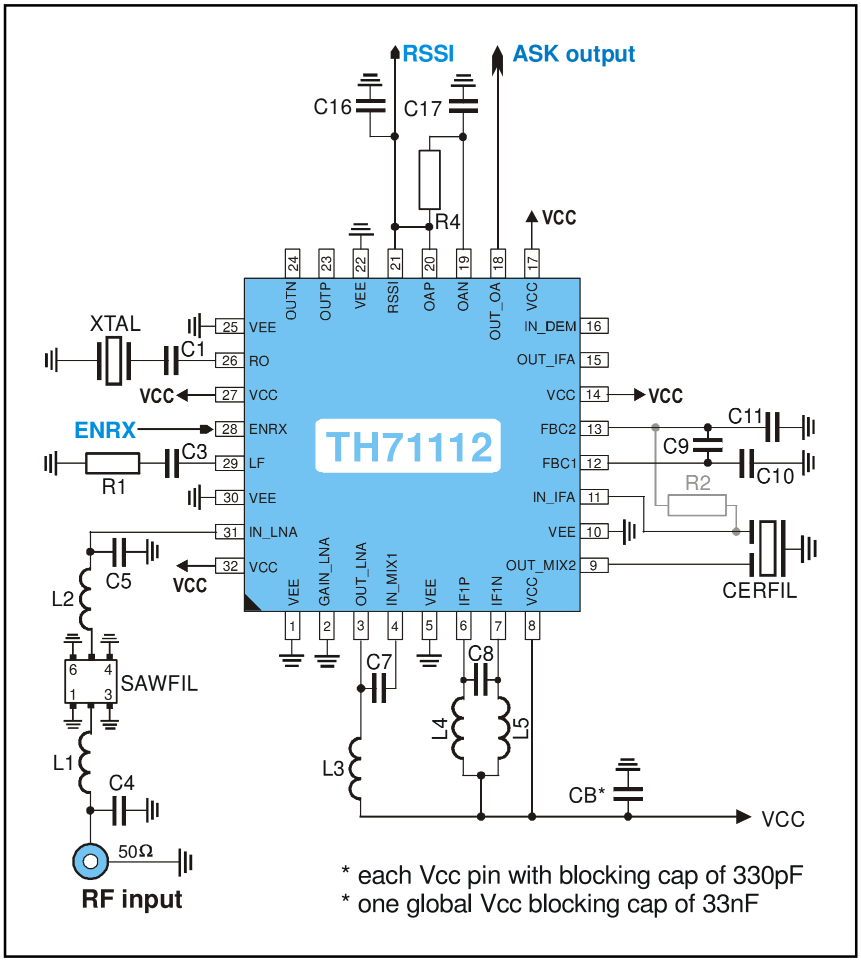


Fig. 4: Test circuit for ASK reception

4.3.2 ASK Component List

Part	Size	Value @ 868.3 MHz	Tolerance	Description
C1	0805	22 pF	±5%	crystal series capacitor
C3	0603	1 nF	±10%	loop filter capacitor
C4	0603	4.7 pF	±5%	capacitor to match SAW filter input
C5	0603	2.7 pF	±5%	capacitor to match SAW filter output
C7	0603	1.0 pF	±5%	MIX1 input matching capacitor
C8	0603	22 pF	±5%	IF1 tank capacitor
C9	0603	33 nF	±10%	IFA feedback capacitor
C10	0603	1 nF	±10%	IFA feedback capacitor
C11	0603	1 nF	±10%	IFA feedback capacitor
C16	0805	1.5 nF	±10%	RSSI output low-pass capacitor, this value for data rates < 10 kbps NRZ, for higher data rates decrease the value
C17	0805	10 nF	±10%	data slicer capacitor, this value for data rates > 0.8 kbps NRZ, for lower data rates increase the value
R1	0603	10 kΩ	±5%	loop filter resistor
R2	0603	330 Ω	±5%	optional CERFIL output matching resistor
R4	0805	330 kΩ	±5%	data slicer resistor
L1	0603	22 nH	±5%	SAW filter matching inductor from Würth-Elektronik (WE-KI series), or equivalent part
L2	0603	22 nH	±5%	
L3	0603	10 nH	±5%	LNA output tank inductor from Würth-Elektronik (WE-KI series), or equivalent part
L4	0805	100 nH	±5%	IF1 tank inductor from Würth-Elektronik (WE-KI series) or equivalent part
L5	0805	100 nH	±5%	
XTAL	SMD 6x3.5	25.22353 MHz @ RF = 868.3 MHz	±25ppm cal. ±30ppm temp.	fundamental-mode crystal from Telcona/Horizon or equivalent par
SAWFIL	SMD 3x3	SAFCC868MSL0X00 (f_0 =868.3 MHz)	B_{3dB} = 2 MHz	low-loss SAW filter from Murata, or equivalent part
CERFIL	SMD 3.45x3.1	SFECF10M7HA00	B_{3dB} = 180 kHz	ceramic filter from Murata, or equivalent part
	Leaded type	SFVLA10M7LF00	B_{3dB} = 80 kHz	optional, ceramic filter from Murata, or equivalent part

- For component values for other frequencies, please refer to the EVB descriptions

5 Package Description

The device TH71112 is RoHS compliant.

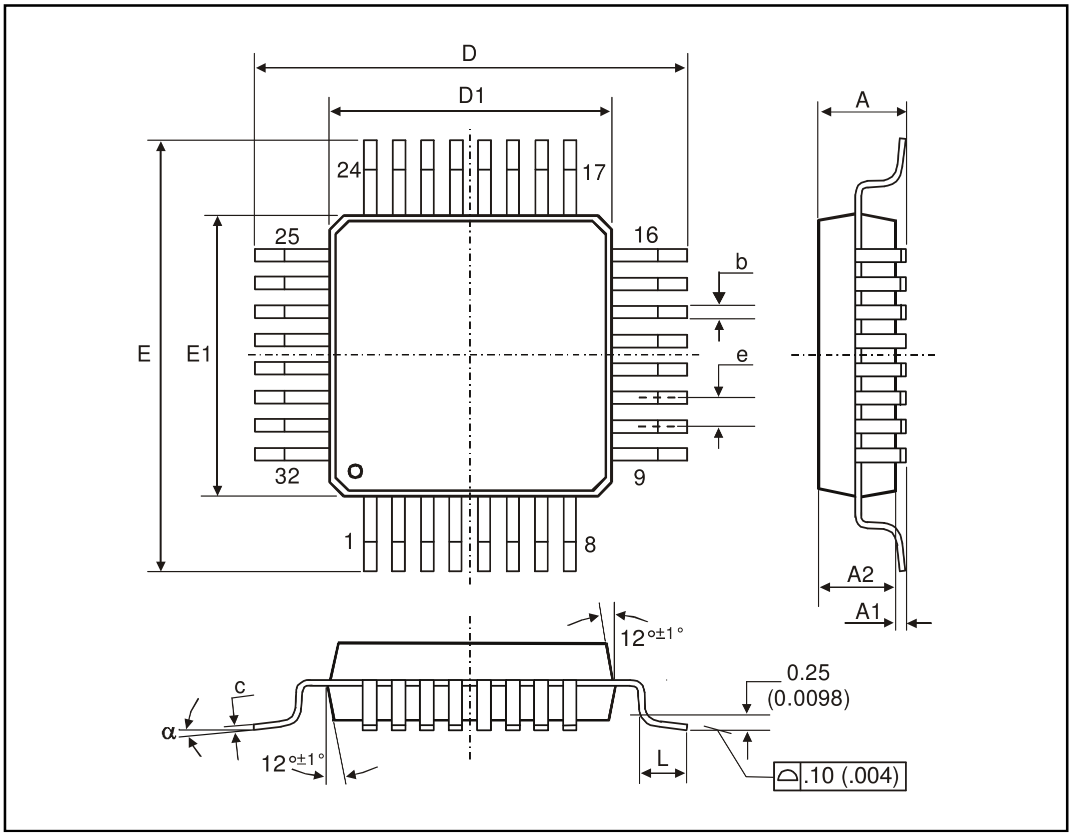


Fig. 6: LQFP32 (Low profile Quad Flat Package)

All Dimension in mm, coplanarity < 0.1mm										
	E1, D1	**E, D**	**A**	**A1**	**A2**	**e**	**b**	**c**	**L**	**α**
min max	7.00	9.00	1.40 1.60	0.05 0.15	1.35 1.45	0.8	0.30 0.45	0.09 0.20	0.45 0.75	0° 7°
All Dimension in inch, coplanarity < 0.004"										
min max	0.276	0.354	0.055 0.063	0.002 0.006	0.053 0.057	0.031	0.012 0.018	0.0035 0.0079	0.018 0.030	0° 7°

5.1 Soldering Information

- The device TH71112 is qualified for MSL3 with soldering peak temperature 260 deg C according to JEDEC J-STD-20

6 Standard information regarding manufacturability of Melexis products with different soldering processes

Our products are classified and qualified regarding soldering technology, solderability and moisture sensitivity level according to following test methods:

Reflow Soldering SMD's (Surface Mount Devices)

- IPC/JEDEC J-STD-020
  Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices
  (classification reflow profiles according to table 5-2)
- EIA/JEDEC JESD22-A113
  Preconditioning of Nonhermetic Surface Mount Devices Prior to Reliability Testing
  (reflow profiles according to table 2)

Wave Soldering SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EN60749-20
  Resistance of plastic- encapsulated SMD's to combined effect of moisture and soldering heat
- EIA/JEDEC JESD22-B106 and EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Iron Soldering THD's (Through Hole Devices)

- EN60749-15
  Resistance to soldering temperature for through-hole mounted devices

Solderability SMD's (Surface Mount Devices) and THD's (Through Hole Devices)

- EIA/JEDEC JESD22-B102 and EN60749-21
  Solderability

For all soldering technologies deviating from above mentioned standard conditions (regarding peak temperature, temperature gradient, temperature profile etc) additional classification and qualification tests have to be agreed upon with Melexis.

The application of Wave Soldering for SMD's is allowed only after consulting Melexis regarding assurance of adhesive strength between device and board.

Melexis is contributing to global environmental conservation by promoting **lead free** solutions. For more information on qualifications of **RoHS** compliant products (RoHS = European directive on the Restriction Of the use of certain Hazardous Substances) please visit the quality page on our website:
http://www.melexis.com/quality.aspx

7 ESD Precautions

Electronic semiconductor products are sensitive to Electro Static Discharge (ESD).
Always observe Electro Static Discharge control procedures whenever handling semiconductor products.

8 Disclaimer

Devices sold by Melexis are covered by the warranty and patent indemnification provisions appearing in its Term of Sale. Melexis makes no warranty, express, statutory, implied, or by description regarding the information set forth herein or regarding the freedom of the described devices from patent infringement. Melexis reserves the right to change specifications and prices at any time and without notice. Therefore, prior to designing this product into a system, it is necessary to check with Melexis for current information. This product is intended for use in normal commercial applications. Applications requiring extended temperature range, unusual environmental requirements, or high reliability applications, such as military, medical life-support or life-sustaining equipment are specifically not recommended without additional processing by Melexis for each application.
The information furnished by Melexis is believed to be correct and accurate. However, Melexis shall not be liable to recipient or any third party for any damages, including but not limited to personal injury, property damage, loss of profits, loss of use, interrupt of business or indirect, special incidental or consequential damages, of any kind, in connection with or arising out of the furnishing, performance or use of the technical data herein. No obligation or liability to recipient or any third party shall arise or flow out of Melexis' rendering of technical or other services.

For the latest version of this document, go to our website at
www.melexis.com

Or for additional information contact Melexis Direct:

Europe, Africa, Asia:
Phone: +32 1367 0495
E-mail: sales_europe@melexis.com

America:
Phone: +1 248 306 5400
E-mail: sales_usa@melexis.com

ISO/TS 16949 and ISO14001 Certified