

**SOP-8**



**Pin Definition:**

- |             |            |
|-------------|------------|
| 1. Source 1 | 8. Drain 1 |
| 2. Gate 1   | 7. Drain 1 |
| 3. Source 2 | 6. Drain 2 |
| 4. Gate 2   | 5. Drain 2 |

**PRODUCT SUMMARY**

$V_{DS}$ (V)	$R_{DS(on)}$ (m $\Omega$ )	$I_D$ (A)
30	13.2 @ $V_{GS} = 10V$	12.2
	18 @ $V_{GS} = 4.5V$	9.4

**Features**

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

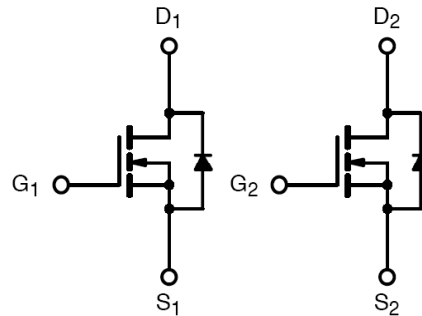
**Application**

- Load Switch
- Dc-DC Conversion

**Ordering Information**

Part No.	Package	Packing
TSM4944DCS RL	SOP-8	2.5Kpcs / 13" Reel

**Block Diagram**



Dual N-Channel MOSFET

**Absolute Maximum Rating** ( $T_a = 25^\circ C$  unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current	$I_D$	12.2	A
Pulsed Drain Current	$I_{DM}$	30	A
Continuous Source Current (Diode Conduction) <sup>a,b</sup>	$I_S$	1.9	A
Maximum Power Dissipation	$P_D$	$T_a = 25^\circ C$	2.3
		$T_a = 75^\circ C$	1.2
Operating Junction Temperature	$T_J$	+150	$^\circ C$
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 to +150	$^\circ C$

**Thermal Performance**

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R_{\theta JC}$	1.8	$^\circ C/W$
Junction to Ambient Thermal Resistance (PCB mounted)	$R_{\theta JA}$	40	$^\circ C/W$

Notes:

- a. Maximum DC current limited by the package
- b. Surface Mounted on 1" x 1" FR4 Board,  $t \leq 10$  sec.

**Electrical Specifications** (Ta = 25°C unless otherwise noted)

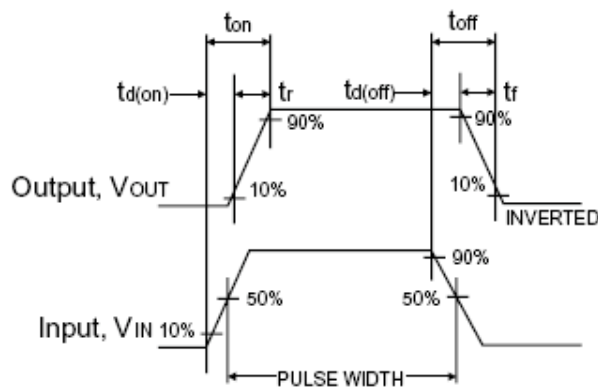
Parameter	Conditions	Symbol	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250uA	BV <sub>DSS</sub>	30	--	--	V
Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250uA	V <sub>GS(TH)</sub>	1.0	1.8	3.0	V
Gate Body Leakage	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V	I <sub>GSS</sub>	--	--	±100	nA
Zero Gate Voltage Drain Current	V <sub>DS</sub> = 30V, V <sub>GS</sub> = 0V	I <sub>DSS</sub>	--	--	1.0	uA
On-State Drain Current	V <sub>DS</sub> ≥ 5V, V <sub>GS</sub> = 10V	I <sub>D(ON)</sub>	30	--	--	A
Drain-Source On-State Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 12.2A	R <sub>DS(ON)</sub>	--	11	13.2	mΩ
	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 9.4A		--	15.4	18	
Forward Transconductance	V <sub>DS</sub> = 15V, I <sub>D</sub> = 15A	g <sub>fs</sub>	--	32	--	S
Diode Forward Voltage	I <sub>S</sub> = 1.9A, V <sub>GS</sub> = 0V	V <sub>SD</sub>	--	0.85	1.3	V
<b>Dynamic<sup>b</sup></b>						
Total Gate Charge	V <sub>DS</sub> = 15V, I <sub>D</sub> = 12.2A, V <sub>GS</sub> = 10V	Q <sub>g</sub>	--	26	--	nC
Gate-Source Charge		Q <sub>gs</sub>	--	6	--	
Gate-Drain Charge		Q <sub>gd</sub>	--	5	--	
Input Capacitance	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz	C <sub>iss</sub>	--	2134	--	pF
Output Capacitance		C <sub>oss</sub>	--	343	--	
Reverse Transfer Capacitance		C <sub>rss</sub>	--	134	--	
<b>Switching<sup>c</sup></b>						
Turn-On Delay Time	V <sub>DD</sub> = 15V, R <sub>L</sub> = 15Ω, I <sub>D</sub> = 1A, V <sub>GEN</sub> = 10V, R <sub>G</sub> = 6Ω	t <sub>d(on)</sub>	--	17	--	ns
Turn-On Rise Time		t <sub>r</sub>	--	3.5	--	
Turn-Off Delay Time		t <sub>d(off)</sub>	--	40	--	
Turn-Off Fall Time		t <sub>f</sub>	--	6	--	

Notes:

- a. pulse test: PW ≤ 300μs, duty cycle ≤ 2%
- b. For DESIGN AID ONLY, not subject to production testing.
- b. Switching time is essentially independent of operating temperature.

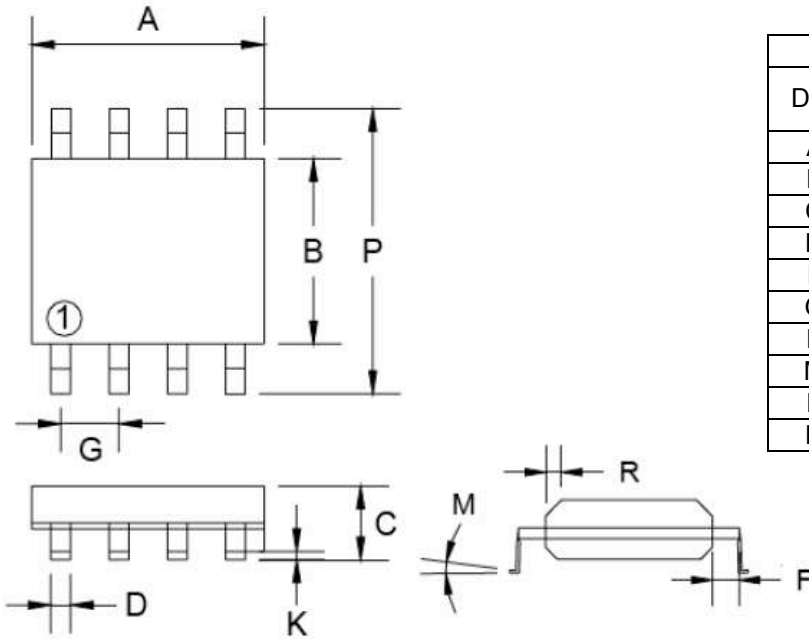


Switching Test Circuit



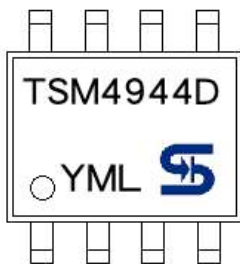
Switchin Waveforms

**SOP-8 Mechanical Drawing**



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

**Marking Diagram**



- Y** = Year Code
- M** = Month Code  
(A=Jan, B=Feb, C=Mar, D=Apr, E=May, F=Jun, G=Jul, H=Aug, I=Sep, J=Oct, K=Nov, L=Dec)
- L** = Lot Code

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