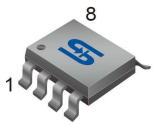
TAIWAN SEMICONDUCTOR

RoHS COMPLIANCE

TSM4539D

Complementary Enhancement MOSFET

SOP-8



Pin Definition:

1. Source 1	8. Drain 1
2. Gate 1	7. Drain 1
3. Source 2	6. Drain 2
4. Gate 2	5. Drain 2

MOSFET PRODUCT SUMMARY

	V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
N-Channel	30	28 @ V_{GS} = 10V	6.5
		42 @ V_{GS} = 4.5V	5.0
P-Channel	-30	65 @ V_{GS} = -10V	-4.2
		90 @ V_{GS} = -4.5V	-3.5

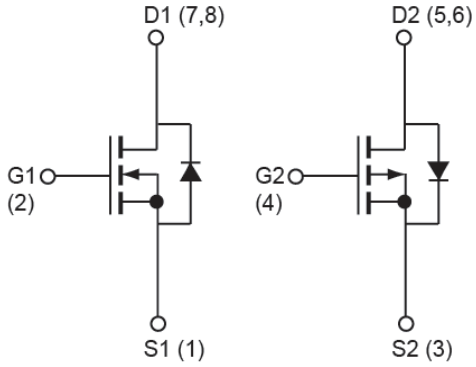
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



N-Channel P-Channel

Ordering Information

Part No.	Package	Packing
TSM4539DCS RLG	SOP-8	2.5Kpcs / 13” Reel

Note: “G” denote for Halogen Free Product

MOSFET Absolute Maximum Rating (T_A=25°C unless otherwise noted)

Parameter	Symbol	N-CH Limit	P-CH Limit	Unit
Drain-Source Voltage	V_{DS}	30	-30	V
Gate-Source Voltage	V_{GS}	±20	±20	V
Continuous Drain Current, V_{GS}	I_D	6.5	-4.2	A
Pulsed Drain Current,	I_{DM}	28	-20	A
Drain-Source Diode Forward Current	I_S	2.5	-1.9	A
Power Dissipation @ Ta = 25°C	P_D	2.1	2.1	W
Operating Junction Temperature	T_J	150		°C
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ +150		°C

Thermal Performance

Parameter	Symbol	N-CH Limit	P-CH Limit	Unit
Junction to Ambient Thermal Resistance	$R\Theta_{JA}$	62.5	62.5	°C/W
Junction to Lead Thermal Resistance	$R\Theta_{JL}$	40	40	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board using 1 inch sq pad size, t ≤ 5sec.

c. Surge Applied at Rated Load Conditions, Half-Wave, Single Phase, 60Hz.

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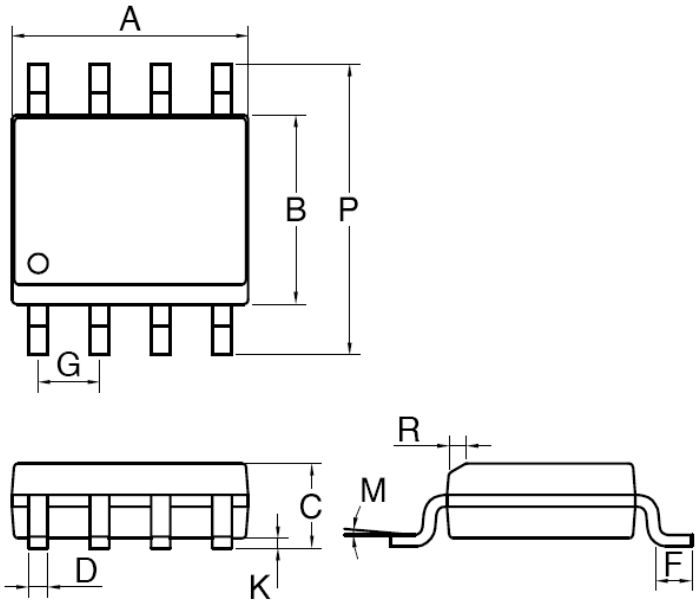
Electrical Specifications (T_A=25°C unless otherwise noted)

Parameter	Conditions	Symbol		Min	Typ	Max	Unit
Static							
Drain-Source Breakdown Voltage	V_{GS}=0V, I_D = 250uA	BV_{DSS}	N-CH	30	--	--	V
	V_{GS}=0V, I_D =-250uA		P-CH	-30	--	--	
Gate Threshold Voltage	V_{DS}=V_{GS}, I_D = 250μA	$V_{GS(TH)}$	N-CH	1.0	1.4	3.0	V
	V_{DS}=V_{GS}, I_D =-250μA		P-CH	-1.0	-1.5	-3.0	
Gate Body Leakage	V_{GS} = ±20V, V_{DS} =0V	I_{GSS}	N-CH	--	--	±100	nA
	V_{GS} = ±20V, V_{DS} =0V		P-CH	--	--	±10	
Zero Gate Voltage Drain Current	V_{DS}=24V, V_{GS} =0V	I_{DSS}	N-CH	--	--	1	μA
	V_{DS}=-24V, V_{GS} =0V		P-CH	--	--	-1	
Drain-Source On-State Resistance[a]	V_{GS}=10V, I_D =6.5A	$R_{DS(ON)}$	N-CH	--	23	28	mΩ
	V_{GS}=-10V, I_D =-4.2A		P-CH	--	50	65	
	V_{GS}=4.5V, I_D =5A		N-CH	--	35	42	
	V_{GS}=-4.5V, I_D =-3.5A		P-CH		82	90	
Dynamic[b]							
Total Gate Charge	N-Channel V_{DS}=10V, I_D=1A, V_{GS}=10V	Q_g	N-CH	--	7	--	nC
			P-CH	--	9.7	--	
Gate-Source Charge	P-Channel V_{DS}=-15V, I_D=-5.2A, V_{GS}=-10V	Q_{gs}	N-CH	--	1.6	--	
			P-CH	--	1.6	--	
Gate-Drain Charge		Q_{gd}	N-CH	--	1.0	--	
			P-CH	--	1.3	--	
Input Capacitance	N-Channel V_{DS}=15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	N-CH	--	610	--	pF
			P-CH	--	100	--	
Output Capacitance	P-Channel V_{DS}=-15V, V_{GS} = 0V, f = 1.0MHz	C_{oss}	N-CH	--	77	--	
			P-CH	--	551	--	
Reverse Transfer Capacitance		C_{rss}	N-CH	--	90	--	
			P-CH	--	60	--	
Switching[b]							
Turn-On Delay Time	N-Channel V_{DD}=15V, I_D = 1A, V_{GEN}=10V, R_G = 6Ω	$t_{d(on)}$	N-CH	--	7	--	nS
			P-CH	--	6.2	--	
Turn-On Rise Time		t_r	N-CH	--	10	--	
			P-CH	--	6.2	--	
Turn-Off Delay Time	P-Channel V_{DD}=-15V, I_D = -1A, V_{GEN}=-10V, R_G = 6Ω	$t_{d(off)}$	N-CH	--	16	--	
			P-CH	--	26	--	
Turn-Off Fall Time		t_f	N-CH	--	7	--	
			P-CH	--	5.5	--	
Diode Forward Voltage	I_S=1 A, V_{GS} = 0V	V_{SD}	N-CH	--	--	1.0	V
	I_S=-1.9A, V_{GS} = 0V		P-CH	--	--	-1.3	

Notes:
a. Pulse test: PW ≤300μS, duty cycle ≤2%
b. For DESIGN AID ONLY, not subject to production testing.

SOP-8 Mechanical Drawing



SOP-8 DIMENSION				
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX.
A	4.80	5.00	0.189	0.196
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27BSC		0.05BSC	
K	0.10	0.25	0.004	0.009
M	0º	7º	0º	7º
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

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